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5 PS JITTER PROGRAMMABLE TIME INTERVAL/FREQUENCY GENERATOR

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Abstract

A new time interval/frequency generator with a jitter below 5 ps is described. The time interval generation mechanism is based on a phase shifting method with the use of a precise DDS synthesizer. The output pulses are produced in a Spartan-6 FPGA device, manufactured by *Xilinx* in 45 nm CMOS technology. Thorough tests of the phase shifting in a selected synthesizer are performed. The time interval resolution as low as 0.3 ps is achieved. However, the final resolution is limited to 500 ps to maximize precision. The designed device can be used as a source of high precision reference time intervals or a highly stable square wave signal of frequency up to 50 MHz.

Keywords: time interval generator, digital-to-time converter, DDS synthesizer, phase shifting, FPGA.

1. Introduction

Generation of precise *time intervals* (TI) is a complementary process to their measurement. Both time interval counters and *time interval generators* (TIG) are widely used in many industrial and scientific areas. In addition, the identification of parameters of time interval counters depends on the quality of calibration and measurement procedures, that are performed using reference TIs with the aid of TIGs [1–3].

Short TIs can be generated using *e.g.* cables of different lengths, a digital-to-analogue converter and a ramp generator [4–6], delay lines [7–9] or DLLs [10, 11]. To obtain a wider generation range an interpolation method, taken from time interval counters, may be applied [12]. Using this approach the TI is divided into coarse and fine parts. The first one is obtained by counting periods of a reference clock while the second one is based on one of previously mentioned generation methods. A commonly used interpolation method in TIGs involves phase shifting of a reference clock [3, 13–16]. Other ways of getting both wide generation range and high TI resolution are based on counting a certain number of periods of selected values [17] or finding coincidence between two clocks that operate on slightly different frequencies [18].

Along with the development of digital electronics TIGs are willingly implemented using FPGA chips. Programmable arrays can be used either as a complete platform that performs timing generation [3, 15, 16, 18] or just as a part of generator [13, 14, 17, 19, 20]. FPGA build-in DLLs and PLLs greatly facilitate TIG integration in a single chip but, so far, cannot generate as low-jitter TIs as those using external modules, *e.g.* a precise DDS synthesizer [13, 21]. Furthermore, modern DDS chips achieve phase shifting of the output clock with a sub-picosecond step that is still difficult to obtain in FPGA.

Based on promising results obtained in [13] we designed a new TIG that employs a DDS synthesizer for fine phase shifting and an FPGA chip for coarse period counting and pulse generation. Special attention was given to characterization of DDS synthesizer features regarding phase shifting.

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2. Generator design

A block diagram of the designed TIG is shown in Fig. 1. The reference clock signal of 10 MHz frequency provided by either the internal *oven-controlled crystal oscillator* (OCXO) or by any external reference source (*e.g.* rubidium standard), is used to create a high frequency clock signal of 1 GHz in a DSPLL synthesizer. Due to the advantage of DSPLL technology the generated signal has an ultra-low jitter and a high resistance to *process, voltage and temperature* (PVT) variations [22]. Based on this signal the DDS synthesizer produces the main clock signal that can be precisely tuneable regarding the phase shift and frequency. The discrete sample values generated at the synthesizer output are filtered in the *low-pass filter* (LPF) to get a sinusoidal signal. Then the fast discriminator is used to obtain a square wave clock. The clock signal is fed to the FPGA device where output pulses of the TIG are generated by the pulse selector and frequency divider. The pulse generation is initialized with regard to the trigger signal that can be produced internally by the trigger generator or with the use of an external signal. The high quality of clock signals is guaranteed by the use of ultra-low jitter *low-voltage positive-referenced emitter-coupled logic* (LVPECL) standard devices applied in the clock signal path. It applies particularly to the DDS synthesizer, which is characterized by a very low value of residual phase noise (up to −152 dBc/Hz [23]).

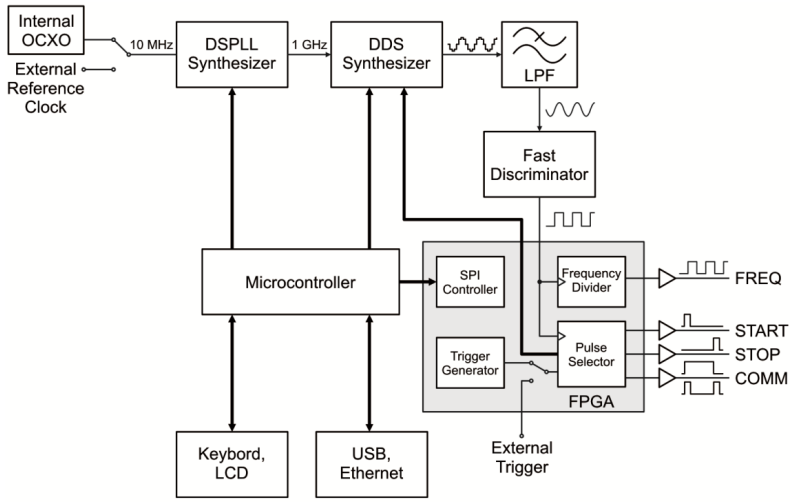

Fig. 1. A block diagram of the TIG.

The TIG can operate either in the time interval mode (START, STOP or COMM outputs) or in the frequency mode (FREQ output). In the first one the TI can be represented as (1) a pair of pulses at two separate outputs (START and STOP), (2) a pair of pulses at a single output (COMM, the time interval common mode), or (3) a single pulse with a declared width (COMM, the time interval width mode). The frequency of the main clock signal in the time interval mode is 50 MHz. The phase shifting of a user-selected value $\Delta\phi$ is performed by the DDS synthesizer synchronously with the START pulse generation in the pulse selector. The STOP pulse is generated after elapsing N periods of the main clock signal and the time interval corresponding to $\Delta\phi$. In the frequency mode the main clock signal for the frequency divider is precisely selected in the DDS within a range from 50 MHz to 100 MHz. The divider enables to further expand the frequency generation range. The pulses generated pulses from the FPGA are distributed (in the low-voltage differential signaling standard LVDS) to the output buffers

Metrol. Meas. Syst., Vol. 24 (2017), No. 1, pp. 57–68.

to obtain possibly steep slopes (rise and fall times < 250 ps) at 50 Ω load. Control of the device is provided either remotely via USB or Ethernet interfaces, or locally with the use of the LCD panel and keyboard integrated with the TIG. All user settings are transformed by the microcontroller into adequate executing commands for the DDS synthesizer and logic implemented in the FPGA chip, *i.e.* the pulse selector, frequency divider and trigger generator.

The designed TIG is packed into a Rack 2U case (Fig. 2) that facilitates its use in laboratory conditions. The front panel provides output signals and a local interface. Inputs of an external trigger and a reference clock are placed on the rear panel together with remote interfaces.

Fig. 2. An external view of the TIG.

2.1. Functional blocks implemented in FPGA chip

FPGA are high performance devices; they operate on relatively high frequency clock signals and can include many user-programmable logic circuits that work autonomously. Hence, to generate the output pulses we selected a Spartan-6 FPGA device manufactured by *Xilinx*. Four modules, *i.e.*: the pulse selector, frequency divider, trigger generator and SPI controller (Fig. 1) were designed using the hardware description language VHDL and were implemented in the FPGA device with the aid of the ISE Design Suite firmware environment [24]. The main task of the FPGA is to generate two output pulses that are mutually shifted in time. This task is executed in the pulse selector module presented in Fig. 3.

The trigger signal, after synchronization to the main clock (CLK_{DDS}) in the double synchronizer, initializes phase shifting in the DDS synthesizer. This operation has to be performed with regard to the DDS synchronization clock (CLK_{SYNC}) of 250 MHz frequency. Thus, another double synchronizer is used for this clock. The DDS profile selector switches between two preselected DDS synthesizer configurations: one with and one without phase shifting. The switching process takes slightly above 100 ns, after execution of the phase shift. To ensure generation of a time interval shorter than 100 ns an additional phase shift delayer is used. It contains a set of serially connected flip-flops. Finally, the delayer initializes generation of START and WIDTH pulses and counting periods in the modulo N counter on the rising edge of the last period of CLK_{DDS} signal that does not contain phase shifting. Then configuration switching is executed in the DDS synthesizer and the main clock signal is shifted in time by a preselected value $\Delta\phi$. The counter operates until it reaches a declared value of N. That causes resetting the double synchronizer and phase shift delayer. Finally, the STOP pulse and falling edge of the WIDTH pulse are generated. The maximum value of N can be 2^{29}. Taking into account the period of CLK_{DDS} clock signal ($T_0 = 20$ ns) the maximum TIG range is slightly above 10 s. The pulse shapers are responsible for generation of pulses with a constant width (START, STOP) and for selection of the operation mode of COMM output (width or common). Also, polarization of pulses can be set.

The square wave signal of a desired frequency is generated in two steps. Firstly, the output frequency of the DDS synthesizer is precisely tuned in a limited range (50 MHz – 100 MHz). Then, the obtained signal is divided by the selectable frequency divider implemented in FPGA. In this way frequencies within an operation range from 0.1 Hz to 1 MHz can be chosen with 1 mHz step, while for the range from 1 MHz to 50 MHz – with a step of 1 Hz. Due to the fact that the pulse selector and the frequency divider operate on the same clock signal, both modules

cannot run in the same time. Therefore, either the time interval mode (active START, STOP and COMM outputs) or the frequency mode (active FREQ output) can be selected in a given time.

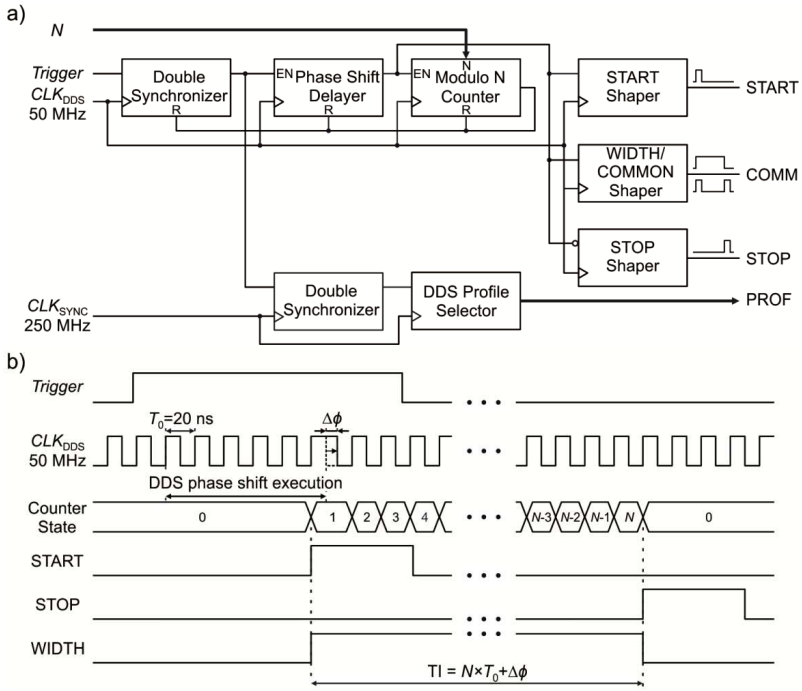

Fig. 3. A block diagram (a) and the operation principle (b) of the pulse selector.

The trigger generator is used to initialize the generation process in the pulse selector. It consists of several clock dividers that are fed by the asynchronous signal with regard to the CLK_{DDS} clock. The SPI controller (Fig. 1) receives commands from the microcontroller, such as: "set N" for the modulo counter or "divide value" for the frequency divider, "choose an operation mode (time interval/frequency, width/common mode)", "select a trigger (internal/ external, internal trigger frequency)".

2.2. DDS Synthesizer features

The TIG parameters depend mainly on the main clock quality and possibilities of its phase shifting. Therefore, the choice of synthesizers is crucial. The selected AD9910 (*Analog Devices*) DDS synthesizer is characterised by 0.23 Hz frequency resolution and $1/2^{16}$ clock period phase shift step [23]. If 50 MHz clock is applied, the minimum $\Delta\phi$ reaches a sub-picosecond value (20 ns / $2^{16} \approx 305$ fs).

We considered three possibilities of using DDS synthesizers. In the first approach we used two of them synchronized to each other. The first synthesizer generated a clock signal for the START shaper, whereas the second one – a signal of the same frequency but shifted in time for the STOP shaper. Both shapers were driven by separate signals so it was possible to generate time intervals from 0 duration. However, the synchronization of both synthesizers caused extension of the generated time interval jitter value above 20 ps. It is a reasonably good result in the case of synchronization, but it is insufficient for the expected TIG precision. For this reason further work with that design was discontinued.

Metrol. Meas. Syst., Vol. 24 (2017), No. 1, pp. 57–68.

The second and third approaches are based on a single DDS synthesizer but differ in the way of phase shift control. According to [23], the value of phase shift is set by the *Phase Offset Word* (POW) register. The value can be changed either by using a dedicated 16-bit parallel port or by choosing preselected profiles. Each profile consists of a group of 8 registers that contain operating parameters for the output signal. A particular profile is activated using a 3-bit PROF port. In the case of TIG two profiles can be configured as signals of the same frequency and amplitude but of different phase shift values. When profiles are changed then only the content of POW register is modified. The parallel port provides direct access to the POW register. In both cases – the parallel port and profile switching – a similar phase shift execution time is needed. Thus, we have chosen the profile selection that minimizes the number of connections on a PCB. Because switching is performed only between two profiles then only one bit of PROF port is needed.

3. Experimental tests

3.1. Test setup

The TIG was examined in a test setup shown in Fig. 4. The generator was placed in a climatic chamber PL-2J (*ESPEC*). The short TIs between START and STOP pulses ($\leq$ 10 μs) were measured using a DSA90804A oscilloscope (*Keysight*) [25] and the longer ones with the use of a newly developed precise time interval counter with a precision even as low as 3 ps [26]. Both the TIG and the counter were driven by two separate rubidium generators FS725 (*Stanford Research Systems*).

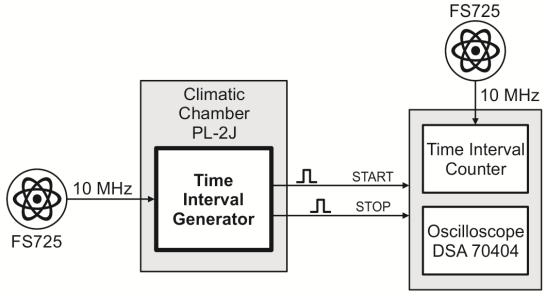

Fig. 4. A test setup for TIG.

3.2. In-period TIG evaluation

Since the TIG performance is largely dependent on the DDS synthesizer, much work was devoted to precisely examine its features regarding phase shifting. We tested the transfer function and time jitter of TIs generated for all POW values. The research was done using a high performance oscilloscope that calculated mean value and standard deviation of TIs based on 1000 samples. Each measurement of the TI length and jitter lasted about 6 seconds. The obtained results for sine and cosine signals are presented in Fig. 5.

In both cases, a cyclic increase of the jitter value is observed. Looking carefully into the conversion characteristic it can be seen that the obtained phase shift step is smaller (the slope of blue line) in the same POW ranges where lower values of timing jitter occur. This feature may result from the process of counting samples in the DDS synthesizer.

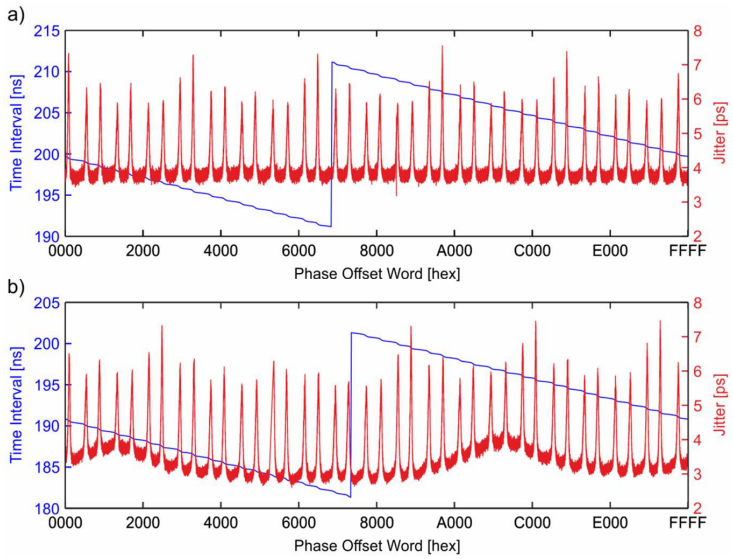

Fig. 5. The length of TI and its jitter within a single period of the main clock for a sine (a) and cosine signal (b).

Unequal length changes of the generated TIs for successive POW values (blue line, Fig. 5) lead to relatively high nonlinearities of conversion. It is common to define nonlinearities using two parameters, *i.e.* differential and integral nonlinearity (denoted by DNL and INL, respectively). The first one describes a difference between the actual size of the *i*-th phase shift step (q_i) and the mean step size (q_m, denoted also as the value of least significant bit LSB). It is expressed as:

$$\mathrm{DNL}_i[\mathrm{LSB}] = \frac{q_i}{q_m} - 1, \tag{1}$$

where the mean step size q_m is calculated as a conversion characteristic range (T_R) divided by the number of steps (M). The second parameter (INL) defines how much the actual conversion characteristic differs from the ideal one in the *i*-th phase shift step. The corresponding equation is as follows:

$$\mathrm{INL}_j = \sum_{i=1}^{j} \mathrm{DNL}_i, \tag{2}$$

where $1 \le j \le M$.

Regarding the designed TIG q_m (denoted as LSB) is equal to 305 fs ($T_R = T_0 = 20$ ns, $M = 2^{16} = 65536$). After reordering TI values, obtained for all POWs, in the increasing order and after calculating differences between the neighbouring values we obtain the actual step sizes q_i. The TIG nonlinearity, evaluated using (1) and (2), is presented in Fig. 6 as bar graphs of DNL and INL values. The maximum DNL is equal to about 31 LSB, which corresponds to 9.5 ps, while the extreme value of INL is 714 LSB, *i.e.* 218 ps.

For most POW values the time interval jitter is below 4 ps, while peaks can reach even 7.5 ps. The characteristics of sine and cosine signals are slightly different. The cyclic growths of time jitter for both signals partly overlap. Therefore, the jitter cannot by minimized by dynamic switching between the sine and cosine types of output signal.

Experimental tests to obtain all possible values of POW ($2^{16} = 65536$) for measurements of both sine and cosine signals lasted about 9 days. To check the reproducibility of measurement results the test was repeated. Fig. 7 shows the difference between the jitter values and the time

Metrol. Meas. Syst., Vol. 24 (2017), No. 1, pp. 57–68.

interval lengths obtained in the first and the second tests for a sine signal. The time interval jitter in both series is within a range from –0.94 ps to 0.75 ps, while the length of generated TIs varies within a range from –9.59 ps to 21.14 ps. Assuming no temperature influence (the tested generator was placed in a climatic chamber that stabilized temperature at 21°C), the obtained slight differences are caused mainly by: (1) the stability of the reference 10 MHz clock signal, (2) the stability of the DSPLL synthesizer 1 GHz output signal, and (3) the quality of the main clock produced by the DDS synthesizer with dynamic phase shifting.

A common problem with integrated circuits is their vulnerability to PVT variation. The process variation is related to a method of CMOS chip fabrication [9]. Thus, some differences in performance of chips are acceptable. However, the use of digital techniques such as DSPLL and DDS makes the presented TIG resistant, to some extent, to the process variation. As a proof, we have tested the second TIG device and obtained very similar results as in Fig. 7. The environmental (power supply voltage and temperature) conditions can vary in time and space resulting in changes of the generated TI length and in the increased jitter [9]. The influence of voltage variation is limited in the designed TIG by applying multi-stage voltage stabilization using ultra low-noise low-dropout regulators, while the impact of temperature variation is discussed further in the paper (Subsection 3.3).

Due to inability to eliminate the cyclic growth of the time jitter of generated TIs we decided to reduce the TIG resolution to 0.5 ns. This enables to arbitrarily choose the phase shift values for which the time jitter of generated TIs does not exceed 4 ps (Fig. 8a). With such a limited resolution the INL error of the designed TIG reaches very low values with the extreme one equal to |–0.0013| LSB = 0.65 ps (Fig. 8b).

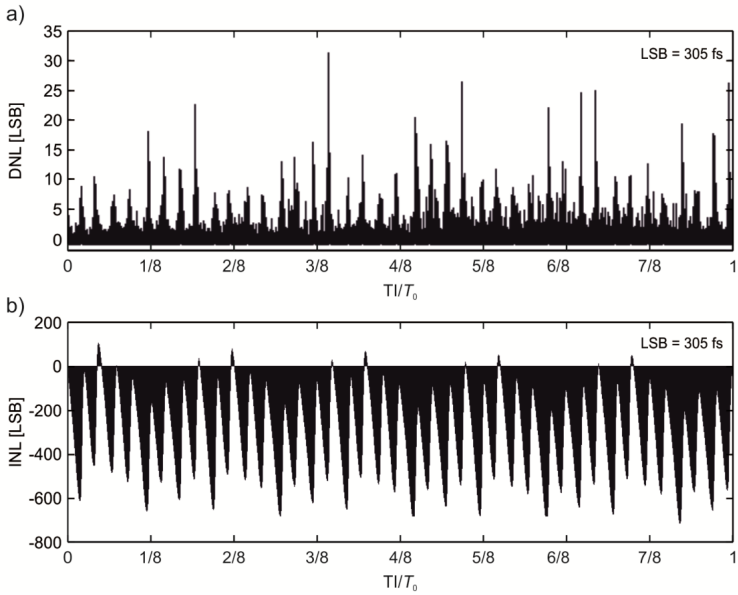

Fig. 6. The DNL (a) and INL (b) plots of the TIG with LSB = 305 fs.

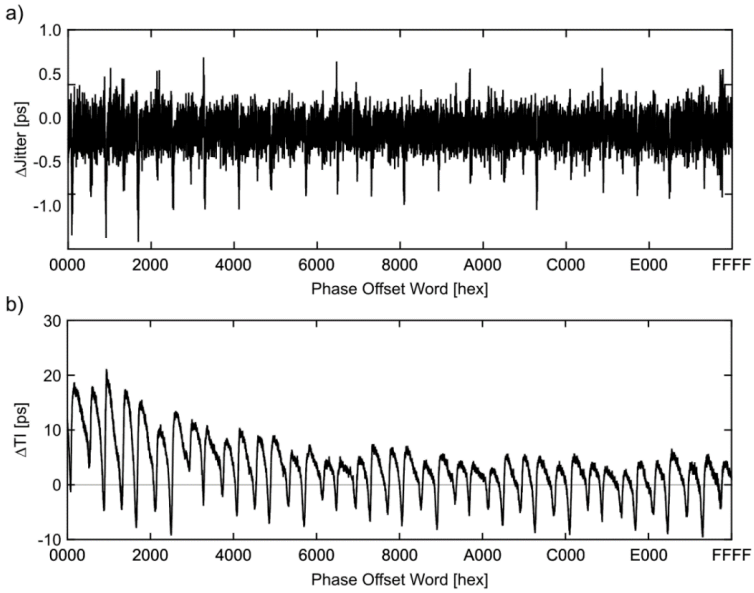

Fig. 7. Differences of jitter (a) and lengths of TI (b) for two independent series of measurements for a sine signal.

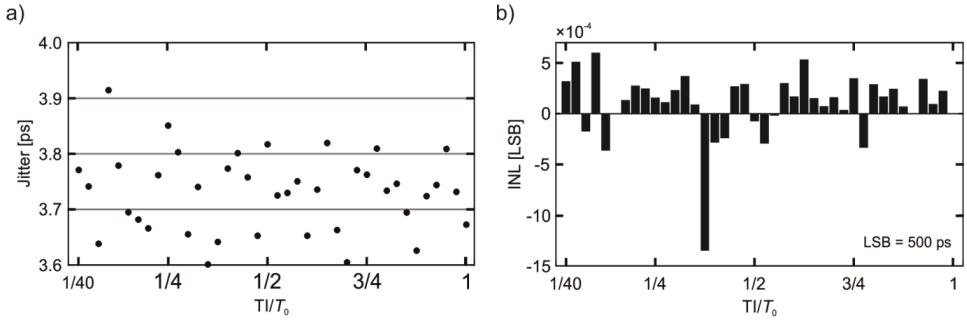

Fig. 8. The time interval jitter (a) and INL plot (b) of the TIG within the range of a single T_0 and resolution of 500 ps.

3.3. Wide range TIG evaluation

In the next test the temperature inside the thermal chamber was stable (21°C) and measurements of the time interval jitter were performed for different TI lengths. As a reference clock we used either the internal built-in OCXO or an external rubidium generator. The results are shown in Fig. 9. The most precise measurements are done with the use of an oscilloscope. Thus, in a range of up to 10 μs the time jitter values are below 5 ps. The time interval counter has a greater intrinsic standard measurement uncertainty than the oscilloscope, so that the obtained jitter is a bit higher. The short-term stability of the reference clock becomes a critical parameter for generated TIs exceeding 20 ms. A more stable clock (*i.e.* a rubidium generator) enables to keep the jitter below 10 ps within a range of up to 50 ms.

Metrol. Meas. Syst., Vol. 24 (2017), No. 1, pp. 57–68.

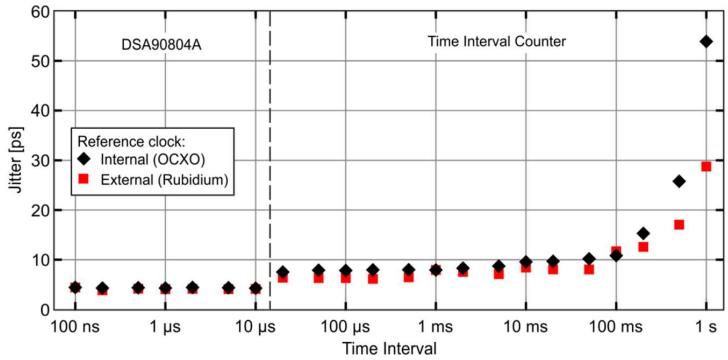

Fig. 9. The time interval jitter of generated TIs.

3.4. Temperature tests

During the thermal tests the TI length was arbitrarily selected as 14,500 µs and the ambient temperature varied from −10°C up to +60°C. The measured value of TI length was changed less than 20 ps with regard to the value obtained at 20°C (Fig. 10). So the ambient temperature changes have a little influence on the TIG accuracy. Also the time interval jitter changes slightly, *i.e.* less than 0.8 ps. Contrary to Fig. 10a, there is no visible trend in Fig. 10b. It can be concluded that the obtained differences come from the noise floor of the oscilloscope input circuits [25]. Therefore, temperature changes do not affect the TIG precision.

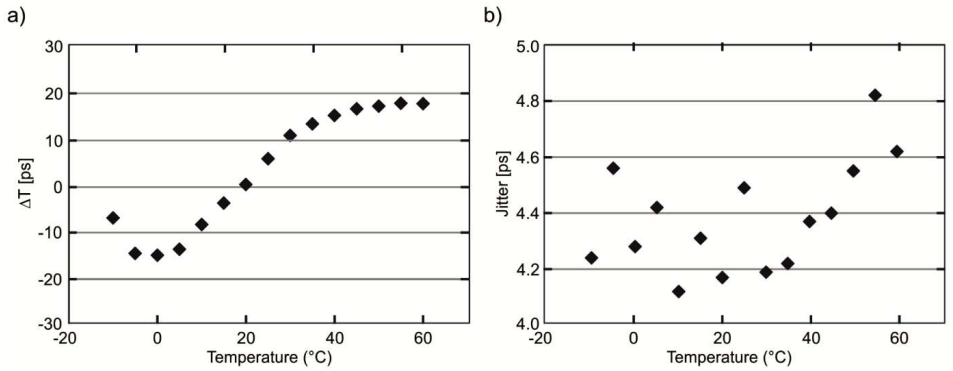

Fig. 10. The temperature dependence of the length of generated TIs (a) and the time interval jitter (b).

3.5. Frequency test

In the last experiment we checked the frequency mode of the TIG. A square wave signal of a selected frequency was measured using an SR620 counter (*Stanford Research Systems*) driven by an external FS725 reference clock generator. Fig. 11 shows the example results of detuning for a frequency range from 10 Hz to 50 MHz. The detuning values may result from the volatility of the build-in OCXO reference signal source. Because the values of detuning are linearly dependent on the selected frequency, they can be easily compensated.

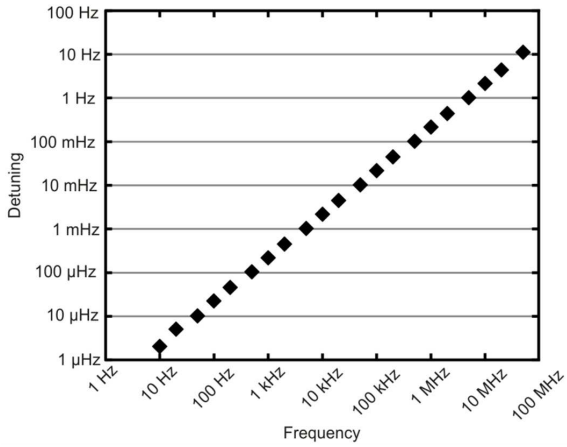

Fig. 11. The detuning for a frequency range from 10 Hz to 50 MHz.

Using a precise time interval counter the *Allan deviation* (ADEV) value of generated signal of 10 MHz frequency was evaluated. The obtained results are summarized below:
ADEV 0.1 s – 1.74×10^{-9}, 1 s – 2.42×10^{-10}, 10 s – 5.10×10^{-11}.

4. Conclusions

The designed generator produces time intervals with the time interval jitter less than 5 ps and the resolution of 500 ps. A low jitter is achieved thanks to the use of an ultra-low jitter synthesizer device. Selected DDS synthesizer features restrict the possibility of obtaining the time interval jitter below 5 ps together with a sub-picosecond resolution. The use of digital methods for generating time intervals makes the generator resistant to PVT variations. The generator can also produce a frequency signal of high stability (*e.g.* ADEV(1 s)= 2.42×10^{-10}).

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