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Ultra-low Power FinFET SRAM Cell with Improved Stability Suitable for Low Power Applications

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***Abstract*—In this paper, a new 11T SRAM cell using FinFET technology has been proposed, the basic component of the cell is the 6T SRAM cell with 4 NMOS access transistors to improve the stability and also makes it a dual port memory cell. The proposed cell uses a header scheme in which one extra PMOS transistor is used which is biased at different voltages to improve the read and write stability thus, helps in reducing the leakage power and active power. The cell shows improvement in RSNM (Read Static Noise Margin) with LP8T by 2.39x at sub-threshold voltage 2.68x with D6T SRAM cell, 5.5x with TG8T. The WSNM (Write Static Noise Margin) and HM (Hold Margin) of the SRAM cell at 0.9V is 306mV and 384mV. At sub-threshold operation also it shows improvement. The Leakage power reduced by 0.125x with LP8T, 0.022x with D6T SRAM cell, TG8T and SE8T. Also, impact of process variation on cell stability is discussed.**

***Keywords*—FinFET, RSNM, WSNM, Hold Margin, Sub-threshold, Leakage Power**

I. Introduction

THE remarkable growth in the semiconductor industry has been seen over the few decades. As, per the ITRS (International Technology Roadmap for Semiconductor, the gate length has been predicted to be 4-5nm by 2023. World has witness that CMOS scaling feature has revolutionize the semiconductor industry in few years. Moore′s Law which predicted that transistor count will be double in 18 months has also been overtaken by More than Moore (MTM) rule. Accodring to ITRS 2009 [1] glossary MTM says that incorporation into services of functions that do not necessarily scale according to Moore law but provide additional value in different ways. Major area of a die is consumed in memory components. Almost 60-70% of chip area is being consumed by "Memory Circuits". The dominant memory in this market is SRAM even though the SRAM size is larger than embedded DRAM,as, SRAM does not have yield issues and cost is not high as compared to DRAM. At the same time, the other attractive feature for the SRAM is speed and it can be used for low power applications. CMOS SRAM are the crucial component in microprocessor chips and applications and as said major portion of the area is dedicated to SRAM arrays so, CMOS SRAM is considered to be the stack holders in memory market. Since, due to the scaling feature of CMOS, SRAM was it having its hold in the market over the last few decades. In the recent years the limitations of the CMOS scaling has raised so many issues like short channel effects, threshold voltage variations. The increased thrust for an alternative devices leads to FinFET. FinFET is emerging as one of the suitable alternative for CMOS and in the region of memory circuits. It became a promising device and in some factors superior choice over conventional MOSFETs because of the property of the low leakage reduction and smaller in size. The reason for the superiority over the CMOS are : it has excellent gate control over the channel which in turn reduces the source/drain leakage current, it also reduces the Short Channel Effects. FinFET is a multi-gate transistor and so because of the several gates acting on the channel, it has excellent electrostatic properties. Over and above the beauty of MOSFET device "Scaling" is also existing in FinFET [2].

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II. Review Work

A. FinFET Technology

The consistent effort to increase current, better control over the Short Channel Effects (SCE multi-gate devices have been evolved from single gate devices. "DELTA" was the first modern self-aligned vertical multi-gate MOSFET. The DELTA MOSFET has two gates front and back which are inherently self-aligned and the channels are on the side wall of the body. Since, DELTA was having great compatibility with conventional CMOS so, FinFET and other Multi-gate structures has come into picture. Since, shrinkage of the gate length has led to Short Channel Effects (SCE) which are: increase in sub-threshold, Variation in threshold voltage, punch through between drain and source [3]. To reduce these variations, researchers have proposed solutions to reduce the gate oxide thickness and channel doping concentration should be increased .But capacitance of gate to channel increases, due to reduction in oxide thickness and there is a reduction of charge sharing between source and drain and increases GIDL. So, then the other approach of controlling the SCE, is to have two or more gate electrode and a thin fully depleted semiconductor body. The vital parameter is the thickness of the thin body which is Fin width in multi-gate transistors. This was the main idea behind the FinFET structure as to keep this body very thin such that there is no leakage path from the gate and gate can have good control. Silicon on Insulator or bulk silicon is used for FinFETs. The 3D structure of FinFET consists of thin body known as Fins .The channel is covered by the gate from the three sides which gives excellence to the gate. The channel is vertical in FinFET so the width of the device is determined by the height of the Fin. The current can be increased by increasing the width of the device or by increasing the number of Fins. The FinFETs are broadly classified as two types DG (Double Gate) FinFET in which

both the gates are biased together to turn on/off the devices while the another one is BG(Back Gate) mode in which the two gates are biased independently, One gate voltage is used for switching the device while the other is used to change the threshold voltage of the device. The double gate FinFET has two gates back and front which are electrically coupled to reduce the SCEs effect by reducing the sub-threshold slope and DIBL. These type of FinFET are more appropriate for low power applications as they can significantly contribute in reduction of standby power dissipation and leakage power [4]. Since, for many years CMOS was one of the single choice for SRAM memories, after FinFET came into existence because if its beauty of scaling and low leakage, FinFET started replacing the CMOS.Various SRAM cells have been proposed by the researchers in last few years with FinFET. Most of sub20nm technology concerns can be overcome by the FinFET devices. As discussed, the thin body of the FinFET suppresses much of the SCEs, threshold variations and impurity scattering reduces the depletion charge and capacitance which in turn reduces the leakage as the sub-threshold slope reduces.

B. SRAM Cell

In [5] the 6T SRAM proposed used a common a common back-gate bias to improve the read performance, read margin, write delay. The cell uses a reverse bias to reduce the leakage. Since, the cell nodes are not disturbed by the read current in the 8T cell, read stability is the same as hold stability, in the read mode, the drain current increases with an increasing back-gate voltage. Thus, the Read performance is improved. To reduce the leakage current during the standby mode the back-gate voltage is switched to a negative voltage or zero voltage. To optimize read/write margins for stable SRAM operation, one would like to have a higher supply voltage during the read operation to maintain an adequate noise margin, and lower supply voltage during the write operation to facilitate writing [6]. In [7] FinFET 8T-Decoupled SRAM has been proposed where an and gate is used which completely removes half select stability problems because of the word line which remain ON of an unselected cell. The authors improved the cell stability without affecting the performance of the design. A 6T-Decoupled SRAM cell has been proposed in [7] which works good for low voltage and half select column also. 8T SRAM in [8] proposed for low power and improved stability. In [9] for enhanced stability SRAM using FinFET with dynamic gate voltage adjustment has been proposed SRAM cell with pass gate feedback has been proposed in [10]. Another SRAM cell with pass p-type access transistor has been discussed in [11]. 8T FinFET SRAM cell has been with enhanced read and write margin 8T SRAM cell reported in [12]. Sub-threshold FinFET SRAM has been proposed for low power applications in [13]. Robust 6T SRAM cell using FinFET has been discussed and proposed in [14]]. Due to the impact of process variations and varying supply voltages in 6T Conventional SRAM using FinFET as shown in Fig.2 it is very difficult maintain both the operation ,Which results majorly in read failure [15].In [16] [17] [18] [19] [20] the Read and write assist circuit has been discussed which helps in reducing the functional failures

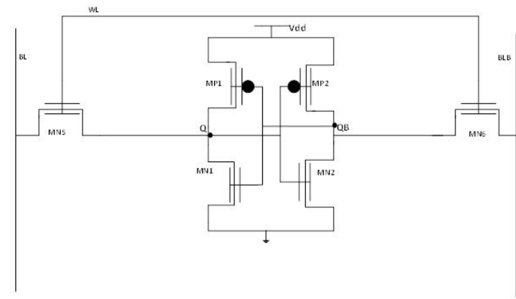

Fig. 1. Conventional 6T SRAM Cell with FinFET.

during read and write operations. Though, the disadvantages are larger delay, area additional circuitry for voltage source to control the voltage level of word-line or bit-line [16]. A number of new single port and multiple port SRAM bit-cell configurations are being suggested by the researchers for low operating voltages, high stability and for robust operations.

In [21] a dierential 8T SRAM-NEW for improved read data stability and higher write ability is discussed. They have used two p-type access transistors which are connected and controlled by additional read word line (RWL) for separating the SRAM cell to form separate read path. The Schmitt trigger (ST) conguration in [22] makes the inverter pair of 10T ST proposed improvement in SRAM but, leads to low SNM with larger read delay. The 10T SRAM cell discussed in [23], however, compensates the read-disturbance problem of [22] as, it has separate read and write ports for read and write which is responsible for decoupling the storage nodes from the bit lines during read operation. This conguration has extra signal VGND (virtual ground) in the read path to reduce bit line leakage. In 10T P-P-N SRAM cell [24] attains the equal RSNM and HSNM as the bit-lines are isolated during read operation from the real storage node through pseudo storage node. 10T P-PN bit-cell also uses the same extra signal VGND in order to reduce the bit line leakage in read path. Another 10T SRAM as shown in Fig.2 has been proposed in [25] for near-threshold having high read and write margins, this paper also has extra virtual ground for improving the stability. The cell works well for super-threshold and near-threshold but the active power was high. A fully differential DTMOS (dynamic threshold MOS) technique based 10T SRAM and another SRAM with CCBB (cell content body bias) 10T SRAM for ultra low power operations and high speed operations using CMOS has been proposed in [26]. In this appear a 11T SRAM has been proposed for low power applications.

III. Proposed 11T FinFET SRAM Cell

A. Proposed Work

The proposed architecture is 11T SRAM having different ports for read and write as shown in Fig.3. The cell is originally a 6T SRAM. This cell has separate port for read and has two read lines (RL). The two access transistors of the 6T SRAM is connected with the bit lines (BL and BLB) and word line (WL) similar to conventional 6T SRAM cell. The pass transistors MN5 and MN6 remain on during the write

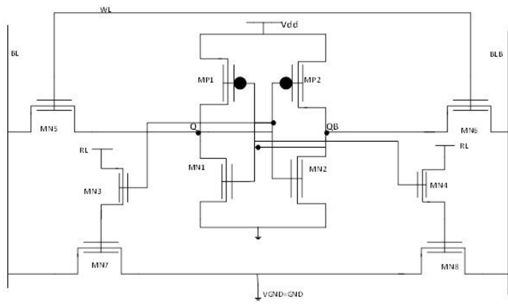

Fig. 2. 10T FinFET SRAM Cell.

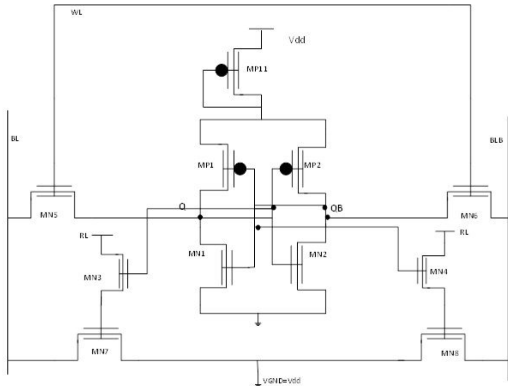

Fig. 3. Proposed 11T FinFET SRAM Cell.

operations as, WL remains high. The bit line value depends on the data to be written in the cell. The others transistors MN3 and MN4 are the switching transistors which are being controlled by the value of Q and QB. MN7 and MN8 basically the pass transistors which will get on during read operation. These two transistors are to be connected to ground mode in read operation and to Vdd during the other two operation of hold and write mode such that bit line leakage current from the read path can be controlled.

In this scheme, by changing the back gate bias voltage of the header transistor MP11, the supply voltage can be varied during read and write operations. During the read operation, the lower gate bias voltage can improve the read margin and during the write operation the higher back gate bias voltage will improve the write margin. During hold mode, lower supply voltage is needed to control leakage. The advantage of this scheme over the conventional dynamic supply voltage is, complexity and hardware increased, as, it requires the external two power supplies or voltage regulator or generators to arrange for the extra supply level and routing of the two supply voltage lines is also required. [21]. In context to the above mentioned scheme, here, routing is needed for the virtual supply voltage line. As discussed, in [21] the header scheme needs only one header diode while the conventional uses two pass transistors, also, in the conventional scheme the drain of the pass transistors are directly connected to the supply voltages due to which, most of the charge is required in charging and discharging of the voltage rail capacitance. While, the scheme used in this paper, has virtual supply control

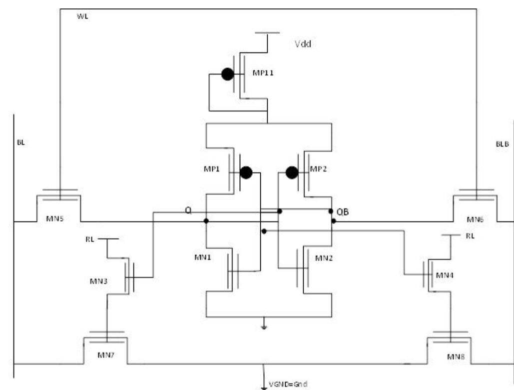

Fig. 4. Proposed 11T FinFET SRAM Cell: Read Operation

line used to charge and discharge the back-gate capacitance, and the front gate current is used to charge or discharged the voltage rails. Consequently, in the header scheme the settling time of the virtual supply is smaller.

B. Working of the Proposed SRAM Cell

1) Write Operation: As mentioned, the proposed cell is a dual port memory cell, so during write operation WL is enabled and RL is disabled, Fig.3 shows the values of each input during the write operation. If, we assume that initial some data is written, lets assume Q to be "0 and in this node if "1" needs to be written we need to enable BL to its high value and BLB to "0". The node which was holding a logic "1" can now be discharged through access transistor MN6 and through MN2 and the node which was holding a value Q can now be charged to Vdd through MN5 and MP1 as MN1 will no longer be "on", to discharge the node. During write operation, the back gate of the PMOS transistor is kept at high voltage to improve the write margin and the virtual ground is kept at Vdd. The MP11 transistor back gate voltage is also kept at high voltage to improve the write stability.

2) Read Operation: During read operation the RL is enabled and the word line is disabled both the bit lines are pre-charged to supply voltage as shown in Fig.4. During read operation the virtual ground is discharged to ground. The Fig.4 shows the circuit during the read operation, since the data stored at Q is at logic "0" and WL is at logic 0 both the pass transistors are off. The transistor MN4 is off which results in switching off the MN8. So, BLB cannot discharge through this path but BL discharges through MN3 and MN7. The back gate bias voltage of transistor MP11 is kept at low voltage which will help in improving the read stability.

3) Hold Operation: As discussed, in the write operation section the hold operation also has the same connections and voltage levels for transistor MP11 where its back gate bias voltage is kept at high voltage, the virtual ground is pulled up to supply voltage. The hold operation is the ideal state of the cell where the word line and the bit lines are disabled and the bit lines are pre-charged to Vdd. The reason behind keeping the virtual ground at Vdd is to turn off the potential leakage path of the bit lines to virtual ground which will improve

the leakage power of the SRAM. The proposed SRAM cell has the important feature of the header transistor which helps in improving the power and stability of the cell. The virtual ground node and the four access transistors, also, helps in improving the performance of the cell, as discussed, in the previous sections.

TABLE I
TECHNOLOGY PARAMETERS.

Parameters	Value for 20nm	Value for 16nm
Supply Voltage	0.9V	0.85V
Channel Length(Lg)	24nm	20nm
Fin Thickness(tsi)	28nm	26nm
Fin Height(Hfin)	20nm	12nm
Equivalent Oxide Thickness(EOT)	0.84nm	0.68nm

IV. SIMULATION RESULTS

The projected bit cell is simulated using HSPICE with 20nm FinFET and 16nm technology at room temperature with typical process corners. The PTM-MG model for FinFET is used to calculate and access the various performance parameters. The cell has been simulated for above threshold voltage and sub-threshold voltages.The technology parameters are different for 20nm and 16nm which are being used to simulate the 11T SRAM cell is shown in TableI. The proposed cell is having 11 transistors and each PMOS transistor is considered with 1 Fin and the access transistors MN5 and MN6 are with 2 Fins. The cell has been simulated from 0.9V to 0.1V to evaluate the performance of during the super-threshold and sub-threshold. If, the cell shows a good performance it can be used in the high performance constrained application,if, it shows better performance in sub-threshold region it can be considered for low power applications.

V. RESULTS AND DISCUSSION

As discussed, in the above sections the proposed 11T SRAM FinFET because of its low voltage operation makes it suitable for low power applications. But FinFET is still not mature as CMOS technology so many issues needs to be taken care especially,the failures during read and write operation and stability parameters. Read operation, read stability and active read power are some of the common issues which need to be taken care in each SRAM. Hence, the paper has emphasized on the evaluation of performance of the SRAM cell for different performance metrics like read and write stability in normal conditions and with process variation conditions, Standby power and active power and delay of the cell has been accessed to judge the performance.

Since, the cell has three modes as discussed, each mode can define its own margin which reflects the stability of the cell in each mode section. In [27] it has been discussed that, Static Noise Margin is a common measure of the ability of the cell to retain the states, it is the minimum noise voltage present at each node of the cell required to flip the data. The conventional method to calculate the RSNM is butterfly curve using the VTC curve of the inverters. Here, to calculate the stability criteria, we have used the butterfly curve. RSNM has been found using butterfly curve. During read operation, both the bit lines are kept at the high voltage equal to Vdd and so, the storing nodes of conventional SRAM cell are not insulated from discharging path of the bit line and hence, may responsible to increase the voltage of the node storing ”0 which may cause flipping of the data. To enhance the read stability of this proposed bit-cell, the back gate bias voltage is kept at lower voltage also, the data storage node which is isolated from the bit line discharging path suppresses increases in voltage level during read ”0. The RSNM using butterfly curve during different supply voltages can be seen in Fig.5.

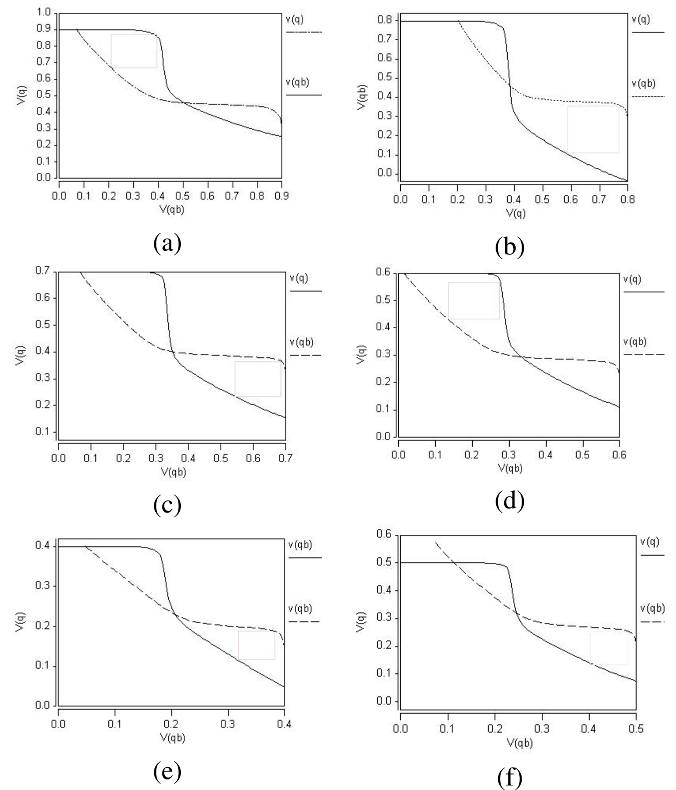

Fig. 5. Read SNM for the proposed Cell: (a) Vdd= 0.9V, (b) Vdd=0.8V, (c) Vdd= 0.7V, (d) Vdd=0.6V, (e) Vdd= 0.5V, (f) Vdd=0.4V

The RSNM at 0.9V is 213mV and at 0.4V is 67mV. The SNM for a bit cell with ideal VTCs is still limited Vdd/2 because of the two sides of the butterfly curve. An upper limit on the change in SNM with Vdd is 0.5V. As shown, in the above figures the Vtrip point is close to VDD/2. The RSNM using butterfly for various voltages is as shown in Fig. 6(a) at technology parameters of 20nm and 16nm. As, at higher temperature the threshold voltage of PMOS reduces more as compared to NMOS [28] so, it increases the Vtrip point of the inverter pair of the SRAM cell and thus the RSNM value increases at higher temperature. However, reduction in absolute value of threshold voltage at higher temperature reduces the RSNM. The temperature variation of RSNM is as shown in Fig. 6(b).

The read power or the active power is one of the important performance parameters which actually depends on the read current. The read power estimated for the cell at 20nm

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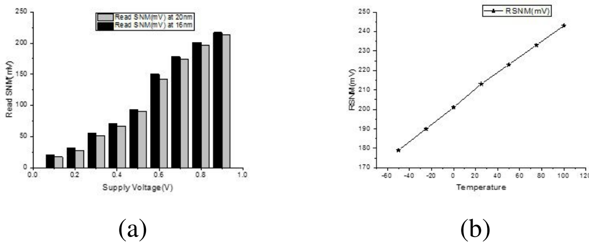
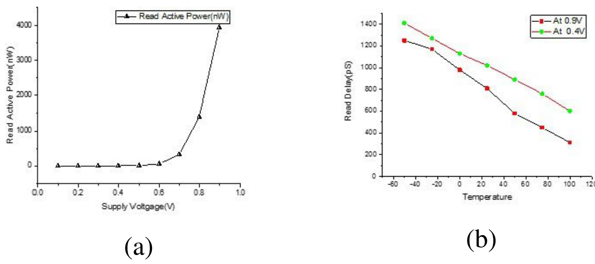


(a) (b)

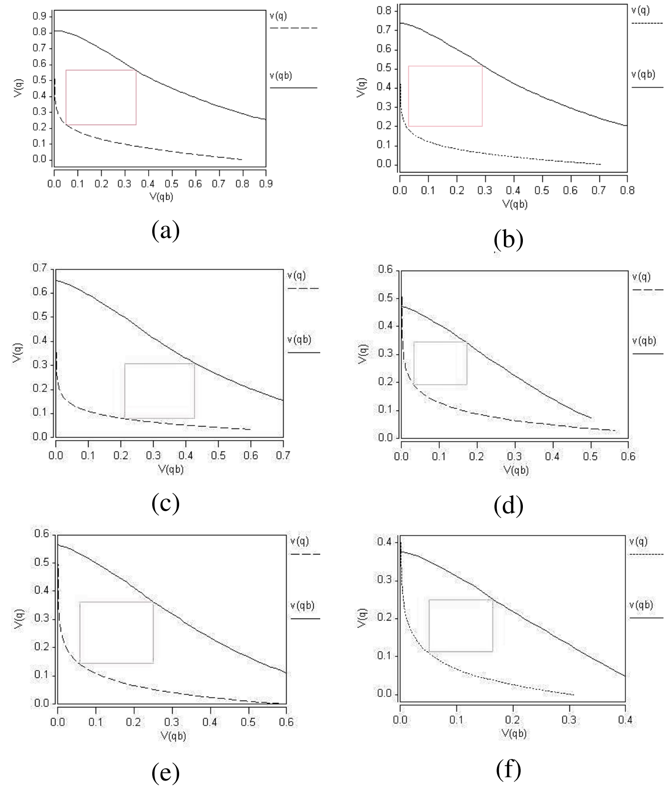
Fig. 6. (a RSNM variation with Supply Voltage, (b) RSNM variation with temperature



(a) (b)

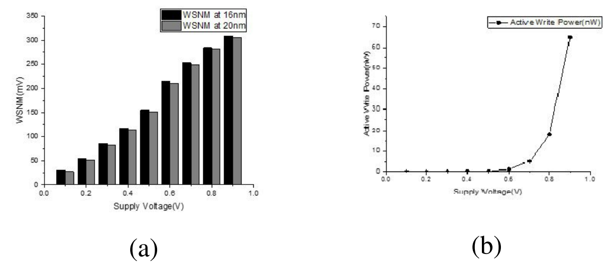
Fig. 7. (a) Read Active Power, (b) Read Delay Variation with temperature.

technology is as shown in Fig.7(a). The read power reduces drastically, due to the lower back gate bias which helps in reducing the read power as compared to other cell reported in [25]. During 0.9V, the read power is 3.95μW and during sub-threshold it is 1nW only. The read power is calculated at 16nm technology and observed for super-threshold voltage of 0.9V which is 3.74μW 0.813nW at the sub-threshold voltage of 0.4V. Access time is one of the important factors of judging the performances of the memory circuit. Here, in this paper, read delay has been evaluated to know the performance of the cell. Basically, read delay is defined as the time needed to develop a differential voltage (100mV) between the bit lines after 50% activation of reading signal [3]. It depends on read current value and number of transistors present in bit line discharging path. In this cell during the operation of read 0 there is only one access transistor path for bit line discharging. This helps in improving its read delay. Temperature is also one of the role players in manipulating the performance of the circuit, here the temperature is varied from 100^oC to -50^oC to observe the effect on the read delay. The effect has been observed at 0.9V and at the sub-threshold supply voltage of 0.4V. The delay at lower voltage has been increased [25]. There is larger variation with respect to variation in temperature. The larger fall in delay at higher temperature can be seen in Fig. 7(b). The important parameters to study the write operation are : write stability, write delay and write margin. Butterfly curve is used to find the WSNM of the proposed bit-cell when WL is kept high and RL is kept low. The values of the BL and BLB are oppositely determined according to the data to be written in the cell. Write delay is measured from 50% of the WL signal voltage level to the voltage level of the WL at which the cell flips to complete the write operation. Write margin (WM) is the voltage difference between the supply voltage and the minimum WL voltage that results in a successful write operation [29]. For determining WM of the cell, WL sweeps from zero to the voltage where the bit-cell completes the operation. As known, SRAM cell with larger WM shows easy write operation compared with the cell having smaller WM. WSNM has been calculated using butterfly curve at various supply voltages which is as shown in Fig.8. The WSNM at 0.9V is 306mV and at 0.4V is 115mV. The WSNM has been evaluated for both the technology parameters 20nm and 16nm. Fig.9 shows the WSNM at both the technology i.e. 20nm and 16nm. The WSNM for 16nm at 0.8V is 310mV and at 0.4V is 119mV.



(a) (b) (c) (d) (e) (f)

Fig. 8. Write SNM for the proposed Cell: (a) Vdd= 0.9V, (b) Vdd=0.8V (c) Vdd= 0.7V, (d) Vdd=0.6V, (e) Vdd= 0.5V, (f) Vdd=0.4V



(a) (b)

Fig. 9. (a)WSNM variation with Supply Voltage, (b)Write Power of the Cell

Like the read delay, write delay has been calculated in this paper. As, mentioned in [21] write delay is measured from 50% of the word line voltage level to the voltage level of the word line at which the cell flips for successful the write operation. The delay has been calculated at 0.9V and at the sub-threshold voltage with variation in temperature as shown in Fig. 10 and the curve verifies that one of the drawbacks of reducing the supply voltage is the increase in the delay.

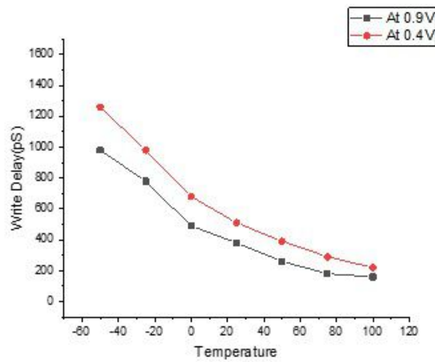
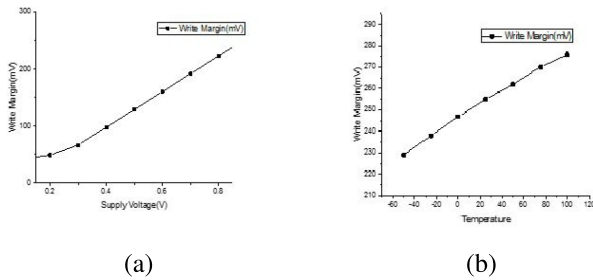
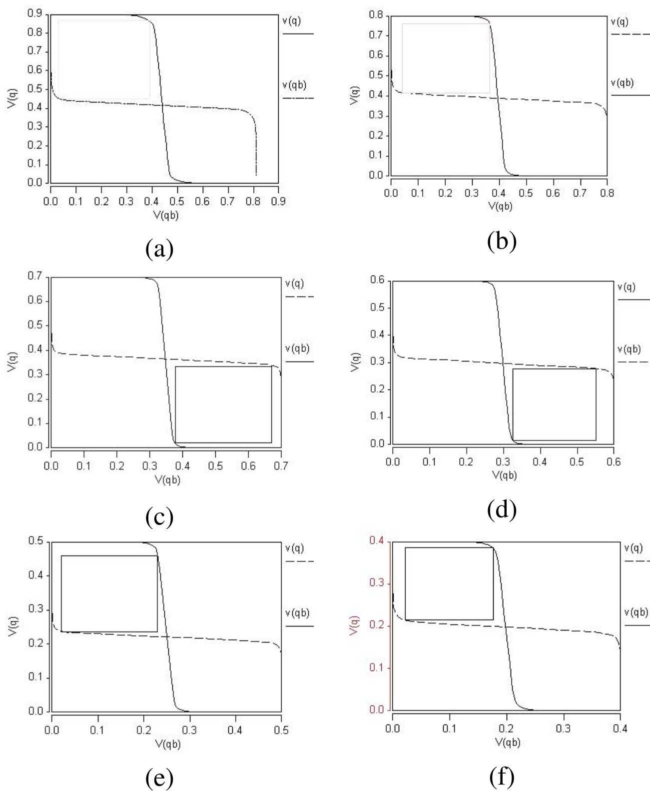


Fig. 10. Variation of the Write delay with temperature



(a) (b)

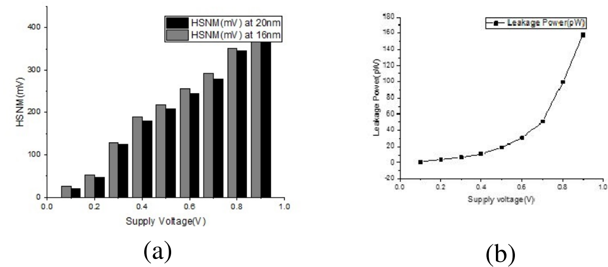
Fig. 11. (a) Variation of the Write Margin with supply voltage, (b) Variation of the Write Margin with temperature.



(a) (b) (c) (d) (e) (f)

Fig. 12. Hold SNM for the proposed Cell: (a) Vdd= 0.9V, (b) Vdd=0.8V (c) Vdd= 0.7V, (d) Vdd=0.6V, (e) Vdd= 0.5V, (f) Vdd=0.4V

As understood, cell with high WM exhibits easy write operation compared to the cell with smaller WM. The WM has been calculated at super-threshold and sub-threshold voltage, Fig.11 shows the variation of the WM with respect to the supply voltage and the variation of the temperature on the WM. The SRAM operates in the hold mode during the idle state. The Hold static Noise margin (HSNM) is found using Butterfly curve. HSNM has been found for voltage range from 0.9V to 0.1V at 20nm and 16nm technology respectively. In hold state, the cell does not read and write but stores the previous value. The parameters metrics calculated in this state are important, as the power dissipation here directly relates to leakage power dissipation of the cell. In this paper, the HSNM is moderately high than the write margin. The HSNM calculated for super-threshold (0.9V) is 384mV and at sub-threshold (0.4V) it is 181mV for 20nm technology as can be seen from the butterfly curves in Fig.12. The HSNM calculated for various voltages is shown in the following Fig.13(a) 20nm and 16nm technology. The PMOS and the stacking transistors



(a) (b)

Fig. 13. (a) HSNM at different technology nodes, (b) Leakage power

helps in reducing the static power dissipation. The hold power or the static power dissipation of the SRAM cell is as shown in the Fig.13(b). It is obvious from the figure that static power reduces at lower voltages. In the idle state, the virtual ground signal is kept at the high voltage equal to Vdd, which checks the possible leakage path from BL and BLB to ground and finally helps in reducing the power during hold mode and write mode. The static power dissipation for 20nm at 0.9V is 158pw and at 0.4V is 11pw. For 16nm the power at 0.9V is 153pW and at 0.4V is 8.8pW.

VI. Conclusion

In this paper, a new SRAM using header transistor scheme with LP mode of FinFET at 20nm and 16nm technology has been proposed. The cell has been analyzed at two technology nodes of 20nm and 16nm.The analysis of the cell has been done in the three modes read, write and hold. The cell has been simulated for super-threshold and sub-threshold voltage. The cell is compared with various SRAM cells reported in [25] for sub-threshold operation and it has shown better results in RSNM during sub-threshold operation. At 0.4V, the cell has 2.39x better than the LP8T SRAM cell, 2.68x with D6T SRAM cell, and 5.5x with TG8T. The WSNM has been also improved over TG8T SRAM cell by 1.33x and slightly reduced with LP8T SRAM i.e. with 0.95x. The leakage power drastically reduced by all the cell reported in [8], the power reduced by 0.125x with LP8T, 0.022x with D6T

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SRAM cell, TG8T, and SE8T. The cell well works for low power applications as the active read and write power is also improved drastically from the cell reported in [8]. The effect of temperature variation and the supply voltage on RSNM, WSNM, and HM has been analyzed for the cell at different voltages and temperatures. Read delay and write delay has also been calculated with respect to the temperature and supply voltages. Overall, the cell has better hold and write ability at super-threshold voltages and the good read and hold ability at sub threshold voltages. The cell is very much suitable for all the low power applications because of the header scheme used in this paper.

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