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Current-fed quasi-Z-source H7 inverter with reduced stress on SiC power devices

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Abstract. This paper discusses selected problems regarding a high-frequency improved current-fed quasi-Z-source inverter (iCFqZSI) designed and built with SiC power devices. At first, new, modified topology of the impedance network is presented. As the structure is derived from the series connection of two networks, the voltage stress across the SiC diodes and the inductors is reduced by a factor of two. Therefore, the SiC MOSFETs may be switched with frequencies above 100 kHz and volume and weight of the passive components is decreased. Furthermore, additional leg with two SiC MOSFETs working as a bidirectional switch is added to limit the current stress during the short-through states. In order to verify the performance of the proposed solution a 6 kVA laboratory model was designed to connect a 400 V DC source (battery) and a 3×400 V grid. According to presented simulations and experimental results high-frequency iCFqZSI is bidirectional – it may act as an inverter, but also as a rectifier. Performed measurements show correct operation at switching frequency of 100 kHz, high quality of the input and output waveforms is observed. The additional leg increases efficiency by up to 0.6% – peak value is 97.8%.

Key words: inverters, silicon carbide, power MOSFET, battery, energy storage.

1. Introduction

Current source inverter (CSI) topologies are very convenient when low voltage sources are connected with three-phase loads or a supply grid and several examples may be found in the literature [1–5]. Recent introduction of Silicon Carbide (SiC) technology has significant impact on CSI performance as passive components may be reduced with the increase of the switching frequency [6–13]. Unfortunately, when bidirectional power flow is required as in grid/battery systems (energy storage) standard CSI structures are problematic as three-phase bridge enables unidirectional current only. Some ideas to overcome this issue were proposed, for instance in [14], but the most promising solution might be a current-fed quasi-Z-source inverter (CFqZSI, see Fig. 1a) proposed in [15] and developed for motor drive applications with standard (Si) [17–23] and SiC devices [24]. Due to an unique impedance network, CFqZSI may operate in buck and boost modes and, moreover, enables bidirectional power flow [15, 17], [21]. In the regenerative/rectifier mode current from the impedance network (see i_{qz} in Fig. 1a) exceeds the current of the main bridge (i_{pn}) and the input current (i_{DC}) becomes negative. Thus, without a change of the input voltage polarity the energy flows also from the AC side to the DC side. The only problem is, in addition to a significant value of i_{qz}, very high voltage stress across elements of the impedance network. Especially adverse are the high voltage peaks across the diode D_Q. For instance, when the inverter is connected between a 400 V DC source and a 3×400 V RMS network this voltage reaches 1360 V. This problem was not studied in the literature before as most papers are related to motor drive applications and regenerative/rectifier mode operation was avoided or presented only for low voltages, mostly in simulations [17, 18, 24]. Nevertheless, such voltage makes rectifier mode operation questionable as a medium voltage diode is necessary in low voltage inverter. In response to this issue a current-fed quasi-Z-source inverter with improved impedance network (iCFqZSI) is discussed in this paper [25–26]. New circuit presented in Fig. 1b is derived from the series connection of two impedance networks and operation modes are similar to the standard version. The difference is that voltage stress on devices is reduced by a factor of two – this issue is discussed more precisely in the paper.

Even with new SiC power devices, on-state losses are major issue for all current-fed inverters, including the CFqZSI, due to four power devices included in the current path. Therefore, another suggested improvement of the standard topology is an additional, fourth leg composed of two SiC MOSFETs similarly to a conventional CSI [27]. An idea of the H7 bridge is to use this leg during short-through states to exclude the two SiC Schottky diodes with relatively high voltage drop from the current path.

Two major issues, mentioned above, related to the reduction of the voltage and current stress across elements of the high-frequency iCFqZSI are investigated in this paper. At first, in Sections 2–4, these problems are closer analyzed and, then, Section 5 shows a simulation study conducted in Saber. Next, Section 6 deals with a 6 kVA/100 kHz laboratory model based on SiC power devices and, finally, Section 7 provides a vital part – a series of experiments.

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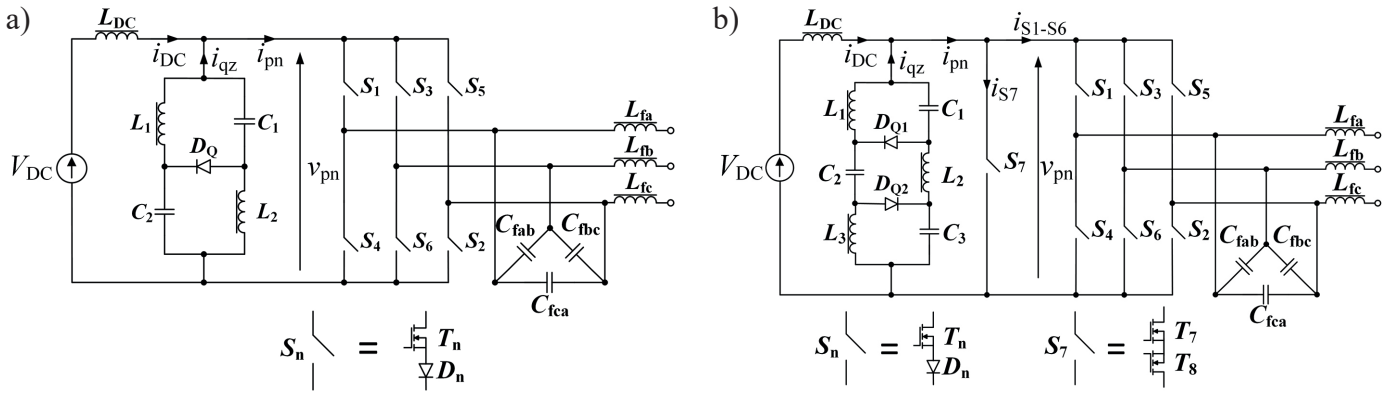


Fig. 1. Standard CFqZSI (a) and improved version iCFqZSI with the additional leg (H7 bridge) (b).

2. Improved impedance network with reduced voltage stress

Most features of the standard CFqZSI (Fig. 1a) and improved (Fig. 1b) inverter are the same, thus, this paper skips most operation principles, which may be found in the literature [15–24]. The main difference between the standard and the improved topology discussed in this paper is the structure of the impedance network. The standard one suffers from very high voltage stress across elements when the inverter enters the rectifier mode, especially during the active states (Fig. 2a). The voltage applied by the three-phase bridge (v_{pn}) is negative and maximum value V_{pnm} may be as high as the peak phase-to-phase voltage of the output filter. According to Fig. 2a, the inductor voltage v_L is a sum of the capacitor voltage V_C (equal to V_{DC}) and v_{pn}, which makes maximum blocking voltage of the diode D_Q:

$$V_{DQm} = V_{pnm} + 2V_{DC}. \tag{1}$$

Considering an example of the $V_{DC} = 400$ V and 3×400 V RMS at the AC output, V_{DQm} reaches 1360 V and even a diode rated at 1.7 kV is not sufficient.

Instead, a series-connection of two networks is proposed in the improved version of the CFqZSI [25, 26]. After simple transformation and reduction of the cells, as can be seen in Fig. 3, the novel network contains three inductors, three capacitors and two diodes. However, it has to be underlined that total capacitance and inductance are the same as in the standard network. Most operation principles are similar to the CFqZSI with one significant difference – the voltage stress of the most passive and active elements is reduced, especially, during the problematic active state in the rectifier mode (Fig. 2b). Now, the voltages across the inductors L_1 and L_3 are two times lower, which together with reduced voltage across C_1 and C_3 seriously limits the voltage across the diodes D_{Q1} and D_{Q2}:

$$V_{DQ1} = V_{DQ2} = \frac{V_{pnm}}{2} + V_{DC}. \tag{2}$$

This means that the diodes in the proposed circuit operating in the conditions mentioned above may be rated at 1.2 kV. On

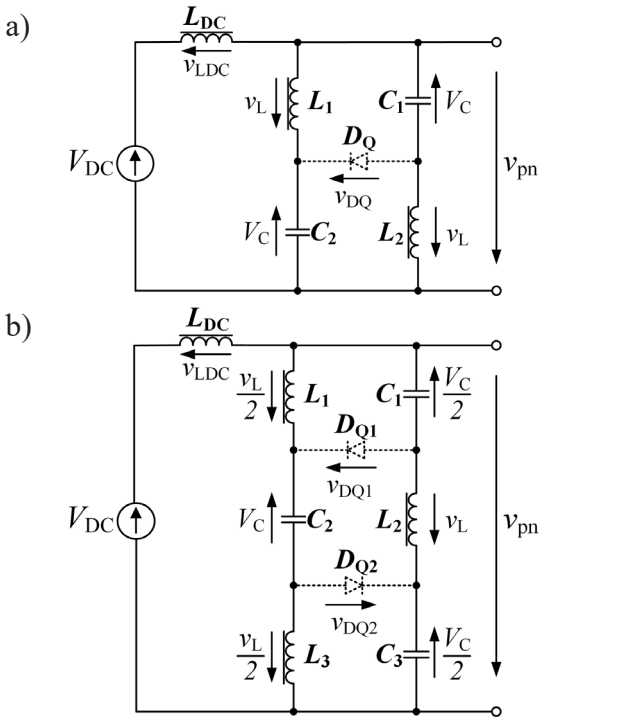


Fig. 2. Standard (a) and improved (b) impedance network during active state in rectifier mode.

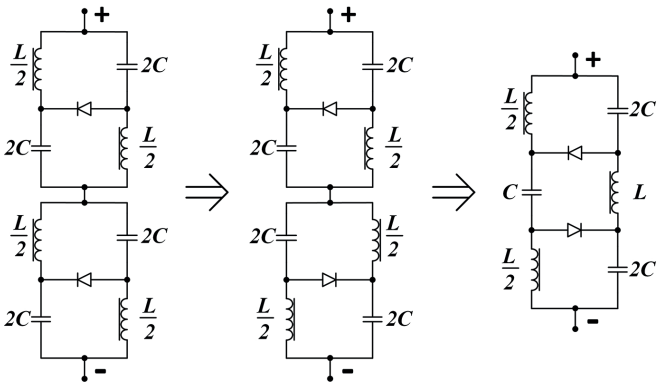


Fig. 3. Evolution of the two series-connected networks into improved network.

the other hand, operating conditions of the capacitor and the inductor in the middle cell (C_2 and L_2) are the same as in the standard network.

3. iCFqZSI: operation principles and PWM

The previous section deals mainly with the active state but two other types of the switching states are necessary to operate the iCFqZSI. Similarly to the CSI, six active states are available with two switches conducting, one from the upper and the lower arm, respectively. Then, in contrast to the CSI, an open-zero state may be introduced by breaking the current path in the bridge [15, 16]. However, the best solution is to open all switches to distribute the voltage stress (Fig. 4a) among the devices. In such conditions, there is no current at the output terminals of the three phase bridge as the current of the inductors L_1–L_3 is commutated to the diodes D_{Q1} and D_{Q2} and the capacitors C_1-C_3 are charged. This state enables the increase of the current from the impedance network i_{qz} to be higher than the bridge current i_{pn} (see Fig. 1b), which is a basic condition to change the direction of the input current i_{DC} and enter the rectifier mode. Note, that i_{pn} is not allowed to change sign due to the diodes in the current-fed bridge. In consequence, both CFqZSI and iCFqZSI are bidirectional but significant currents appears in the impedance

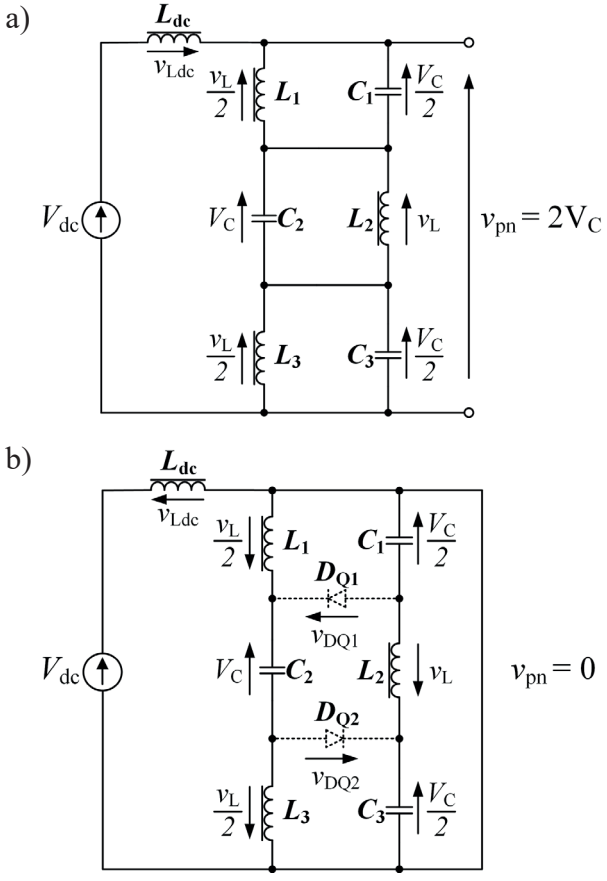


Fig. 4. Impedance network of the iCFqZSI in open-zero (a) and zero (b) state.

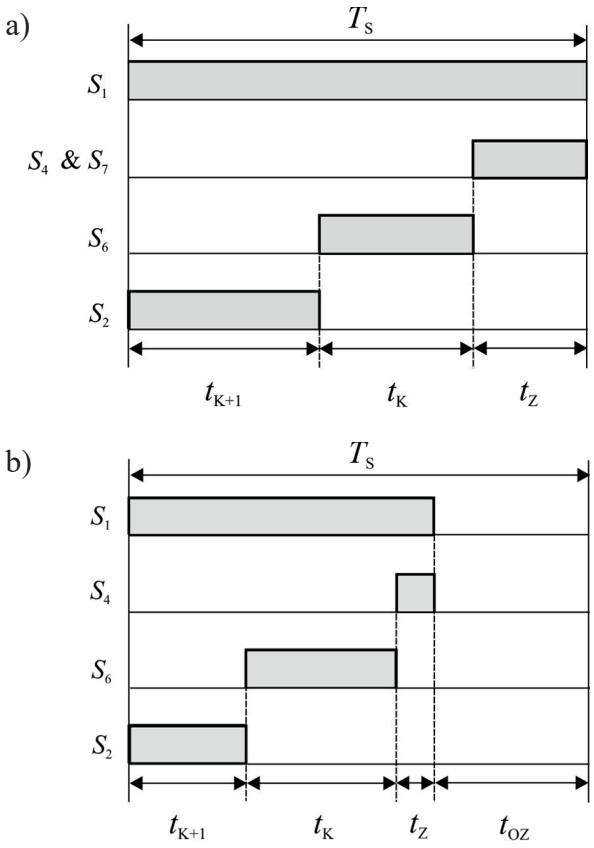


Fig. 5. The applied switching pattern in the inverter mode (a) and rectifier mode (b) – an example for the first sector.

networks during this mode. Finally, the zero state is performed by means of short circuit of the impedance network from the bridge side (Fig. 4b), which may be introduced by switching on the two transistors of the same phase-leg (three states available). Another possibility discussed in this paper is an additional, seventh switch introduced to perform short-through states only [27]. This solution will be discussed in the next section.

On the base of mentioned switching states various PWM were developed for the CFqZSI [22–23] and may be also applied for the improved version. As high-frequency operation of the SiC-based iCFqZSI is discussed in this paper, only very simple techniques based on space vectors are considered. When the iCFqZSI is expected to operate in the inverter mode, active and zero states are sufficient and a plain switching pattern with three states is applied – example for the first sector is presented in Fig. 5a. The switch S_1 is permanently in the on-state, while three other switches S_2, S_6 and S_4 are conducting alternately, the additional, seventh switch S_7 may be switched on during zero states. The same sequence is applied in following six sectors according to the SV PWM rules. When the iCFqZSI enters the rectifier mode, open-zero states with constant duration are required. Therefore, the switching pattern is changed by an addition of the open-zero state, after the regular zero state at the end of the switching period T_S (Fig. 5b). The main difference is that S_1 is turned off at the beginning of the open-zero state. Moreover, the time of the regular zero states t_Z is very short

and there is no point to use additional leg as switching losses exceeds the gain from the decrease of the conduction losses.

4. Reduction of the current stress with H7 bridge

A fundamental feature of the current-fed bridge is that all switches S_1–S_6 (Fig. 1b) must be able to conduct unidirectional current and block bidirectional voltage. A switch with such properties can be obtained through various configurations of semiconductor power devices [1–13], including reverse blocking IGBTs, but when high frequency operation is discussed SiC MOSFETs and Schottky diodes are the obvious choice. Therefore, a basic version of the switch contains series connection of these elements but two MOSFETs in common source configuration may also be considered. Benefits from the application of two MOSFETs in series can be observed in Fig. 6 where different switch scenarios, using common 80 mΩ and 40 mΩ SiC MOSFETs [28, 29] and Schottky diode [30] ($V_{T0} = 0.85$ V, $r_F = 43$ mΩ, $T_j = 25°C$) are compared by means of the simplified V-I characteristics. It can be observed that lower voltage drop, hence also lower conduction power losses, may be achieved with two transistors, especially two 40 mΩ devices show very good performance. On the other hand, switching of two MOSFETs always ends with higher loss than switching the MOSFET and Schottky pair. Moreover, switching losses of the 40 mΩ devices are more substantial in comparison to the 80 mΩ counterparts due to the increased chip area and higher parasitic capacitances. According to datasheets [28, 29] the switching energies of C2M0040120D are approximately between 8 and 15 percent higher than C2M0080120D for the same test conditions. Similar performance is expected for the devices from other manufacturers and, therefore, a gain from the lower on-state drop is slightly reduced by a switching loss difference. Looking for an optimal solution a H7 bridge should also be considered. Additional leg with seventh switch [27], which is applied during zero states, offer the possibility to reduce the on-state power losses.

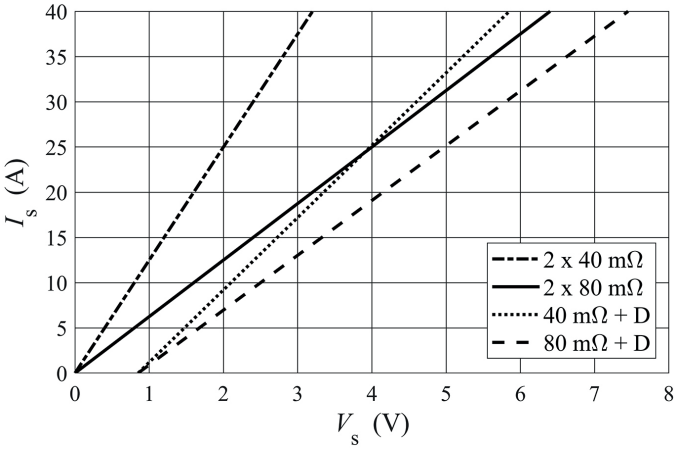


Fig. 6. VI-characteristics of the various switches: 2×40 mΩ MOSFETs, 2×80 mΩ MOSFETs, 40 mΩ MOSFET + Schottky, 80 mΩ MOSFET + Schottky ($Tj = 25°C$)

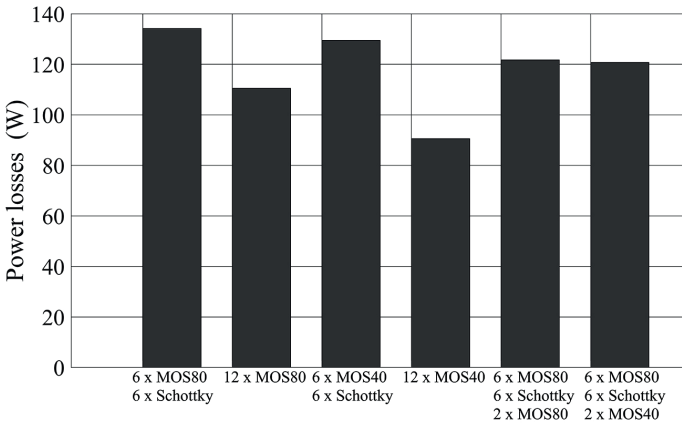


Fig. 7. Power losses for various switch scenarios at nominal conditions during inverter operation mode ($M = 0.8$).

On the base of the conducted simulations and data provided in [25], power losses for different switch scenarios were calculated. Results obtained for switches S_1–S_7 during inverter operation (output power 6 kVA, switching frequency 100 kHz and modulation index $M = 0.8$) are presented in Fig. 7. As expected, SiC MOSFETs in common source configuration as a single switch ensure the lowest losses (90.5 W with 12×40 mΩ SiC devices, 110.5 W with 12×80 mΩ devices). However, such a solution requires, in addition to six extra transistors, also extra gate circuits. The highest power losses were calculated for the three-leg bridge (SiC MOSFET + Schottky diode) – 134 W or almost 130 W for 80 mΩ or 40 mΩ devices, respectively. When the three-leg bridge with 6 80 mΩ transistors is equipped with the additional leg, almost the same loss is estimated – 122 W with 80 mΩ devices and 121 W with 40 mΩ transistors. Nevertheless, with lower modulation indexes (higher i_{pn} current) lower resistive transistors will ensure minor overall losses.

Another crucial factor is cost of power semiconductors and necessary gate drivers, especially, when the still expensive SiC technology is on the table. Fig. 8 illustrates cost of the

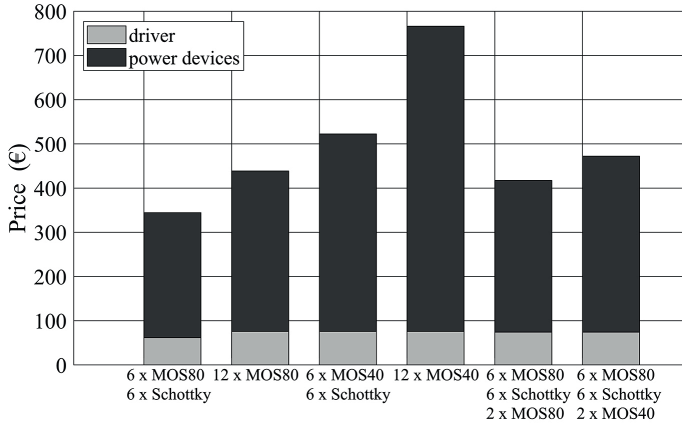


Fig. 8. Cost of various switch scenarios (prices from a common on-line distributor)

necessary devices using the same bridge configurations as in Fig. 7 (prices taken form from a common on-line distributor). Assuming as a basic scenario 6 switches with 80 mΩ MOSFETs and Schottky diodes, a change for 12 MOSFETs increase the power semiconductor cost by 27%. Using 6×C2M0040120D elevates the costs by more than 50%, while a complete bridge based on 12, 40 mΩ SiC MOSFETs is 122% more expensive. A scenarios with two extra transistors show similar costs to the bridge with twelve 80 mΩ MOSFETs. However, the performed loss analysis shows that the additional leg with two 40 mΩ transistors provides higher efficiency in a wide operating range. Thus, the switch S_7 with two 40 mΩ SiC MOSFETs in addition to a basic version of the bridge is recognized as a solution close to optimal from both performance and cost point of view.

Table 1
Parameters of the simulation model

Element	Value
AC output (*grid*)	3×400 V RMS, 50 Hz
V_{DC}	400 V
L_{DC}, L_2	700 µH
L_1, L_3	350 µH
C_1, C_3	4 µF
C_2	2 µF
L_f	3×100 µH
C_f	3×2 µF

5. Simulation study

A simulation model of the 6 kVA iCFqZSI was developed in Saber software to verify the proposed improvements of the discussed inverter and design a laboratory model. The model was operating in the open loop with modulation index $M = 0.8$ (inverter mode) and $M = 0.4$ (rectifier mode, duration of the open-zero states $D_{OZ} = 0.6$). The PWM patterns presented in Fig. 5 were applied in a DSP board to control all switches of the iCFqZSI, according to the space vector method. Switching frequency of 100 kHz was assumed and, in the first step, parameters of the passive components were determined for the inverter and rectifier mode – see Table 1 [25].

5.1. Voltage stress. The first studied problem was the performance of the impedance network during the rectifier mode. As it was mentioned before, a serious drawback of the standard CFqZSI is high voltage stress across the input diode D_Q and the inductors L_1, L_2, L_{DC}. This problem can be observed in Fig. 9a when the standard CFqZSI inverter is fed from a three-phase grid (3×400 V RMS) and the DC side voltage is 400 V. Waveforms of the inductor voltages show significant changes, especially when the inverter is switching from the open-zero to the active state. But the most severe is the problem of the diode D_Q – the peak voltage is measured to be 1385 V. This value is slightly above the level calculated from (1) due to ripples of the capacitor voltages. All in all, the simulation study confirms that medium voltage diode is required, another solution is to use two series connected 1.7 kV diodes.

In contrast to the standard CFqZSI, waveforms of the improved impedance network are presented in Fig. 9b. Operating conditions of the inductors L_2 and L_{DC} are similar but pulses of the voltage across inductors L_1, L_3 are two times lower. The main advantage is the reduction of the voltage across the diodes D_{Q1}, D_{Q2} (positive voltage bias in Fig. 9 corresponds to the arrows marked in Fig. 2). As was expected from the equation (2), the peak voltage measured during the active state is close to 692 V. Therefore, SiC Schottky diodes rated at 1.2 kV are suitable to be applied in the impedance network of the iCFqZSI.

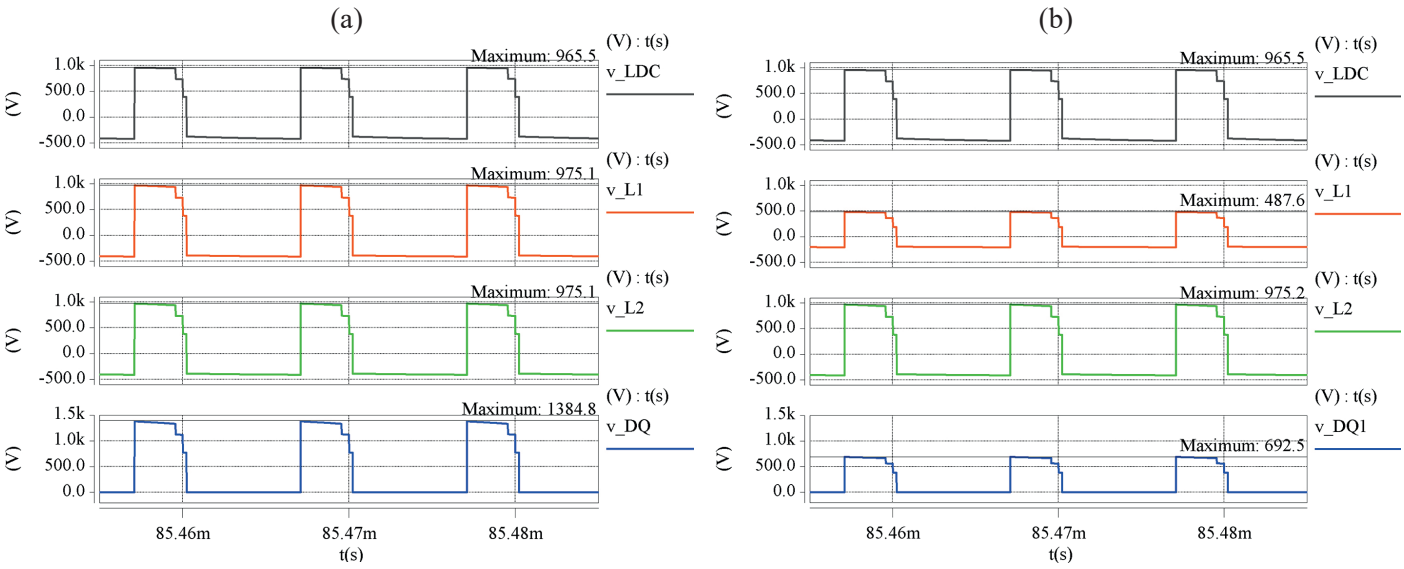


Fig. 9. Rectifier mode at 400 V/ 3 kVA: CFqZSI (a) vs. iCFqZSI (b), from the top: voltages across inductors, diodes.

5.2. Current stress. Another set of simulations in Saber was performed to verify the performance of the H7 bridge, especially the additional leg with two SiC MOSFETs. The inverter was supplied from a 400 V DC source and operating in open-loop ($M = 0.8$, $f_S = 100$ kHz). From Fig. 10 it could be observed that seventh switch is on only during zero states but takes all the current. In spite of the switched on transistors of the same leg (Fig. 5a), current from the three-phase bridge is equal to zero, which is due to very low voltage drop across two 40 mΩ SiC MOSFETs of S_7 (lower than two built-in voltages of two series Schottkys). All in all, conduction losses are reduced because total voltage drop on two, low-resistive MOSFETs is inferior than on two standard MOSFETs connected in series with two Schottky diodes. Sum of average bridge and additional leg currents is equal to the DC link current which proves that seventh switch does not affect operation of the main bridge and increases its efficiency.

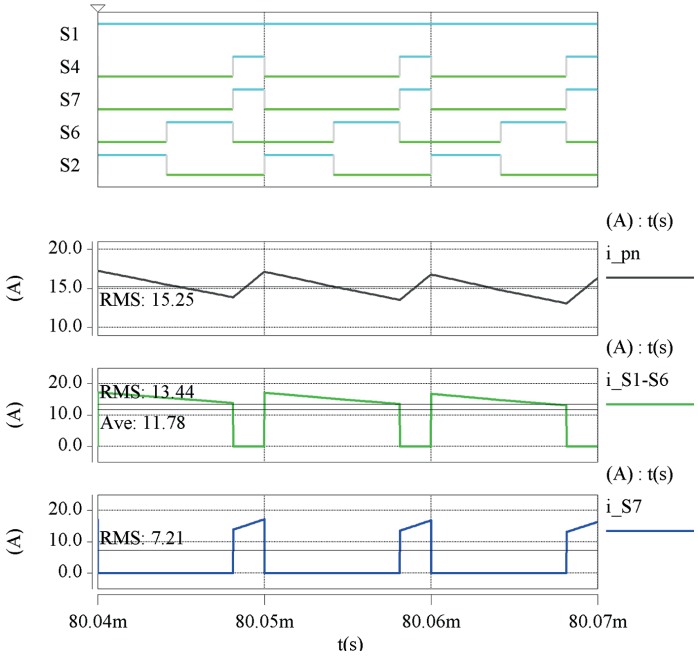


Fig. 10. Inverter mode of the iCFqZSI at 400 V/ 6 kVA, from the top: transistors gate signals, DC link current, 3-phase bridge current and additional leg current.

6. Laboratory model

A high-frequency, SiC based model of the iCFqZSI was designed and built to operate at 100 kHz and 6 kVA. In addition to the selection of SiC semiconductors, custom-made design of inductors, careful selection of the heatsink and optimal placement of all elements were conducted to ensure the best possible switching conditions and correct thermal performance [25].

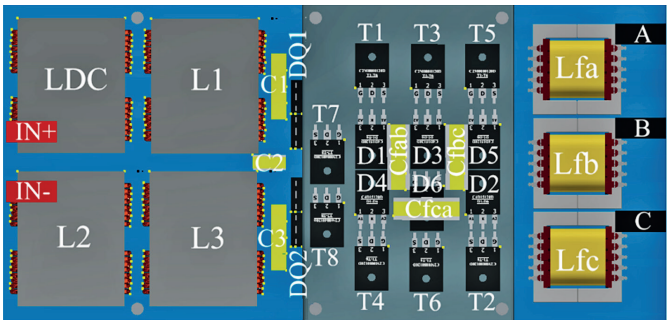
On the base of data from Table 1, the impedance network capacitors B58031U5105M062 from TDK were selected. They are capable of handling high RMS currents and, thanks to the SMD package, are very compact. Then, four inductors of the impedance network were designed on the E64/15/50 and PLT64/50/5 cores from 3F3 material and wounded with Litz wire. As with Table 1, 2×350 µH and 2×700 µH inductors were built with saturation current of 25 A. Taking into account the assumed switching frequency (100 kHz), the LC-filter resonant frequency was selected to be 10 kHz to avoid unnecessary resonance in the circuit [31]. In practice the filter was composed with 0.5 µF capacitors (B58031I7504M062 – 4 units in parallel per phase) and 100 µH inductors (DEMS-42/0.1/25). On the base of the simulation model, currents and voltages in H7 bridge and in impedance network diodes were determined to estimate the power losses in semiconductors [25]. Afterwards, thermal model of the designed iCFqZSI was developed and a value of heatsink thermal resistance was determined under a condition that junction temperature of all semiconductors is below 90°C when ambient temperature is 25°C. Finally, LAM 5 D heatsink was chosen (thermal resistance at 0.27°C/W). Additionally, the selected heatsink enables installation of heat sources from 4 sides. All components of the 6 kVA iCFqZSI model are listed in Table 2.

Table 2
Components of iCFqZSI power stage and their parameters

Element	Name	Quantity/Value
T_1–T_6	C2M0080120D	6
D_1–D_6	C4D15120D	6
T_7–T_8	C2M0040120D	2
D_{Q1}, D_{Q2}	C4D20120D	4
L_{DC}, L_2	L700	2×707 µH
L_1, L_3	L350	2×352 µH
C_1, C_3	B58031U5105M062	2×(4×1 µF)
C_2	B58031U5105M062	2×1 µF
L_f	DEMS-42/0.1/25	3×100 µH
C_f	B58031I7504M062	3×(4×0.5 µF)
Heatsink	LAM 5 D	1

In the next step 3D model of the iCFqZSI was built in Autodesk Inventor 2018 software (Fig. 11a, b). Three dimensional modeling of the inverter allowed optimal component placement and avoiding unintentional errors. On the base of this model, the 6 kVA laboratory model of the iCFqZSI has been built – see Fig. 11c. Design process of the main circuit started with the arrangement of the transistors T_1–T_6 and the diodes D_1–D_6 with maximum possible symmetry of each bridge branch. Additional leg is located on the same plane of the heatsink as the bridge transistors and close to them. Key issue to achieve good switching conditions and high-quality AC side electrical parameters is the location of the filter capacitors – they are placed as close as possible to the power devices. This was much more convenient with delta connection of the capacitors in LC. The diodes of the impedance network were

a)



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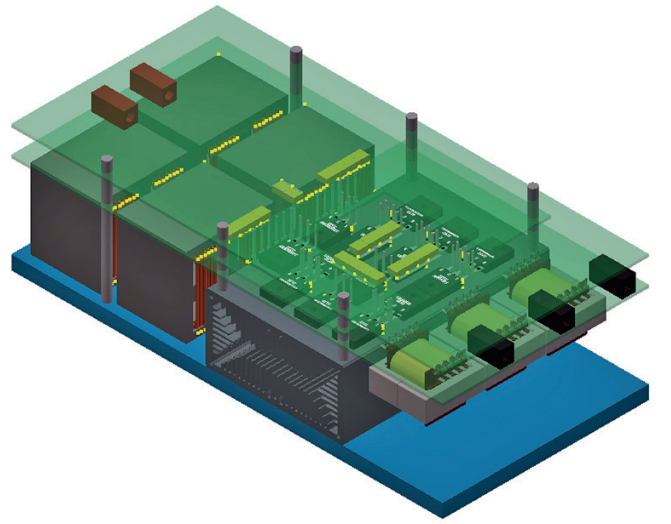

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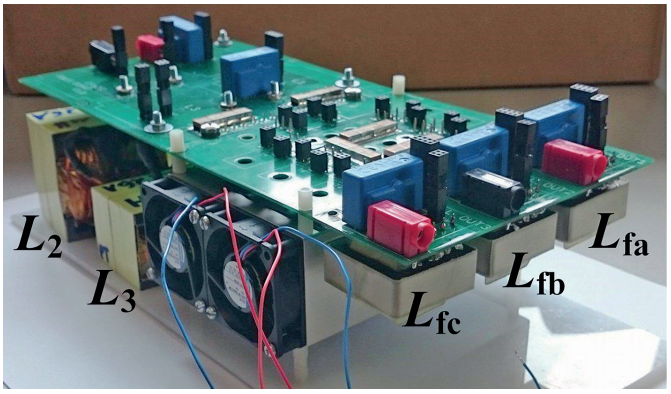


Fig. 11. Power board components placement (a), the 3D model view (b) and complete power stage view (c) of the built iCFqZSI 6 kVA prototype

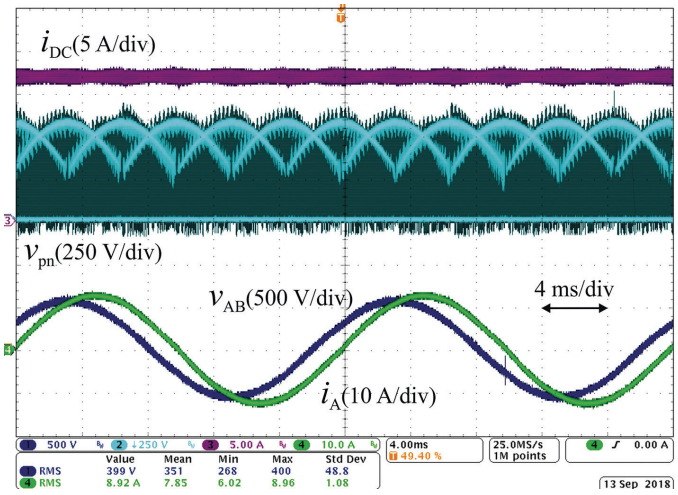
placed on the same backside of the heatsink. All connections to the impedance network capacitors are kept as short as possible to avoid parasitic inductances. Similarly, any parasitic capacitance of the points with floating potentials is avoided [25].

7. Experiments

The laboratory model of the iCFqZSI presented in previous section was a subject of various experiments performed during off-grid and on-grid operation. The control system was based on TMS320F28335, which was mainly providing a grid synchronization and modulation signals at 100 kHz.

7.1. iCFqZSI in the inverter mode. At first, experiments were conducted in the inverter mode – with variable modulation index and input voltage and constant amplitude of the output voltage. Example of the recorded waveforms for $V_{DC} = 400$ V and $M = 0.8$ is presented in Fig. 12 where the input current i_{DC}, voltage across the inverter v_{pn}, output phase-to-phase voltage v_{AB} and phase current i_A can be seen. In both time scales – 4 ms/div scale (Fig. 12a) and 4 µs/div scale (Fig. 12b) – correct operation of the iCFqZSI model can be observed during the operation at nominal conditions (6 kVA/100 kHz). Actually, the iCFqZSI behaves as a conventional CSI as currents in the inductors L_1–L_3 contain AC component only (average value of $i_{qz} = 0$). Voltages across key components of the modified impedance network are presented in Fig. 13. The visible waveforms of the voltages across capacitors (C_1, C_2) and inductors

(a)



(b)

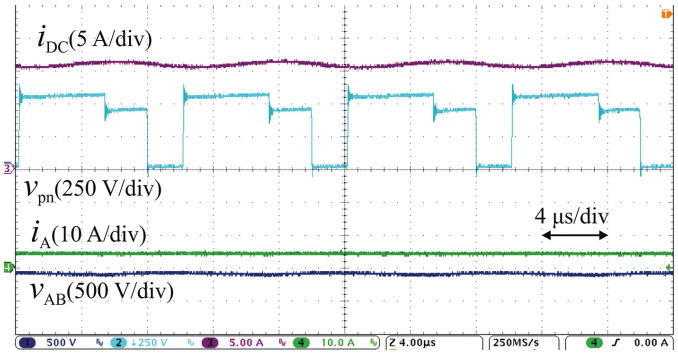


Fig. 12. Waveforms of the input current (i_{DC}), voltage across the inverter (v_{pn}), phase current (i_A) and phase-to-phase voltage (v_{AB}) during steady-state operation of the iCFqZSI inverter mode in 4 ms/div scale (a) and 4 µs/div scale (b)

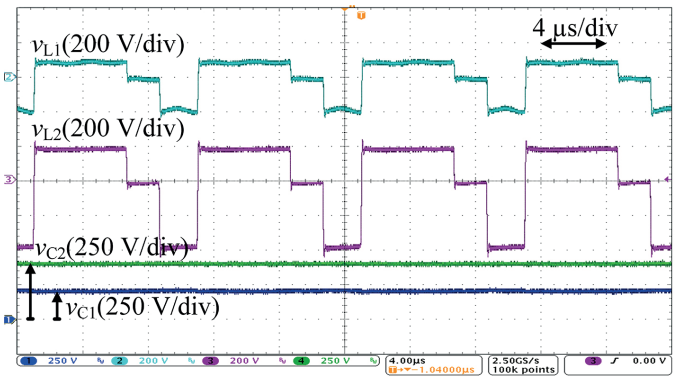


Fig. 13. Voltages across inductors L_1 and L_2 (v_{L1}, v_{L2}), voltages across capacitors C_1 and C_2 (v_{C1}, v_{C2}) during steady-state operation of the iCFqZSI inverter mode in 4 µs/div scale at 3 kVA output power

(L_1, L_2) prove that stress passive elements is reduced with the proposed topology of the impedance network. Moreover, the voltage across D_Q diodes is also decreased.

In the next step a series of power loss measurements were performed with the high-precision power analyzer Yokogawa WT1800 – example of the recorded screen is presented in Fig. 14. The aim was to test the influence of the additional leg, thus the same measurements were repeated for the operation with or without S_7 for various modulation indexes and switching frequencies – see Fig. 15. Examples of 3-leg and 4-leg operation of the iCFqZSI are shown in Fig. 16, where i_{pn}, i_{S7}, i_{S4} currents and v_{pn} voltage can be seen. Along with the increase of the modulation index (shorter zero states) and the input voltage (varying from 300 to 400 V), the bridge current i_{pn} is decreased (lower conduction losses), which results in a rise of the total efficiency (Fig. 15a). On the other hand, decrease of the bridge

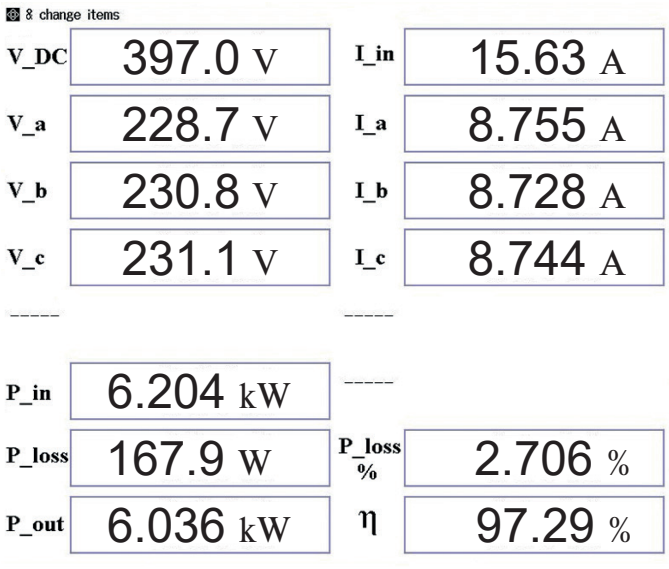


Fig. 14. Screen from the power meter recorded at nominal conditions in the inverter mode with S_7 at $f_s = 100$ kHz, M = 0.8.

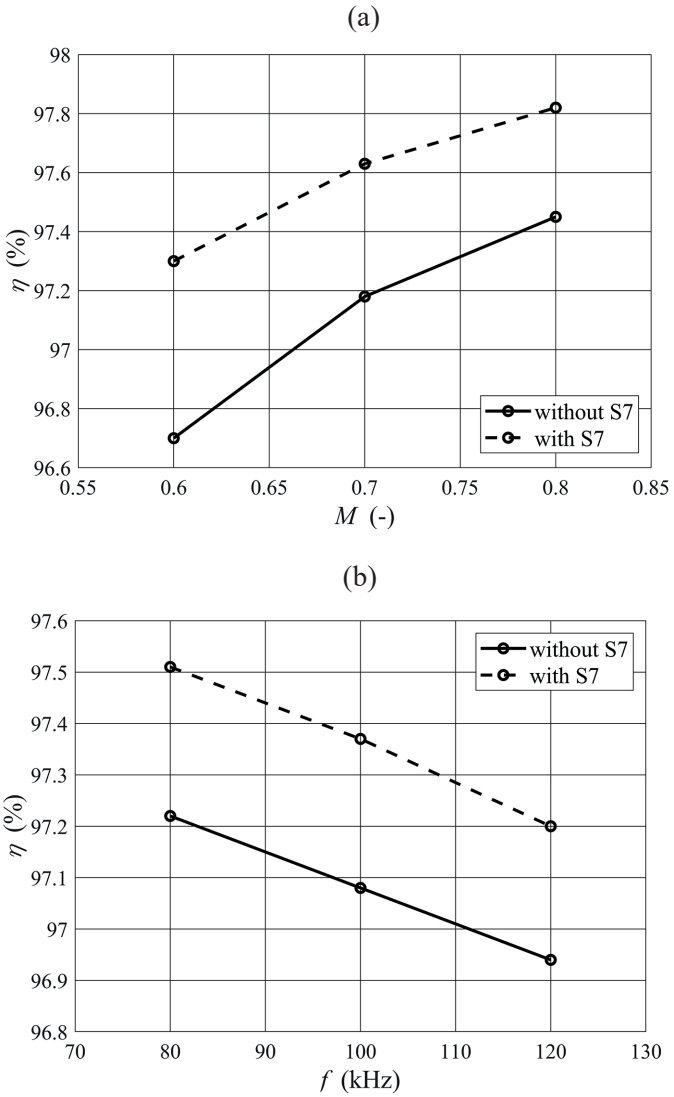


Fig. 15. Efficiency measurements of the iCFqZSI in inverter mode for different modulation techniques: efficiency for 3 kVA output power versus modulation index (a), efficiency for 6 kVA output power versus switching frequency (b).

power devices conduction loss due to the additional leg with two 40 mΩ SiC MOSFETs is more visible for lower modulation indexes (longer zero states) and reaches 0.6% at $M = 0.6$. Moreover, power losses are distributed among 8 power devices in TO-247 package which improves thermal performance. Figure 15 confirms that benefit from the additional leg – reduced on-state losses are higher than the additional switching losses, even for switching frequencies higher than 100 kHz. All in all, peak recorded efficiency during laboratory tests was 97.82%.

7.2. iCFqZSI in the rectifier mode. Further measurements were performed with the iCFqZSI model connected to the three-phase grid. Similarly to other current-fed inverters the iCFqZSI does not require any closed-loop control to be able control the current/power, therefore, the system was synchronized with the grid and operated at 100 kHz with modulation index $M = 0.4$

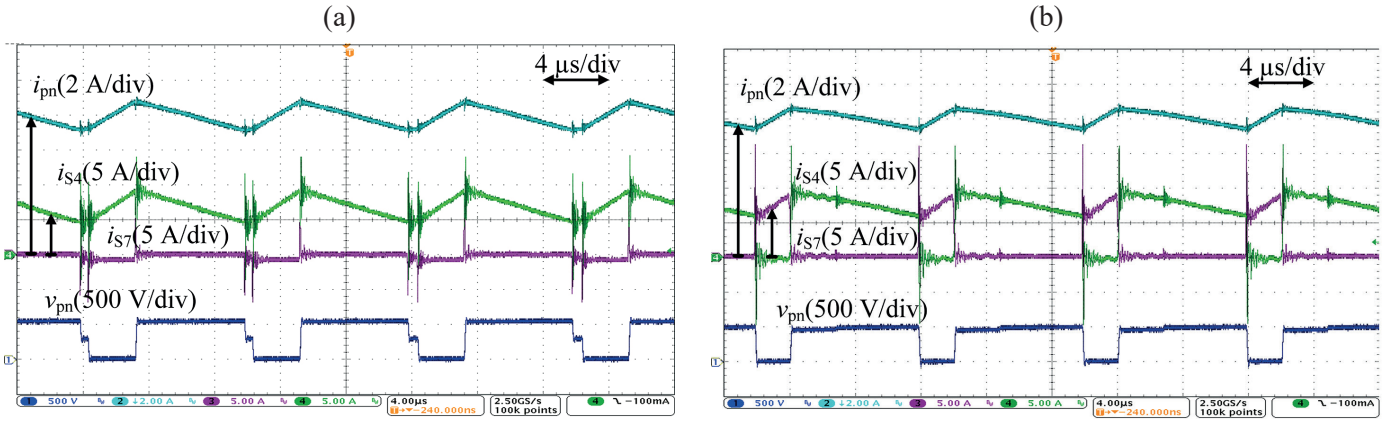


Fig. 16. Waveforms of bridge current (i_{pn}), switch S_4 current (i_{S4}), additional leg current (i_{S7}) and voltage across the inverter (v_{pn}) during steady-state operation of the iCFqZSI inverter mode in 4 µs/div scale at 3 kVA output power during 3-leg operation (a) and 4-leg operation (b)

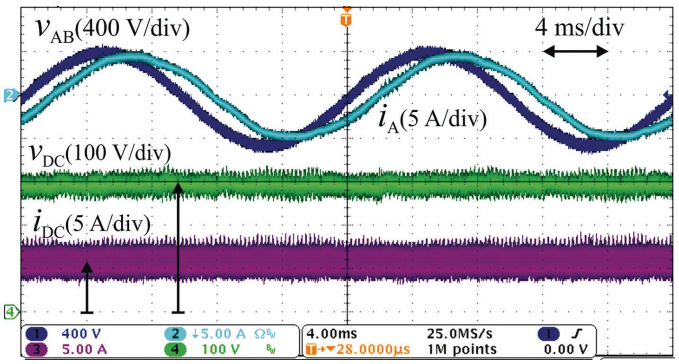


Fig. 17. Waveforms of phase-to-phase voltage (v_{AB}), phase current (i_A), input voltage (v_{DC}) and input current (i_{DC}) during steady-state operation of the iCFqZSI rectifier mode in 4 ms/div scale

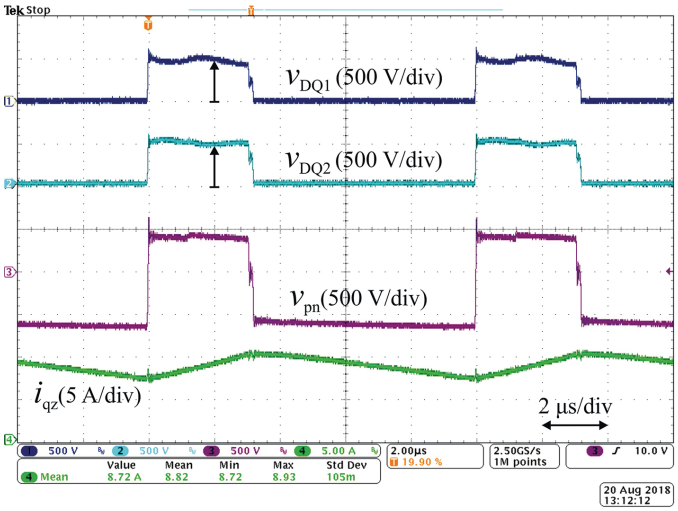


Fig. 18. Waveforms of input diodes voltages (v_{DQ1}, v_{DQ2}), bridge voltage (v_{pn}) and impedance network current (i_{qz}) during steady-state operation of the iCFqZSI rectifier mode in 2 µs/div scale

and $D_{OZ} = 0.6$. Due to safety issues the grid voltage was reduced to 75% of nominal value (the preliminary model was not equipped with protection circuits). Specific waveforms for steady-state are shown in Fig. 17, where phase-to-phase voltage (v_{AB}), phase current (i_A), input voltage (V_{DC}) and current (i_{DC}) are visible. It can be seen that the iCFqZSI works correctly in the rectifier mode, quality of the input and output waveforms is as expected, however, input waveforms are distorted with high-frequency spikes. Another Fig. 18 shows operating conditions of the diodes D_{Q1} and D_{Q2}. The measured waveforms confirm that the voltage across the diodes is reduced to an acceptable level. Moreover, voltage sharing looks proper and each diode is blocking similar amount of the negative voltage during active state. Slight oscillation at the level of tens of volts is caused by the parasitic capacitances and inductances of the diodes and does not have a serious impact on the converter operation. It was also observed that efficiency of the improved current-fed quasi-Z-source inverter is lower in rectifier mode than in inverter mode. The reason is high current stress in components of the impedance network. During test at the highest achieved output power the efficiency was measured at the level of 84.8%.

8. Conclusion

Comprehensive investigations on the novel topology of the improved current-fed quasi-Z-source inverter have been focused on the reduction of the voltage and current stress on the passive components and, especially the SiC power devices. It has been proven that the main drawback of the standard CFqZSI – high voltage stress across input diode in rectifier mode – has been solved and two Schottky diodes block two times lower voltages. In consequence, the developed SiC based 6 kVA laboratory model has been able to operate at high frequency of 100 kHz with peak efficiency of 97.8%. Furthermore, significant reduction of the current stress due to additional leg of two 40 mΩ SiC MOSFETs has been also confirmed, increase of the efficiency up to 0.6% has been observed.

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References

[1] S. Nonaka, K. Kesamaru, K. Yamasaki, and M. Nishi, "Interconnection system with single phase IGBT PWM CSI between photovoltaic arrays and the utility line," in *Conference Record of the 1990 IEEE IAS Annu. Meeting* 2, Seattle, WA, USA, pp. 1302–1307, 1990.

[2] M.K. Kazimierczuk and R.C. Cravens, "Current-source parallel-resonant DC/AC inverter with transformer," *IEEE Transactions on Power Electronics* 11(2) 275–284, March 1996.

[3] C. Klumpner, "A New Single-Stage Current Source Inverter for Photovoltaic and Fuel Cell Applications using Reverse Blocking IGBTs," in *2007 IEEE Power Electronics Specialists Conference*, Orlando, FL, pp. 1683–1689, 2007.

[4] B. Sahan, A.N. Vergara, N. Henze, A. Engler, and P. Zacharias, "A Single-Stage PV Module Integrated Converter Based on a Low-Power Current-Source Inverter," *IEEE Trans. Ind. Electron* 55(7), 2602–2609, 2008.

[5] M. Rajeev and V. Agarwal, "Single Phase Current Source Inverter With Multiloop Control for Transformerless Grid–PV Interface," *IEEE Trans. Ind. Appl* 54(3), 2416–2424, 2018.

[6] I. Koch, F. Hinrichsen, and W.-R. Canders, "Application of SiC-JFETs in current source inverter topologies," in *2005 European Conference on Power Electronics and Applications*, Dresden, pp. 7 pp.-P.7, 2005.

[7] A. Domino, K. Zymmer, and M. Parchomiuk, "Comparative study between two-level and three-level high-power low-voltage AC-DC converters," *Bull. Pol. Ac.: Tech.* 67(3) 583–592 , 2019.

[8] T. Friedli, S.D. Round, F. Krismer, and J.W. Kolar, "Design and Performance of a 200 kHz All-SiC JFET Current Source Converter," in *2008 IEEE IAS Annu. Meeting*, Edmonton, AB, Canada, pp. 1–8, 2008.

[9] J. Rabkowski and R. Barlik, "Three-phase grid inverter with SiC JFETs and Schottky diodes," in *2009 MIXDES-16th International Conference Mixed Design of Integrated Circuits & Systems*, Lodz, pp. 181–184, 2009.

[10] F. Xu, B. Guo, L.M. Tolbert, F. Wang, and B.J. Blalock, "Design and performance of an all-SiC three-phase buck rectifier for high efficiency data center power supplies," in 2012 *IEEE Energy Conversion Congress & Exposition (ECCE)*, Raleigh, NC, USA, pp. 2927–2933, 2012.

[11] E. Lorenzani, F. Immovilli, C. Bianchini, and A. Bellini, "Performance analysis of a modified Current Source Inverter for photovoltaic microinverter applications," in *IECON 2013 – 39th Annual Conference of the IEEE Industrial Electronics Society*, Vienna, pp. 1809–1814, 2013.

[12] J. Martin, A. Bier, S. Catellani, L.G. Alves-Rodrigues, and F. Barruel, "A high efficiency 5.3kW Current Source Inverter (CSI) prototype using 1.2kV Silicon Carbide (SiC) bi-directional voltage switches in hard switching," in *PCIM Europe 2016; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, Nuremberg, Germany, pp. 1–8, 2016.

[13] L.G.A. Rodrigues, G. Lefèvre, J. Martin, and J.P. Ferrieux, "Switching cell design optimization of SiC-based power modules for current source inverter applications," in *2017 19th Proc. Eur. Conf. Power Electron. Appl. (EPE'17 ECCE Europe)*, Warsaw, pp. P.1-P.10, 2017.

[14] T.B. Soeiro and M.L. Heldwein, "Bidirectional three-phase PFC concept based on an integrated inverting-link current source converter," in *2013 IEEE Energy Convers. Congr. Expo (ECCE)*, Denver, CO, USA, pp. 5137–5144, 2013.

[15] J. Anderson and F.Z. Peng, "Four quasi-Z-Source inverters," in *2008 Power Electron. Spec. Conf.*, Rhodes, Greece, pp. 2743–2749, 2008.

[16] V.P. Galigekere and M.K. Kazimierczuk, "Analysis of PWM Z-Source DC-DC Converter in CCM for Steady State," *IEEE Transactions on Circuits and Systems I: Regular Papers* 59(4), 854–863, April 2012.

[17] S. Yang, F.Z. Peng, Q. Lei, R. Inoshita, and Z. Qian, "Current-Fed Quasi-Z-Source Inverter With Voltage Buck–Boost and Regeneration Capability," *IEEE Trans. Ind. Appl* 47(2), 882–892, 2011.

[18] Q. Lei, S. Yang, F.Z. Peng, and R. Inoshita, "Application of current-fed quasi-Z-Source Inverter for traction drive of hybrid electric vehicles," in *2009 IEEE Veh. Pow. and Prop. Conf*, Dearborn, USA, pp. 754–760, 2009.

[19] Q. Lei, F.Z. Peng, L. He, and S. Yang, "Power loss analysis of current-fed quasi-Z-source inverter," in *2010 IEEE Energy Convers. Congr. Expo (ECCE)*, Atlanta, GA, USA, pp. 2883–2887, 2010.

[20] Q. Lei, F.Z. Peng, and S. Yang, "Discontinuous operation modes of current-fed Quasi-Z-Source inverter," in *2011 Twenty-Sixth Annual Proc. IEEE Appl. Power Electron. Conf. (APEC)*, Fort Worth, TX, USA, pp. 437–441, 2011.

[21] X.P. Fang, Z.Q. Chen, and X.G. Wang, "Current-Fed Quasi-Z-Source Inverter-Based Adjustable Speed Drive System With Bidirectional Power Flow," *IEEE Trans. Appl. Supercond.* 24(5), 1–6, 2014.

[22] Q. Lei, D. Cao and F.Z. Peng, "Novel Loss and Harmonic Minimized Vector Modulation for a Current-Fed Quasi-Z-Source Inverter in HEV Motor Drive Application," *IEEE Trans. on Power Electronics* 29(3) 1344–1357, 2014.

[23] Q. Lei, D. Cao, and F.Z. Peng, "Novel SVPWM switching pattern for high efficiency 15KW current-fed quasi-Z-source inverter in HEV motor drive application," in *2012 Twenty-Seventh Annual Proc. IEEE Appl. Power Electron. Conf. (APEC)*, Orlando, FL, USA, pp. 2407–2420, 2012.

[24] F.E. Alfaris and S. Bhattacharya, "A current-fed quasi Z-source inverter with SiC power modules for EV/HEV applications," in *2017 IEEE Energy Convers. Congr. Expo*, Cincinnati, OH, USA, pp. 5445–5452, 2017.

[25] P. Trochimiuk, M. Zdanowski, P. Majtczak, and J. Rabkowski, "Design of a High-Frequency Improved Current-Fed Quasi Z-Source Inverter based on SiC devices," in *2018 Progress in Applied Electrical Engineering (PAEE)*, Koscielisko, Poland, pp. 1–6, 2018.

[26] M. Zdanowski, P. Trochimiuk, and J. Rabkowski, "Modified Current-Fed Quasi Z-Source Converter with Reduced Voltage Stress Across SiC Power Devices," in *2018 20th European Conference on Power Electronics and Applications (EPE'18 ECCE Europe)*, Riga, 2018, pp. P.1-P.10.

[27] W. Wang, F. Gao, Y. Yang, and F. Blaabjerg, "Operation and Modulation of H7 Current-Source Inverter With Hybrid SiC and Si Semiconductor Switches," *IEEE Journal of Emerging and Selected Topics in Power Electronics* 6(1) 387–399, 2018.

[28] Datasheet of C2M0080120D from Wolfspeed webpage www.wolfspeed.com, 2018.

[29] Datasheet of C2M0040120D from Wolfspeed webpage www.wolfspeed.com, 2018.

[30] Datasheet of C4D15120D from Wolfspeed webpage www.wolfspeed.com, 2018.

[31] S. Jayalath and M. Hanif, "CL-filter design for grid-connected CSI," in 2015 IEEE 13th Brazilian Power Electronics Conference and 1st Southern Power Electronics Conference (COBEP/SPEC), Fortaleza, Brazil) 1–6, 2015.