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Analysis of triple metal surrounding gate (TM-SG) III–V nanowire MOSFET for photosensing application

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ABSTRACT

In this paper, a low power highly sensitive Triple Metal Surrounding Gate (TM-SG) Nanowire MOSFET photosensor is proposed which uses triple metal gates for controlling short channel effects and III–V compound as the channel material for effective photonic absorption. Most of the conventional FET based photosensors that are available use threshold voltage as the parameter for sensitivity comparison but in this proposed sensor on being exposed to light there is a substantial increase in conductance of the GaAs channel underneath and, thereby change in the subthreshold current under exposure is used as a sensitivity parameter (i.e., $I_{illumination}/I_{Dark}$). In order to further enhance the device performance it is coated with a shell of $Al_xGa_{1-x}As$ which effectively passivates the GaAs surface and provides a better carrier confinement at the interface results in an increased photoabsorption. At last performance parameters of TM-SG Bare GaAs Nanowire MOSFET are compared with TM-SG core-shell GaAs/AlGaAs Nanowire MOSFET and the results show that Core-Shell structures can be a better choice for photodetection in visible region.

1. Introduction

From decades, one golden rule has guided the entire microelectronics world, the downscaling of the Metal Oxide Semiconductor Field Effect Transistor (MOSFET). Downscaling the device degrades the gate controllability over the channel and has the disadvantage of increased short channel effects (SCE's) [1,2]. Several novel design structures has been proposed to extend device scaling down to nanometer regime [3–6]. Out of those novel device structures Multigate MOSFET's proved to be one of the most effective solutions to reduce SCE's. In several Multigate structures, Gate-All-Around (GAA) Nanowire MOSFETs have a better electrostatic coupling between gate and the channel as gate electrode completely surrounds the channel which in turn reduces off state leakage current and provides immunity from short channel effects (SCEs) [7–9]. Many authors in the recent past have also reported gate stack engineering [10,11] an effective way to reduce off state leakage current which provides a pathway to scale down beyond 45 nm as reported in International Roadmap to Semiconductor [12,13]. Despite using high-k dielectrics, SCE's is still a problem when channel length reduces further down. Authors have also suggested that Gate Material engineering can be one of the effective solution for down scaling further down to 20 nm [14]. Dual Material Surrounding Gate MOSFET (DMSG) has been proposed which improves SCE's as compared to Single Material Surrounding Gate [15]. Recently, triple material(TM)in SG MOSFET isreported by Wang et al. [16] in which a formation of two-step potential in the channel allows further gate length scaling which effectively diminishes the SCEs as compared with both Single Metal and Dual Metal MOSFET.

Semiconductor nanowires have gained much attention in the near past for their novel photonic, electronic, mechanical, thermal and electrical properties [17–20]. Semiconductor nanowires have one dimensional structure possess large surface to volume ratio [21] which can be utilized in the effective confinement of light energy and, hence, this unique feature is favourable in the designing of highly sensitive photodetectors, optical interconnects, and solar cells [22–24]. As compared to a indirect band gap semiconductor (e.g., Si), a direct band gap semiconductor nanowire III–V compound such as Gallium Arsenide (GaAs) has an advantage of absorbing light energy more efficiently. MOSFETs made up of GaAs as the channel material also offer very high carrier mobility [25]. As bare GaAs Nanowire has large density of surface states because of its inherent geometry which in turn severely degrades device characteristics by pinning the surface Fermi energy [26–28]. So in order to prevent device degradation in bare GaAs is coated with shell of $Al_xGa_{1-x}As$ that passivates the non radiative charge trap-

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swhich and decreases surface scattering results in higher carrier transport efficiency [29,30]. Also, it is found that a tri-metal gate nanowire MOSFET with gate stack provides high performance in analogue and RF application [31]. Moreover, a simplified compact model, comprising quantum effects for cylindrical nanowire MOSFET was developed by Ragi et al. [32], which reduces the complexity involved in previous models.

In this paper, to incorporate the effect of both Triple Metal Gate and III–V compound channel material, we demonstrate a Triple Metal Surrounding Gate III–V Nanowire MOSFET (TM-SG) photosensor in which triple metal gate with different work functions are used to enhance carrier transport proficiency. Higher work function metal is placed near the source end to accelerate the charge carrier inside the channel [30]. Lower work function metal is placed near the drain end which will reduce the peak electric field at the drain side and, hence, results in a reduced Hot Carrier Effect [30]. GaAs is used as the device material for effective absorption of light energy in the desired region of spectrum. GaAs being a direct bandgap semiconductor absorbs light more efficiently as compared to indirect bandgap materials. Further the impact of encapsulation of GaAs with $Al_xGa_{1-x}As$ acting as a shell is studied on photosensitivity and Quantum Efficiency.

2. Device structure and simulation setup

Figure 1(a) depicts the 2D-cross section view of TM-SG GaAs MOSFET, Figure 1(b) depicts the 2D-cross section view of TM-SG Core-Shell GaAs/AlGaAs MOSFET and Figure 1(c) depicts the 3D-simulated structure of TM-SG MOSFET under incident radiation. R is the radius of channel, L is the channel length, L_S is the source length, L_D is the drain length, z is the channel direction, and t_{ox} is the oxide thickness and L_1, L_2, L_3 are the lengths of Metal Gates.

In order to extricate device characteristics under dark and under incident radiationa SILVACO ATLAS-3D simulator [33] is used to simulate TM-SG III–V Nanowire MOSFET. The parameters used in the simulation process are as given in Table 1. It also incorporates an advance LUMINOUS-3D optical device simulator to extricate device characteristics under incident radiation which uses Ray Trace method for calculating the photogeneration rate at defined mesh points. The optical parameters for the incident radiation such as radiation intensity, wavelength and location is set by using a BEAM keyword incorporated in a LUMINOUS-3D module. Various models used for the purpose of simulation of TM-SG III–V NanowireMOSFET are: Shockley Read Hall model (SRH) and Bohm Quantum Potential (BQP) with parameters of alpha = 0.5 and gamma = 1.2. SRH model accounts for the chances of recombination phenomenon at traps and BQP model accounts for the inclusion of quantum effects as the radius of the device is less than 5 nm, quantum mechanical effects cannot be neglected [34].

The path of light from air to the channel underneath in Bare GaAs is obstructed due to reflections at three interfaces namely air to gate metal, gate metal to oxide layer and oxide layer to GaAs. For a Core-Shell GaAs-AlGaAs structure one additional interface from oxide layer to AlGaAs is added. Reflection at theses interfaces helps analyzing the behaviour of the device under incident radiation. The reflection coefficients for these three interfaces can be calculated using the formula [35]:

$$R_c = \frac{(n_c - n_{c+1})^2 + {k_{c+1}}^2}{(n_c + n_{c+1})^2 + {k_{c+1}}^2} \quad (1)$$

where R_1, R_2 and R_3 are the reflection coefficients at the three interfaces, i.e., air to metal gate, metal gate to oxide layer and oxide layer to semiconductor respectively. n_1, n_2, n_3 and n_4 are the real part of refractive index of air, gate metal, oxide layer and semiconductor, respectively, and k_cs are the corresponding imaginary part of the refractive indices. SOPRA database [36] is referred to get the real and imaginary values of the refractive index in order to calculate the reflection coefficients for the purpose of simulation of TM-SG III–V Nanowire MOSFET under incident radiation. Table 2 shows the real and imaginary refractive index values for Oxide Layer (Al_2O_3), GaAs and AlGaAs for different wavelengths of incident radiation. It also shows the values of absorption coefficient (α) for GaAs and AlGaAs for different wavelengths.

The amount of incident light being absorbed by the GaAs channel underneath which results in the generation of electron-hole pairs (EHP) depends mainly on the absorption coefficient of GaAs denoted by the absorption coefficient (α). The parameter α for GaAs has different values for different wavelengths (λ) of incident radiation and generally decreases with higher wavelengths [35,37].

Rate of generation of EHP depends upon the absorption of incident radiation by the GaAs channel underneath. As mentioned above the generation rate depends on the absorption coefficient of the photosensitive material which is GaAs in our device. The rate of generation of EHP is given by the formula [38]:

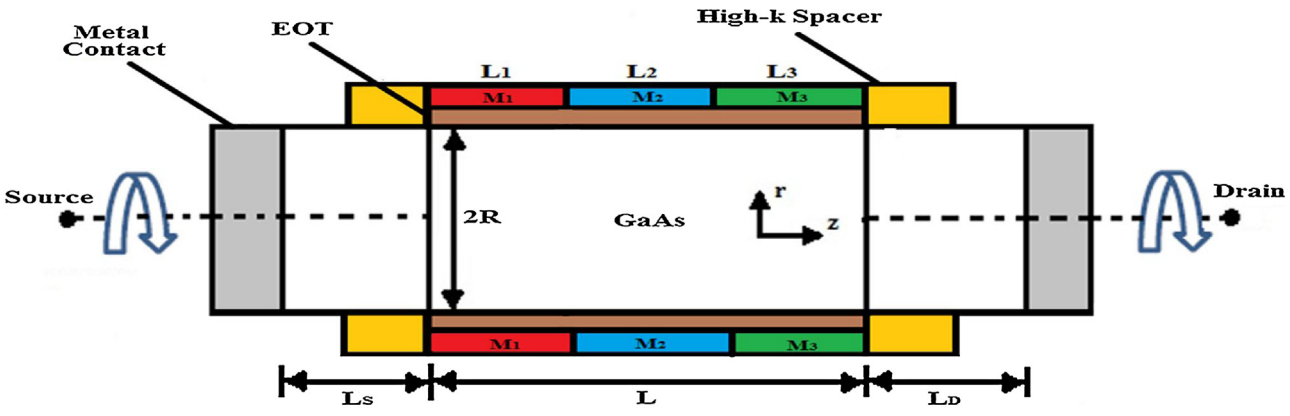
$$G_r = \alpha\phi_d \quad (2)$$

Table 1
Parameters utilized in simulation process.

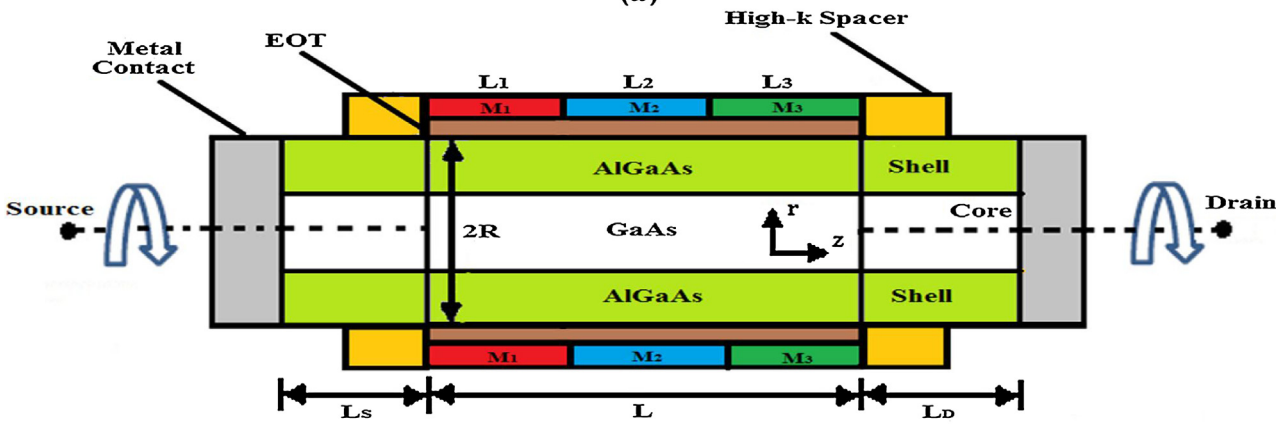
Symbol	Definition	Value
L	Channel length	21 nm
R	Channel radius	2.5 nm
L_S	Source length	20 nm
L_D	Drain length	20 nm
EOT	Equivalent Oxide thickness	0.7 nm
N_A	Channel doping	1×10^{16} cm^{-3}
N_D	Source/Drain doping	1×10^{20} cm^{-3}
L_1	Length of 1st Metal Gate	7 nm
L_2	Length of 2nd Metal Gate	7 nm
L_3	Length of 3rd Metal Gate	7 nm
$Ø_1$	Work Function of 1st Metal Gate	4.8 eV
$Ø_2$	Work Function of 2nd Metal Gate	4.6 eV
$Ø_3$	Work Function of 3rd Metal Gate	4.4 eV
R_c	Radius of Core	1.25 nm
R_s	Radius of Shell	1.25 nm

Table 2
Refractive Indexes of materials used in the simulation of TM-SG Nanowire MOSFET.

Wavelength (μm)	Al_2O_3		$Al_xGa_{1-x}As$ (x = 0.33)			GaAs		
	n	k	n	k	α (cm^{-1}) × 10^6	n	k	α (cm^{-1}) × 10^6
0.25	1.8452	0	2.3924	3.8898	1.9552	2.7760	4.2690	2.145800
0.30	1.8144	0	3.7147	1.9907	0.8338	3.8170	1.9460	0.815140
0.35	1.7972	0	3.6850	2.0257	0.7273	3.5920	1.9610	0.704085
0.40	1.7865	0	4.8247	1.5539	0.4881	4.4590	2.0810	0.653770
0.45	1.7794	0	4.3399	0.5077	0.1417	4.8580	0.7550	0.210840
0.50	1.7742	0	4.0148	0.2956	0.0074	4.3070	0.3760	0.094499
0.55	1.7704	0	3.8466	0.2158	0.0049	4.0580	0.2680	0.061232
0.60	1.7675	0	3.7305	0.1598	0.0033	3.9120	0.2140	0.044820
0.65	1.7651	0	3.6531	0.1136	0.0021	3.8250	0.1780	0.034413



(a)



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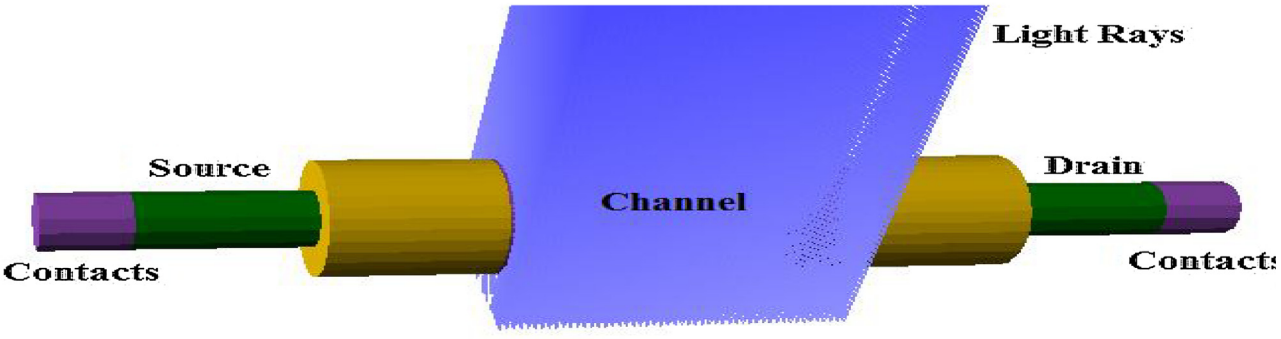

(c)

Fig. 1. **(a)** 2D-Cross Section of TM-SG GaAs MOSFET, **(b)** 2D-Cross Section of TM-SG core-shell GaAs/AlGaAs MOSFET, **(c)** 3D-Simulated structure of TM-SG GaAs MOSFET under incident radiation.

where ϕ_d is the incident spectral photon flux density and is given by [38].

For Bare GaAs Nanowire MOSFET:

$$\phi_d = I_o \frac{h}{c\lambda}(1-R_1)(1-R_2)(1-R_3) \quad (3)$$

where R_3 is the reflection coefficient for the interface Al_2O_3 to GaAs as shown in Table 3.

For Core-Shell GaAs/AlGaAs Nanowire MOSFET:

$$\phi_d = I_o \frac{h}{c\lambda}(1-R_1)(1-R_2)(1-R'_3)(1-R_4) \quad (4)$$

where: I_o is the intensity of incident radiation in Watt/cm^2,
c is the speed of light,
h is the Planck's constant.
R'_3 and R_4 are the reflection coefficients at the interface Al_2O_3 to AlGaAs and AlGaAs to GaAs, respectively as shown in Table 3.

Results and Discussions

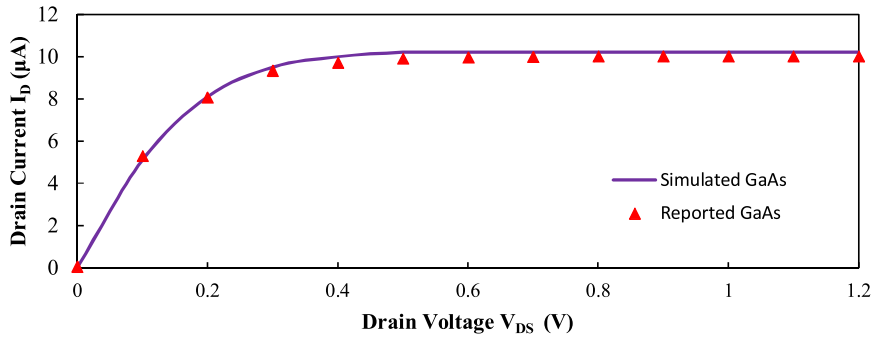

Fig. 2. I_D–V_{DS} characteristics of GaAs Nanowire MOSFET for simulated device and reported device.V_{GS}–V_T = 0.5 V, L = 1 μm, $N_A = 10^{14}$ cm^{-3}, 2R = 15 nm.

Table 3
Reflection Coefficients for different interfaces.

Wavelength (μm)	Al_2O_3 To $Al_{0.33}Ga_{0.66}As$ R'_3	Al_2O_3 To GaAs R_3	$Al_{0.33}Ga_{0.66}As$ To GaAs R_4
0.25	4.66E-01	4.82E-01	4.09E-01
0.30	2.19E-01	2.20E-01	6.28E-02
0.35	2.24E-01	2.15E-01	6.79E-02
0.40	2.52E-01	2.65E-01	4.93E-02
0.45	1.81E-01	2.25E-01	9.84E-03
0.50	1.52E-01	1.77E-01	3.27E-03
0.55	1.38E-01	1.56E-01	1.86E-03
0.60	1.28E-01	1.44E-01	1.35E-03
0.65	1.22E-01	1.37E-01	1.09E-03

From the table it is observed that as the wavelength of incident light increases reflection coefficients at different interface decreases hence at higher wavelengths absorption is predominant due to low reflection coefficients. At higher wavelengths absorption coefficients decreases drastically as shown in Figure 3 the operating wavelength for the proposed TM-SG Nanowire MOSFET.

3. Results and discussions

In order to validate the device the simulation result obtained from the 3D-Device simulator (Atlas 3D) is well calibrated with the result collected from the reported paper of E. G. Marin et al. [39]. Simulation results, as well as reported data extracted at the same parameter for 2R = 15 nm, L = 1 μm, $N_A = 10^{14}$ cm^{-3} are well calibrated as shown in Fig. 2.

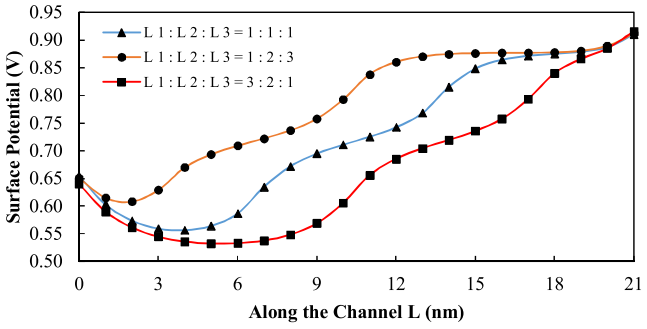

Fig. 3. Surface potential variation along the channel for different metal gate length ratios for TM-SG GaAs MOSFET. V_{DS} = 0.1 V, V_{GS} = 0.5 V, $Ø_1$ = 4.8 eV, $Ø_2$ = 4.6 eV, $Ø_3$ = 4.4 eV, EOT = 0.7 nm, $N_A = 1 \times 10^{16}$cm^{-3}.

Figure 3 shows the variations of surface potential for various metal gate length ration L_1: L_2: L_3. Figure shows that there is a potential abruptness at different point due to the junction formed between the interfaces of different metal gate. This abruptness at junction results in improvement of short channel effects. Moreover, it is observed that minimum potential decides the threshold voltage of the device. From the figure it is observed that as we increase the screen metal gate length L_1 (i.e., source side metal gate length) it not only shifts the potential across the channel but also shifts the

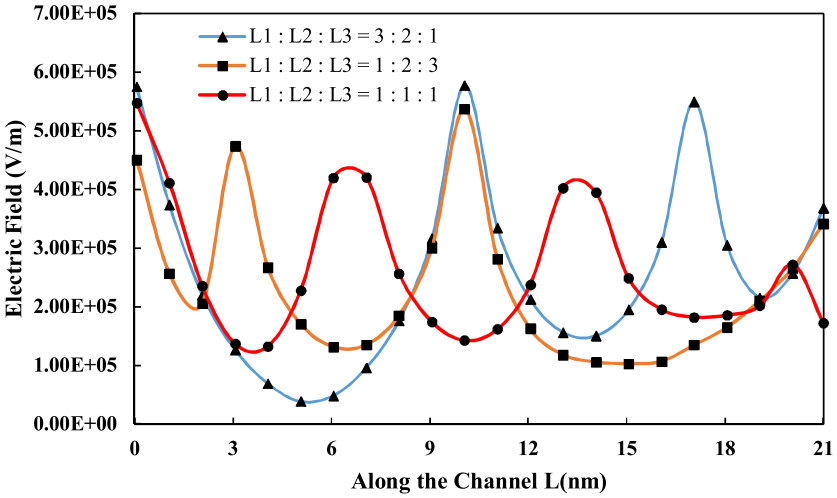

Fig. 4. Electric Field variation along the channel for different metal gate length ratios for TM-SG GaAs MOSFET. V_{DS} = 0.1 V, V_{GS} = 0.5 V, $Ø_1$ = 4.8 eV, $Ø_2$ = 4.6 eV, $Ø_3$ = 4.4 eV, EOT = 0.7 nm, $N_A = 1 \times 10^{16}$cm^{-3}.

minimum potential to a smaller magnitude. This shift in minimum potential increases the $V_T$of the device and reduces the DIBL.

Figure 4 shows the variation of electric field for TM-SG Bare GaAs MOSFET. It is observed from the results that the minimum value of electric field decreases near the source side which results in least impact of drain on the source side as the length of screen gate L_1 increases (i.e., in the case of L_3: L_2: L_1 = 3: 2: 1) which leads to reduction of breakdown voltage, impact ionization and, hence, decreases the off state current as shown in Fig. 5. The figure shows the variation of I_D-V_{GS} characteristics for different metal gate length ration. It is observed that L_3:L_2:L_1 = 3:2:1 shows the lowest off state current that's why we have chosen the length of the metal gate as L_3:L_2:L_1 = 3:2:1 for our device.

Figure 6 is a result showing the variation in I_D-V_{GS} characteristics of TM-SG GaAs Nanowire MOSFET under the different incident power (P_o) at a wavelength λ = 0.550 μm. As incident power increases generation of electrons' hole pair increase results in increased conductivity of GaAs channel under incident power due to photo-gating and photo-dopping effects [40] which results in higher current available under incident radiation and this variation of illumination current with respect to the power variation is more pronounced in subthreshold region as compared to linear or saturation region and, hence, the proposed device works better as a UV–vis Photosensor in subthreshold region. As shown in the figure if we increased the power frompicowatts towards the

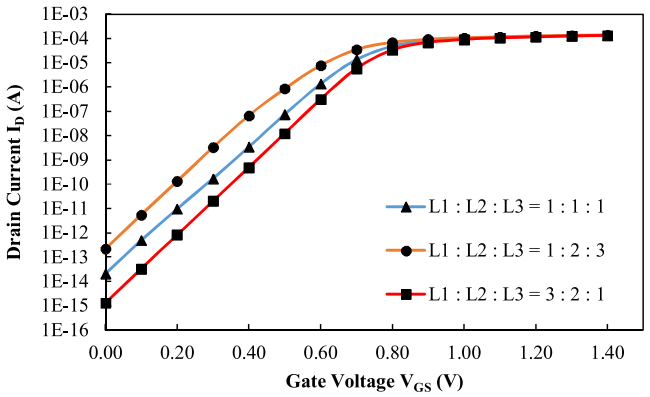

Fig. 5. I_D – V_{GS} characteristics of TM-SG GaAs Nanowire MOSFET for different channel length ratios. V_{DS} = 0.1 V, $Ø_1$ = 4.8 eV, $Ø_2$ = 4.6 eV, $Ø_3$ = 4.4 eV, EOT = 0.7 nm, $N_A = 1 \times 10^{16}cm^{-3}$.

microwatts the available photocurrent increases and maximum saturation occurs at P = .5 μWatts. Further increasing the power degrades the performance of the device and increases its power consumption.

Figure 7 shows the plot of the available photocurrent Vs wavelength extracted at V_{GS} = 0.0 V,V_{DS} = 0.1 V, R = 2.5 nm, L = 21 nm at a fixed power of P_o = 16.5 μWatts where we get the maximum avail-

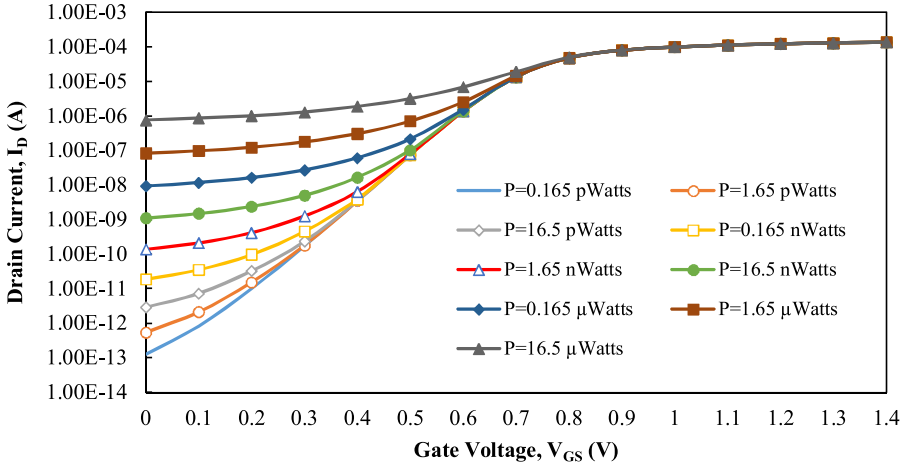

Fig. 6. I_D – V_{GS} characteristics of TM-SG GaAs Nanowire MOSFET under illumination for different incident power. λ = 0.550 μm, L_1:L_2:L_3:3:2:1, V_{DS} = 0.1 V, $Ø_1$ = 4.8 eV, $Ø_2$ = 4.6 eV, $Ø_3$ = 4.4 eV, EOT = 0.7 nm, $N_A = 1 \times 10^{16}cm^{-3}$.

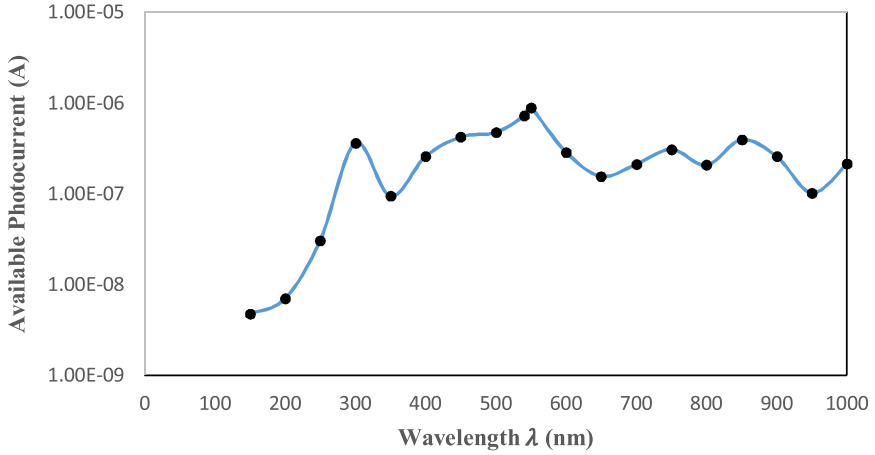

Fig. 7. Available Photocurrent vs. Wavelengthfor TM-SG GaAs Nanowire MOSFET under illumination P_o = 16.5 μWatts, λ = 0.550 μm, L_1:L_2:L_3:3:2:1, V_{DS} = 0.1 V, V_{GS} = 0.0 V, $Ø_1$ = 4.8 eV, $Ø_2$ = 4.6 eV, $Ø_3$ = 4.4 eV, EOT = 0.7 nm, $N_A = 1 \times 10^{16}cm^{-3}$.

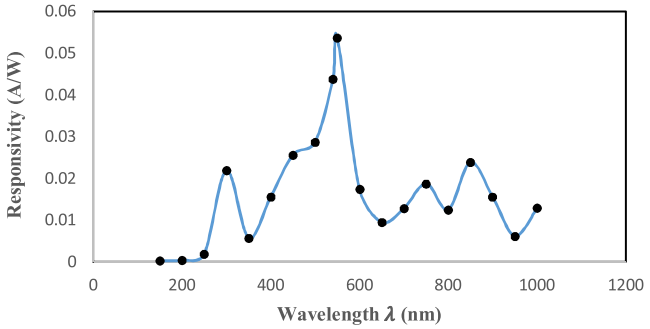

Fig. 8. Responsivity vs. Wavelength for TM-SG Bare GaAs Nanowire MOSFET under illumination $P_o = 16.5\ \mu$Watts, $\lambda = 0.550\ \mu$m, $L_1:L_2:L_3:3:2:1$, $V_{DS} = 0.1$ V, $V_{GS} = 0.0$ V, $Ø_1 = 4.8$ eV, $Ø_2 = 4.6$ eV, $Ø_3 = 4.4$ eV, EOT = 0.7 nm, $N_A = 1 \times 10^{16}$cm^{-3}.

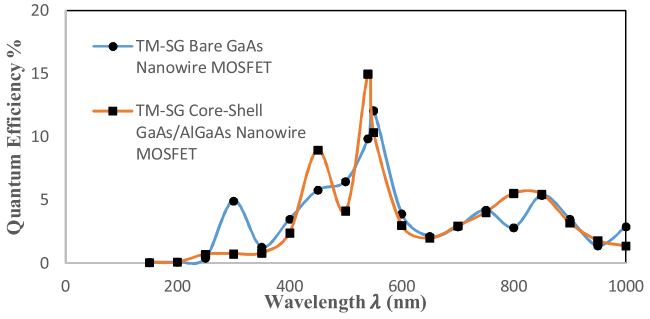

Fig. 11. Quantum Efficiency vs. Wavelength comparisonfor TM-SG Bare GaAs and TM-SG Core-Shell GaAs/AlGaAs Nanowire MOSFET under illumination $P_o = 16.5\ \mu$Watts, $L_1:L_2:L_3:3:2:1$, $V_{DS} = 0.1$ V, $V_{GS} = 0.0$ V, $Ø_1 = 4.8$ eV, $Ø_2 = 4.6$ eV, $Ø_3 = 4.4$ eV, EOT = 0.7 nm, $N_A = 1 \times 10^{16}$cm^{-3}.

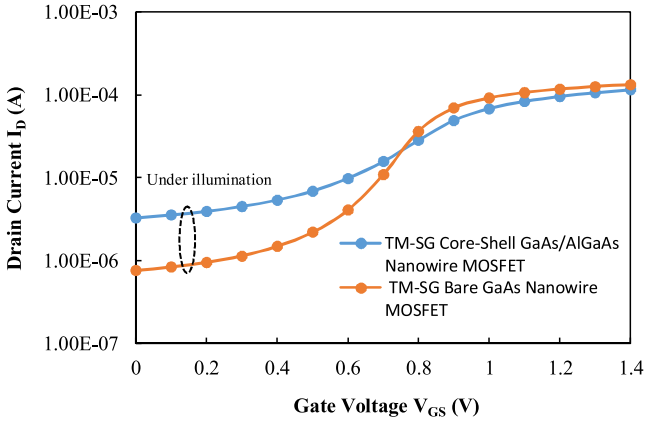

Fig. 9. I_D–V_{GS} characteristics of Bare TM-SG GaAs and Core-Shell TM-SG GaAs/AlGaAs Nanowire MOSFET under illumination. $P_o = 16.5\ \mu$Watts, $L_1:L_2:L_3:3:2:1$, $V_{DS} = 0.1$ V, $Ø_1 = 4.8$ eV, $Ø_2 = 4.6$ eV, $Ø_3 = 4.4$ eV, EOT = 0.7 nm, $N_A = 1 \times 10^{16}$ cm^{-3}.

able photocurrent observed in figure. From the figure it shows that the peak of available photocurrent occurs around 0.550 μm. Because at this wavelength the maximum light is absorbed from the source reaching the GaAs channel.

Figure 8 shows the responsivity of the TM-SG GaAs MOSFET with a wavelength ranging from 0.15 μm–1 μm. From the given figure it is observed that peak Responsivity is observed at λ=0.550 μm extracted at $V_{GS} = 0.0$ V, $V_{DS} = 0.1$ V, R = 2.5 nm, L = 21 nm, at fixed $P_o = 16.5\ \mu$Watts. As the peak responsivity lies in the visible region of spectrum, hence proposed device works efficiently as a visible photodetector which is of great importance in environment, biological and sensing applications [41,42].

However, we can increase the performance of the bare GaAs nanowire MOSFET, by capping it with a shell of suitable material whose bandgap is more than the bandgap of the GaAs. In present work we chose $Al_xGa_{1-x}As$(x = 0.33) as a capping material due to its lattice match with GaAs [43]. Capping with the shell of AlGaAs decreases the non radiative carrier traps, decreases the surface scattering, as well as potential fluctuations which otherwise present in bare GaAs.TM-SG Bare GaAs Nanowire MOSFET response is compared with the TM-SG Core-Shell GaAs/AlGaAs Nanowire photosensor. The core shell significantly improves the illumination current as shown in Figure 9 .

The figure shows the I_D–V_{GS} charV_{GS} obtained by illuminating with the power of 16.5 μWatts. At this power bare GaAs shows the illumination current as 7.64E-07 whereas Core-Shell GaAs/AlGaAsshows the illumination current as 3.28E-06 which is 4.29 times higher than that of bare GaAs.

Figure 10 Figure 10 shows the responsivity comparison of the TM-SG Bare GaAs, as well as TM-SG Core-Shell GaAs/AlGaAs Nanowire MOSFET. TM-SG Bare GaAs shows the peak responsivity of 0.053A/W at λ = 0.550 μm and for TM-SG core-shell GaAs/AlGaAs the peak responsivity is of 0.0654A/W at λ = 0.540 μm. This shift in the peak value of the responsivity depends upon number of factors like absorption and reflection coefficient of GaAs and AlGaAs, as well as channel thickness.

Figure 11 shows the Quantum Efficiency comparison of the TM-SG Bare GaAs, as well as TM-SG Core-Shell GaAs/AlGaAs Nanowire MOSFET. Bare GaAs shows the peak Efficiency of 12% at λ = 0.550 μm whereas for core-shell GaAs/AlGaAs the peak Effi-

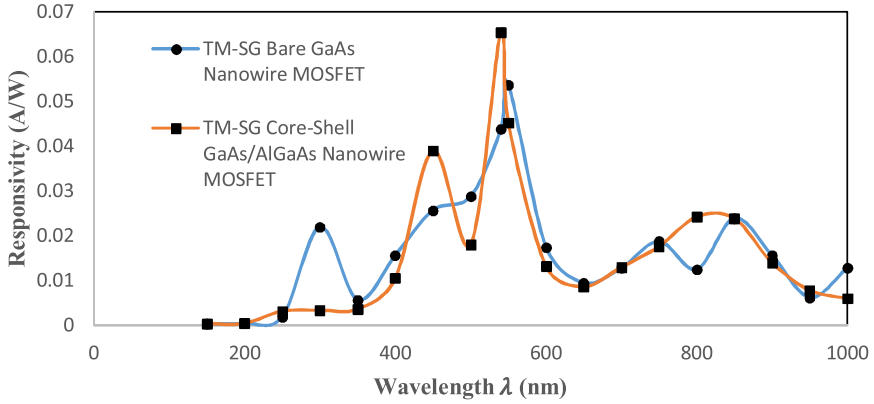

Fig. 10. Responsivity vs. Wavelength comparisonfor TM-SG Bare GaAs and TM-SG Core-Shell GaAs/AlGaAs Nanowire MOSFET under illumination $P_o = 16.5\ \mu$Watts, $L_1:L_2:L_3:3:2:1$, $V_{DS} = 0.1$ V, $V_{GS} = 0.0$ V, $Ø_1 = 4.8$ eV, $Ø_2 = 4.6$ eV, $Ø_3 = 4.4$ eV, EOT = 0.7 nm, $N_A = 1 \times 10^{16}$cm^{-3}.

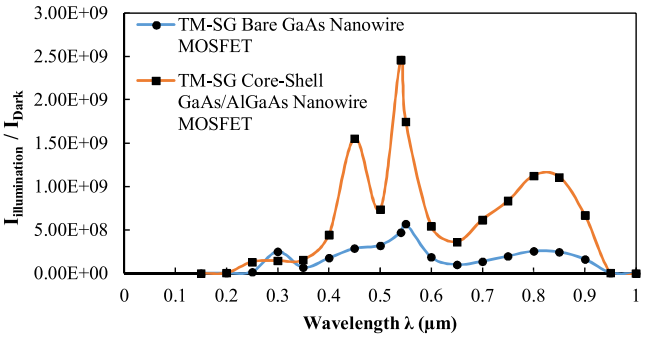

Fig. 12. Sensitivity vs. Wavelength comparisonfor TM-SG Bare GaAs and TM-SG Core-Shell GaAs/AlGaAs Nanowire MOSFET under illumination $P_o = 16.5$ μWatts, $L_1:L_2:L_3:3:2:1$, $V_{DS} = 0.1$ V, $V_{GS} = 0.0$ V, $Ø_1 = 4.8$ eV, $Ø_2 = 4.6$ eV, $Ø_3 = 4.4$ eV, EOT = 0.7 nm, $N_A = 1 \times 10^{16}$cm^{-3}.

ciency is of 15% at λ = 0.540 μm which is 3% higher than that of Bare GaAs and hence capping effectively increases quantum efficiency.

Figure 12 shows the comparison of sensitivity ($I_{Illuminination}/I_{Dark}$) at V_{GS}=0.0 V, V_{DS}=0.1 V, $P_o = 16.5$ μWatts. It is observed from the figure that the peak sensitivity for bare GaAs is of 5.74E+08 at λ = 0.550 μm and for TM-SG core-shell GaAs/AlGaAs peak sensitivity is observed to be 2.46E + 09. It clearly shows that TM-SG Core-Shell GaAs/AlGaAs Nanowire MOSFET is a better device for highly sensitive photosensing application as compared to the bare TM-SG GaAs Nanowire MOSFET.

4. Conclusions

In the paper, we have designed a TM-SG Bare GaAs Nanowire MOSFET and to improve its photoabsorption efficiency we have encapsulated it with a capping of AlGaAs to create a new device named as TM-SG Core-Shell GaAs/AlGaAs Nanowire MOSFET. Bare GaAs after being illuminated with light intensity shows the maximum increase in drain current at gate bias $V_{GS} = 0.0$ V. With the variation in the intensity of light or incident power the drain current increases with increase in the incident power till it achieves its saturation point, where saturation point is defined as when the device gets on at $V_{GS} = 0.0$ V. Moreover, the available photocurrent also depends upon the wavelength of light being incident. Higher the wavelength more will be the available photocurrent, hence more will be the responsivity. But as the wavelength of light exceeds the critical value photoresponse of the proposed device again decreases due to many factors including decreases in the absorption coefficients at higher wavelength, reflections at different interfaces, thickness of the GaAs as channel material and many more. So there is a tradeoff between the desired wavelength of operation and the maximum available photoresponse, hence the proposed device TM-SG Bare GaAs MOSFET shows peak response at a wavelength of λ = 0.550 μm. The maximum available responsivity is of 0.053A/W and the maximum quantum efficiency is of 13% with a photosensitivity [i.e., the ratio ($I_{Illuminination}/I_{Dark}$)] of 5.74E+08. Further encapsulating the bare GaAs with a shell of AlGaAs has the advantage of surface passivation and better carrier confinement in the interface between GaAs and AlGaAs due to a higher bandgap of AlGaAs. Hence, this further increases the photoresponse and the encapsulated device TM-SG Core-Shell GaAs/AlGaAs shows a peak responsivity of 0.0654A/W and the maximum quantum efficiency of 15% at λ = 0.540 μm which is 3% higher than TM-SG Bare GaAs Nanowire MOSFET. The photosensitivity is also increased from 5.74E+08 to 2.46E+08, i.e., 4.29 times. There is a shift in peak occurring wavelength for Core-Shell structure due to on many factors including core-shell thickness and absorption coefficient of AlGaAs. As the above proposed devices work efficiently in visible region of spectrum. Hence, these structures can be used in UV–vis Photodetection applications.

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