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The Behavioural Model of Graphene Field-effect Transistor

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***Abstract*—The behavioural model of a graphene field-effect transistor (GFET) is proposed. In this approach the GFET element is treated as a "black box" with only external terminals available and without considering the physical phenomena directly. The presented circuit model was constructed to reflect steady-state characteristics taking also into account GFET capacitances. The authors' model is defined by a relatively small number of equations which are not nested and all the parameters can be easily extracted. It was demonstrated that the proposed model allows to simulate the steady-state characteristics with the accuracy approximately as high as in the case of the physical model. The presented compact GFET model can be used for circuit or system-level simulations in the future.**

***Keywords*—Graphene field-effect transistor, behavioural model, circuit simulations, sensors**

I. Introduction

In many different electronic applications a field-effect transistor (FET) plays a crucial role. The so-called field effect, being the result of an electric field generation by the external voltage applied across the insulated gate and the source electrodes, is responsible for controlling the semiconductor conductivity in the region between the source and the drain contacts (the channel) for both the electron and hole carriers. In the static on-state a conventional metal-oxide semiconductor field-effect transistor (MOSFET) device enables to control the i_D drain current by the u_{GS} voltage between the gate and the source pads without any consumption of the power. This technology is still under development aimed to improve the performance of the MOSFET transistors and to reduce their size. Recently, it has been demonstrated that graphene field-effect transistors (GFET) could successfully compete with the existing FET technology [1], [2].

Graphene consists of monolayer sheets of carbon atoms arranged in a honeycomb structure. The electronic structure of graphene indicates that this material is a zero-gap semiconductor because conduction and valence bands meet at the corners of the Brillouin zone. The low energy band dispersion at these points, which are commonly called Dirac points, is linear, revealing that the charge carriers in graphene could be treated as massless Dirac fermions moving with the Fermi velocity of approximately 10^6 m/s. Because of the zero density of states at the Dirac points, electronic conductivity of graphene is actually very low. However, it could be enhanced by the appropriate doping with electrons or holes to create a material with a potentially better conductivity than in metals. In large part, the constantly increasing interest in GFET is caused by its great potential for developing sensors (e.g. [3]–[8]) to enable detection of target factors with a much higher accuracy than in the currently used commercial devices. In graphene-based sensor applications the external physical, chemical or biological factor introduces additional charge to the system, what results in the shift of current-voltage ($I - V$) transfer characteristics [9], [10]. In Fig. 1 an important example of highly sensitive GFET-based biosensor, capable of detecting SARS-CoV-2 virus in clinical samples [11], is presented. This COVID-19 sensor contains the graphene layer, which is functionalized with SARS-CoV-2 spike antibody and enables detection of antigen protein with a limit as low as 1 fg/mL. The unquestionable advantage of the reported biosensor is that the SARS-CoV-2 antigen protein could be distinguished from the one of MERS-CoV.

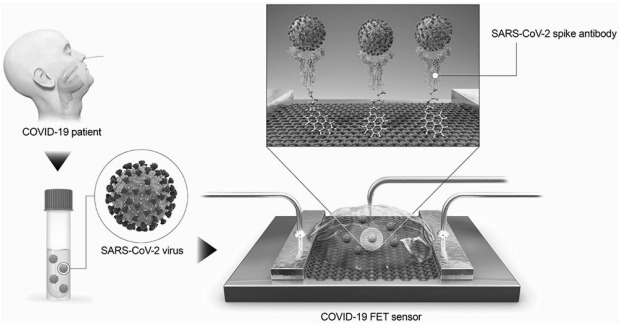

Fig. 1. Graphene field-effect transistor as a COVID-19 sensor [11]

It was demonstrated that typical static characteristics of the graphene field-effect transistor could be well reproduced from a physical model [12]. The aim of this article is to present the behavioural model taking into account such fundamental phenomena as nonlinear steady-state characteristics and the influence of parasitic capacitance which can be easily adapted for further effective circuit simulations.

II. Model

A. Problem statement

As far as we know, most of the available numerical models of GFET are physical models [13]. Such approaches provide high accuracy of the obtained results but in fact their integration into a circuit simulator could be problematic. It should be also noted, that level of physical models complexity is

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in general relatively high due to the significant number of complex mathematical formulas describing the model [14]. Moreover, these equations are often based on parameters which are quite difficult to obtain, thus the problem of model parameters extraction methods development appears [15]–[17]. Therefore, it is desirable to develop the GFET model based on parameters which could be easy extracted. Moreover, an "open structure" of the proposed model should enable easily implementation into widespread circuit simulators as well as its further modification and development.

In this paper the authors propose a behavioural model taking into account nonlinear steady-state characteristics and the parasitic capacitance. In contrast to physical models, the behavioural models allow to describe transistor "behavior" without considering the physical phenomena directly [18]. It means that in such an approach the modelled object is treated as a "black box" with only external terminals available. Models representing this category of approaches can be easily employed for further circuit simulations since the computational cost is reduced. It should be pointed out that the availability of parameters used in the behavioural models is much more higher than in the case of physical models. Moreover, procedures of parameters extraction for behavioural models are less complicated. The accuracy of behavioural models is usually lower than in the physical models but this kind of approach seems to be an attractive trade-off between the accuracy and total cost of model performance due to its lower complexity and higher availability of the parameters.

B. Solution

Behavioural modelling based on the general model of MOSFET is an effective tool and it can be successfully applied to develop the model of the graphene-based FET, too. In this approach the circuit model is composed of two essential components, namely, the one reflecting steady-state characteristics and the second one taking into account transistor capacitances which are important in the case of transient states simulations or estimation of the cut-off frequencies of GFET [17], [19]. Such model construction should guarantee satisfying accuracy with relatively low complexity. In the proposed model of GFET the authors made the following simplifications. Firstly, it is assumed that an operating point of the GFET device is placed in the first linear region of the output characteristic. Secondly, the gate-to-source voltage u_{GS} range should not include values from the vicinity of the Dirac voltage because of complex phenomena appearing for these voltages. For this reason it was decided to set a margin of 5V arround the Dirac voltage to be excluded from the analysis. Finally, thermal effects are not taken into account. All the listed assumptions enable to simplify the description of steady-state characteristics and allow to use a linear model of transistor capacitances.

Details of the authors' GFET behavioural model are shown in Fig. 2. As can be noticed from the diagram, the controlled current source I_T represents steady-state characteristics, whereas C_{GS} and C_{GD} denote linear parasitic capacitances. In contrast to the general MOSFET model, an influence of drain-to-source capacitance C_{DS} can be neglected in GFET [15]–[17].

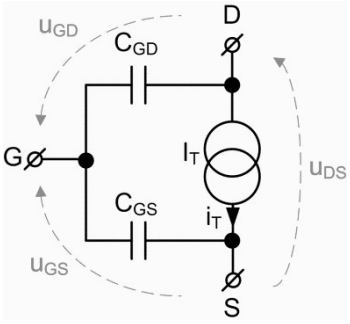

Fig. 2. Behavioural model of GFET

C. Modelling of steady-state characteristics

The current of the controlled current source I_T is expressed by:

$$i_T = i_D(u_{GS}, u_{DS}) + i_{DIR}(u_{DS}) \tag{1}$$

where $i_{DIR}(u_{DS})$ is defined as a transistor drain current for $u_{GS} = U_{DIR}$ and U_{DIR} is the Dirac voltage. The component $i_D(u_{GS}, u_{DS})$ is assumed to be the drain current for $|u_{GS}| > |U_{DIR}|$.

The drain current component $i_{DIR}(u_{DS})$ depends on the drain-to-source voltage:

$$i_{DIR}(u_{DS}) = I_{DIR(sat)}(e^{u_{DS}/\Delta U_{DS(DIR)}} - 1) \tag{2}$$

where $I_{DIR(sat)}$ is the transistor drain saturation current for $u_{GS} = U_{DIR}$ and $\Delta U_{DS(DIR)}$ is a constant of the curve. The $i_D(u_{GS}, u_{DS})$ component of I_T is expressed as a function of u_{DS} and u_{GS} voltages as follows:

$$i_D(u_{GS}, u_{DS}) = i_{D(sat)}(u_{GS}) \tanh[u_{DS}/\Delta U_{DS}(u_{GS})]. \tag{3}$$

In this equation $i_{D(sat)}(u_{GS})$ represents the transistor drain saturation current and $\Delta U_{DS}(u_{GS})$ denotes the width of the linear region of the steady-state $i_D(u_{DS})$ output characteristic. The coefficients $i_{D(sat)}(u_{GS})$ and $\Delta U_{DS}(u_{GS})$ depend on the gate-to-source voltage u_{GS}. It should be noted, however, that these values are not symmetrical in relation to the Dirac point U_{DIR} and therefore the following equations are formulated:

$$i_{D(sat)}(u_{GS}) = \begin{cases} i_{D_p(sat)}(u_{GS}) & u_{GS} < U_{DIR} \\ 0 & u_{GS} = U_{DIR} \\ i_{D_n(sat)}(u_{GS}) & u_{GS} > U_{DIR} \end{cases} \tag{4}$$

$$\Delta U_{DS}(u_{GS}) = \begin{cases} \Delta U_{DS_p(sat)}(u_{GS}) & u_{GS} \le U_{DIR} \\ \Delta U_{DS_n(sat)}(u_{GS}) & u_{GS} > U_{DIR} \end{cases} \tag{5}$$

Next:

$$\begin{aligned} i_{D_p(sat)}(u_{GS}) &= x_{1_p}\text{atan}[x_{2_p}|u_{GS} - U_{DIR}|] + \\ &+ x_{3_p}|u_{GS} - U_{DIR}| \end{aligned} \tag{6}$$

$$\begin{aligned} i_{D_n(sat)}(u_{GS}) &= x_{1_n}\text{atan}[x_{2_n}(u_{GS} - U_{DIR})] + \\ &+ x_{3_n}(u_{GS} - U_{DIR}) \end{aligned} \tag{7}$$

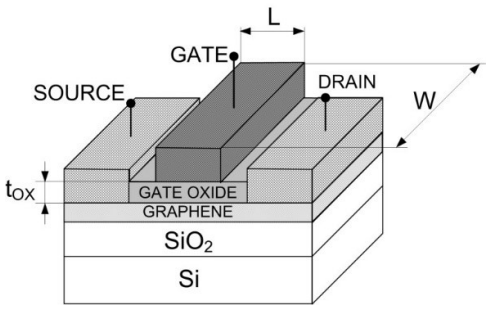

Fig. 3. Cross section of the modelled GFET

where: x_{1_p}, x_{1_n} – proportionality factor, x_{2_p}, x_{2_n} – transconductance in non-linear operating region, x_{3_p}, x_{3_n} – transconductance in linear operating region.

And similarly:

$$\Delta U_{DS_p(sat)}(u_{GS}) = y_{1_p}\{1 - \text{atan}[y_{2_p}|u_{GS} - U_{DIR}|]\} + + y_{3_p}|u_{GS} - U_{DIR}| \quad (8)$$

$$\Delta U_{DS_n(sat)}(u_{GS}) = y_{1_n}\{1 - \text{atan}[y_{2_n}(u_{GS} - U_{DIR})]\} + + y_{3_n}(u_{GS} - U_{DIR}) \quad (9)$$

where: y_{1_p}, y_{1_n} – saturation voltage at $u_{GS} = U_{DIR}$, y_{2_p}, y_{2_n}, y_{3_p}, y_{3_n} – proportionality factors.

D. Modelling of C_{GD} and C_{GS} capacitances

As it was reported in literature [13], [17], [19], significant non-linearity of the gate-to-source C_{GS} and gate-to-drain C_{GD} GFET capacitance characteristics is visible in the narrow range of voltages around the Dirac point. Except this voltages range, capacitances C_{GD} and C_{GS} can be regarded as linear, whose values strictly result from the top oxide capacitance C_{OX} [19]. Capacitance C_{OX} depends on the construction details of the transistor and it can be described similarly as for the classic MOSFET [20]:

$$C_{OX} = \frac{\varepsilon_0 \varepsilon_{SiO_2}}{t_{OX}} \quad (10)$$

where: ε_0 - dielectric constant of vacuum, ε_{SiO_2} - dielectric constant of SiO_2 ($3.97\varepsilon_0$) and t_{OX} is the thickness of oxide layer (Fig. 3). Hence, assuming construction symmetry of the considered GFET element, values of capacitances C_{GD} and C_{GS} can be calculated as follows:

$$C_{GS} = C_{GD} = \frac{C_{OX} W L}{2} \quad (11)$$

where W and L are construction parameters of the gate region.

E. Parameters extraction

Many different "handmade" graphene-based FET devices have been reported in literature so far. However, to the authors' best knowledge, the reliable ready-to-use commercial GFET devices, exhibiting stable parameters and reproducible characteristics, are still not available on the market. That is why the authors decided to extract the necessary parameters directly from the physical model. The GFET Tool program [12] enables simulation of electrical characteristics and thermal properties of top-gated graphene-based field-effect transistor on the basis of the drift-diffusion approach. The *I-V* characteristics could be calculated in the self-consistent manner for chosen temperatures and additionally temperature profiles, electron and hole densities and velocities in the graphene channel can be plotted by the use of this software for various parameters which could be altered by the user. Also, transistor thermal breakdown effect caused by the self-heating is included in the simulations. The spatial charge inhomogenity in the form of "puddles", which is provoked by the impurity contamination in the material, is taken into account, too. The set of parameters used for GFET Tool simulations is listed in Table I.

TABLE I
GFET TOOL INPUT PARAMETERS

Parameter	Value	Unit
Width (W)	10.0	μm
Length (L)	3.0; 10.0	μm
Initial temperature	298	K
Gate voltage (U_{GS})	-50 – +50	V
Dirac voltage (U_{DIR})	0	V
Maximum drain cureent (i_D)	10.0	mA
Drain current step	50	μA
Top gate oxide thickness (t_{OX})	10.0	nm
Mobility	3000	$cm^2/V \cdot s$
Breakdown temperature	873	K
Back gate oxide thickness	30.0	μm
Metal contact resistance	350	$\Omega \cdot \mu m^2$
Thermal conductivity of insulator (SiO_2)	1.3	$W/m \cdot K$
Thermal conductivity of wafer substrate (Si)	100.0	$W/m \cdot K$
Thermal conductivity of graphene	1000.0	$W/m \cdot K$

As mentioned above, the steady-state conduction characteristics described by equations (1) – (9) were adapted from output characteristics derived from the physical model simulations. Values of the coefficients $i_{DIR}(u_{DS})$ and $\Delta U_{DS(DIR)}$ basing on the output $i_D(u_{DS})$ characteristic obtained for $u_{GS} = U_{DIR}$ have been calculated. For this purpose the authors carried out a fitting procedure with the use of *fminsearch* function in MATLAB/OCTAVE programs taking the sum of square deviation as the main criterion. Next, basing on the equations (1) – (3), transistor output $i_D(u_{DS})$ characteristics were obtained for the wide range of voltages u_{GS} and the relationship between $i_{D(sat)}(u_{GS})$ and $\Delta U_{DS}(u_{GS})$ was determined using *fminsearch* function. Similarly, when relations $i_{D(sat)}(u_{GS})$ and $\Delta U_{DS}(u_{GS})$ had been estimated, the authors calculated values of coefficients $x_{1_p} \ldots x_{3_p}, x_{1_n} \ldots x_{3_n}, y_{1_p} \ldots y_{3_p}, y_{1_n} \ldots y_{3_n}$ from equations (6) – (9). The values of C_{GD} and C_{GS} capacitances were calculated using equations (10) – (11).

In the next step, the GFET behavioural model was implemented into the SABER simulator.

TABLE II
BEHAVIOURAL MODEL PARAMETERS FOR $W \times L$= $10\mu m \times 3\mu m$ GRAPHENE CHANNEL GEOMETRY

Parameter	Value	Unit
C_{GS}	52.7	fF
C_{GD}	52.7	fF
$I_{DIR(sat)}$	5.801	mA
$\Delta U_{DS(DIR)}$	3.7607	V
U_{DIR}	0	V
x_{1_p}	10.0807	–
x_{2_p}	0.1014	S
x_{3_p}	0.3621	mS
x_{1_n}	9.3431	–
x_{2_n}	0.1850	S
x_{3_n}	0.3944	mS
y_{1_p}	1.8779	V
y_{2_p}	4.0585	1/V
y_{3_p}	1.8828	–
y_{1_n}	1.8587	V
y_{2_n}	1.3044	1/V
y_{3_n}	1.9020	–

TABLE III
BEHAVIOURAL MODEL PARAMETERS FOR $W \times L$= $10\mu m \times 10\mu m$ GRAPHENE CHANNEL GEOMETRY

Parameter	Value	Unit
C_{GS}	175.7	fF
C_{GD}	175.7	fF
$I_{DIR(sat)}$	5.801	mA
$\Delta U_{DS(DIR)}$	3.7607	V
U_{DIR}	0	V
x_{1_p}	13.3347	–
x_{2_p}	0.0613	S
x_{3_p}	0.1173	mS
x_{1_n}	8.9395	–
x_{2_n}	0.1995	S
x_{3_n}	0.2144	mS
y_{1_p}	0.9031	V
y_{2_p}	0.1067	1/V
y_{3_p}	1.2983	–
y_{1_n}	1.7900	V
y_{2_n}	0.1428	1/V
y_{3_n}	1.7494	–

III. RESULTS

It is well known, that in the majority of transistor models numerical values of parameters depend on the channel geometry. In other words, one cannot use the same parameters for different $W \times L$. In this work GFETs with $10\mu m \times 3\mu m$ and $10\mu m \times 10\mu m$ graphene channels were tested to check the "flexibility" of the proposed model. All the determined parameters of the behavioural model are collected in Table II and Table III, whereas the results of comparison between the physical and the behavioural model simulations of steady-state characteristics are presented in Figs. 4, 5, 6 and 7.

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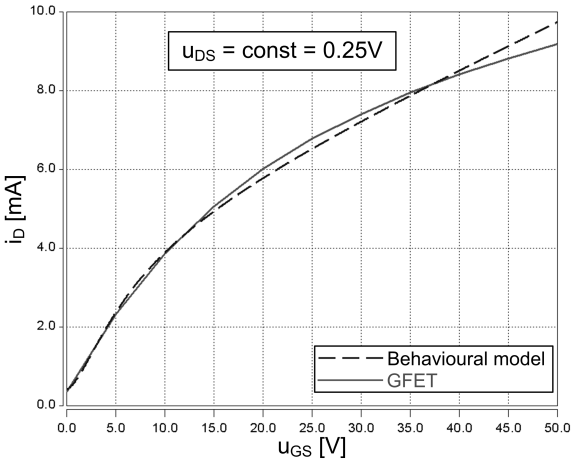

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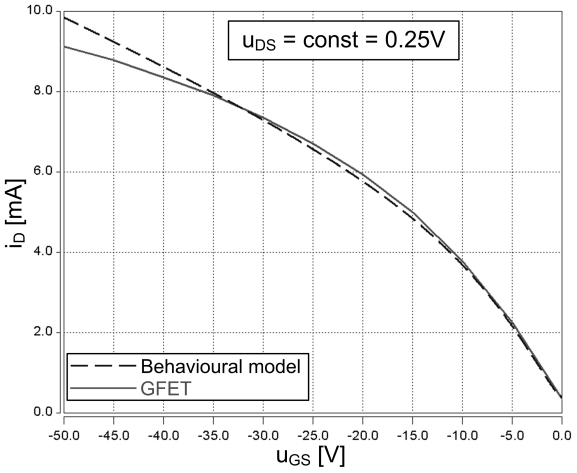


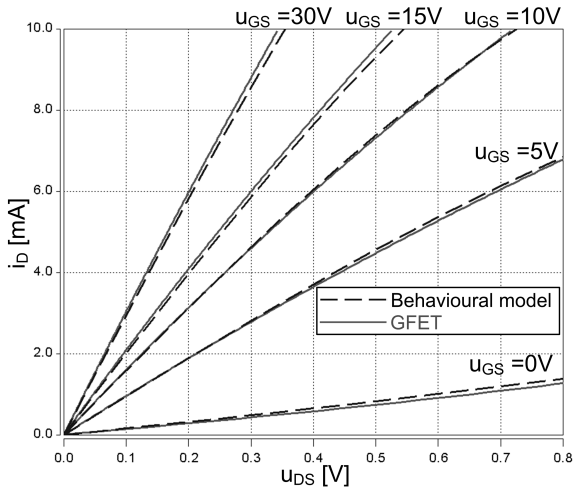
Fig. 4. Steady-state transfer characteristics from the physical model (GFET) and the behavioural model for $W \times L$= $10\mu m \times 3\mu m$ graphene channel geometry for a) $U_{GS} > 0$ and b) $U_{GS} < 0$

It is apparent that the GFET transfer characteristic $i_D(u_{GS})$ is different than the typical one for MOSFET (Figs. 4 and 6). The threshold voltage is not recognized and thus GFET element is in the conduction state no matter what the u_{GS} voltage value is [1]. The i_D current is minimal for the Dirac voltage.

The GFET output $i_D(u_{DS})$ characteristics are similar to the typical FET $I - V$ curves (Figs. 5 and 7). It can be assumed, that in the considered u_{DS} voltage range the GFET device operates in a triode mode. A small saturation occurs with increasing u_{DS} voltage. However, the observed drain saturation current results from the gate-to-source voltage, what is a characteristic feature of all types of field-effect transistors.

The steady-state characteristics obtained from the behavioural model simulations exhibit satisfying accuracy for the both studied geometries. The drain saturation current as well as nonlinearity of the characteristics were properly reproduced. Also, the asymmetry with respect to the Dirac point was

a)



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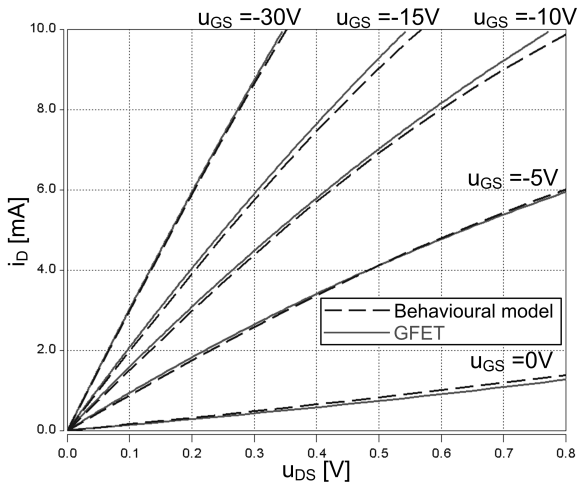
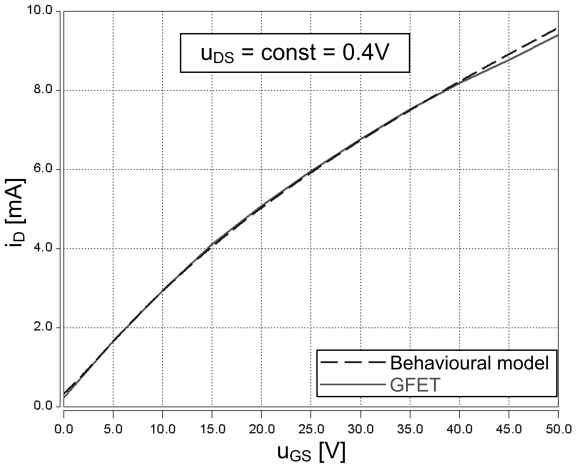


Fig. 5. Steady-state output characteristics from the physical model (GFET) and the behavioural model for $W \times L = 10\mu m \times 3\mu m$ graphene channel geometry for a) $u_{GS} \geq 0V$ and b) $u_{GS} \leq 0V$

a)



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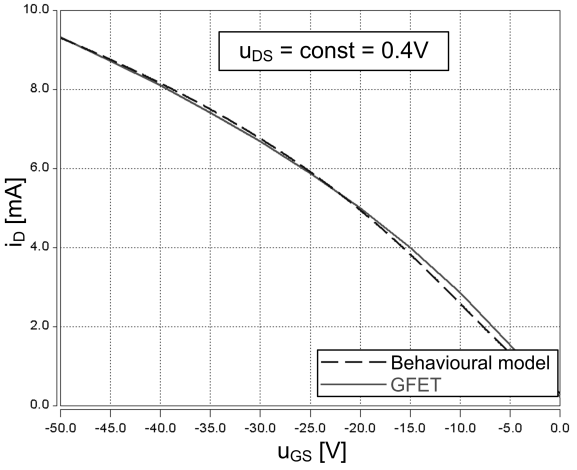

Fig. 6. Steady-state transfer characteristics from the physical model (GFET) and the behavioural model for $W \times L = 10\mu m \times 10\mu m$ graphene channel geometry for a) $U_{GS} > 0$ and b) $U_{GS} < 0$

modelled correctly for the considered range of gate-to-source u_{GS} and drain-to-source u_{DS} voltages.

IV. Conclusions

Semiconductor device modelling plays a very important role in the modern industry. It is clear that the model of transistor should reproduce its physical properties as precisely as possible. On the other hand, there is plenty of transistors in the integrated circuits and the computational cost of the simulation could be very high when all the unit devices are described by the complicated physical transistor model. There are lots and lots of advantages to using physical models for the electronic device studies. An ideal physical model should allow for understanding and correct interpretation of experimentally obtained characteristics of the investigated element. What is more, it should enable to predict the influence of construction details modification on the overall behaviour of the device, calculate theoretical values of different parameters, etc. The problem is, however, that construction of such a perfect physical model, i.e. the one taking into consideration all important physical phenomena, is practically impossible, mainly because of the natural complexity of the physical processes taking place in the real element and sometimes the lack of precise mathematical description. Therefore, some essential simplifications are always necessary to be assumed. Moreover, it is a very common practice to tune the physical models by introducing additional (and most often arbitrarily chosen) parameters to improve the accuracy of the initial approach. In some sense, this kind of solution could be treated as a mixed variant, that is, the combination of a physical model (based on physical principles and appropriate mathematical equations) and a ”black box” type model (based only on empirical equations). In this context, the issue of preparation of compact models which could guarantee the

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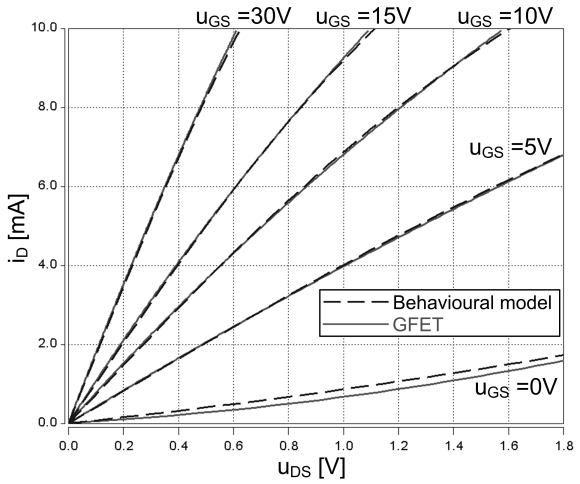

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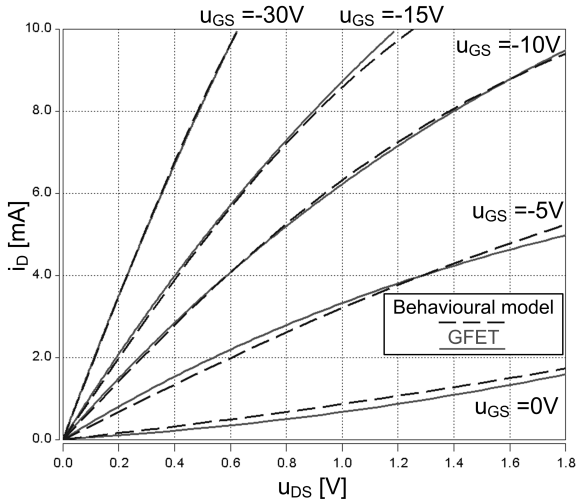

Fig. 7. Steady-state output characteristics from the physical model (GFET) and the behavioural model for $W \times L = 10\mu m \times 10\mu m$ graphene channel geometry for a) $u_{GS} \geq 0V$ and b) $u_{GS} \leq 0V$

sufficient efficiency and accuracy of the calculations seems to be crucial.

In this paper the behavioural model of graphene field-effect transistor is proposed. The authors' model is defined by a relatively small number of equations, which are not nested, and all the parameters can be easily extracted for chosen W and L dimensions. It was demonstrated that the presented approach allows to reproduce the steady-state GFET characteristics for different graphen channel geometries with good accuracy. The authors are aware, however, that in the future the procedure of parameters extraction should be performed with the use of a high-quality real GFET element, if only available. Even though, the proposed model neglects some important effects (e.g. the impact of temperature), it can be a good starting point to develop more advanced versions.

In conclusion, further intensive work is still necessary to develop and validate the model of graphene field-effect transistor. The authors' compact GFET model can be used for circuit or system-level simulations for various sensor applications in the future.

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