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A 1.67 pJ/Conversion-step 8-bit SAR-Flash ADC Architecture in 90-nm CMOS Technology

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***Abstract*—A novice advanced architecture of 8-bit analog to digital converter is introduced and analyzed in this paper. The structure of proposed ADC is based on the sub-ranging ADC architecture in which a 4-bit resolution flash-ADC is utilized. The proposed ADC architecture is designed by employing a comparator which is equipped with common mode current feedback and gain boosting technique (CMFD-GB) and a residue amplifier. The proposed 8 bits ADC structure can achieve the speed of 140 mega-samples per second. The proposed ADC architecture is designed at a resolution of 8 bits at 10 MHz sampling frequency. DNL and INL values of the proposed design are -0.94/1.22 and -1.19/1.19 respectively. The ADC design dissipates a power of 1.24 mW with the conversion speed of 0.98 ns. The magnitude of SFDR and SNR from the simulations at Nyquist input is 39.77 and 35.62 decibel respectively. Simulations are performed on a SPICE based tool in 90 nm CMOS technology. The comparison shows better performance for this proposed ADC design in comparison to other ADC architectures regarding speed, resolution and power consumption.**

***Keywords*—Analog to Digital Converter (ADC), Successive Approximation Register(SAR), Common Mode Current Feedback Gain Boosting (CMFD-GB), Residue Amplifier(RA), Spurious-free dynamic range (SFDR), Integral Non-Linearity (INL), Differential Non-Linearity (DNL)**

I. Introduction

DATA converter circuits are one of the crucial and integral components of the electronics domain as it is through these devices that an interface is established between analogous and digital world [1]. Almost every field of electronic domain entails the services of these data converters by cautiously stipulating their specific parameter [2], [3]. Various applications necessitate different features, for example, biomedical applications need very high accuracy ADC which dissipates limited power with small die area while the ADC utilized in digital communication demands extremely high speed of conversion [4], [5]. Portable electronic and multimedia systems devices operating on batteries require extra energy potent ADCs with full bandwidth. Initially, the conventional ADCs are designed by only considering their conversion speed. These conventional fast ADCs suffer from the issues like high parasitic capacitance and large power dissipation which ultimately makes them least applicable in the shallow power ultra-deep sub-micron range [6], [7]. To cope up with these specific requisites, the designers of these data converters should cautiously design and fabricate these devices by considering the factors like speed, resolution, accuracy and power [8].

Successive approximation register (SAR), flash, sigma-delta and pipelined are the most prevalent ADC architectures that are frequently employed in various electronics fields [9]. Applications which necessitates high operation speed employs flash and pipelined ADCs structure while the applications which entail very high resolution with optimum power dissipation utilize sigma-delta ADC [10], [11]. The predominant among these architectures is successive approximation register ADC (SAR). Its broad applicability lies in the fact of its architectural simplicity and mid resolution range with moderate power utilization. However, ADC (SAR) is slightly unfit for the applications which require very high speed with high resolution [12], [13]. The count of significant components like comparators, encoders/decoders, pre-amplifiers, registers increases exponentially as the designers go for higher resolution and fast speed [14], [15].

A reinvigorate advanced architecture of 8-bit ADC is proposed and endowed in this work. The proposed structure is simulated with the comparator employing gain boosting technique with common mode current feedback (CMFD-GB) [16], [17]. A residue amplifier is employed for improving the signal strength inside the segmented DAC capacitor rail [18]. Simulations on the proposed 8-bit ADC structure are then executed in 90 nanometres CMOS technology at supply voltages of 0.7 volts. The results are recorded and compared at different channel lengths and different temperatures. Results for the proposed design with CMFD-GB comparator shows the excellent speed with stable linearity (DNL and INL) values with slightly more power exhaustion.

The further assemblage of the paper is as follows. The details regarding the composition of the architecture with the significant components of proposed 8-bit ADC is exemplified in the next segment. Thereafter the recorded results and their analysis are presented. The comparison and conclusion are then given in the end with references.

II. Circuit Description

Figure 1 represents the comprehensive structure of the proposed 8-bit ADC. This proposed architecture is carved out

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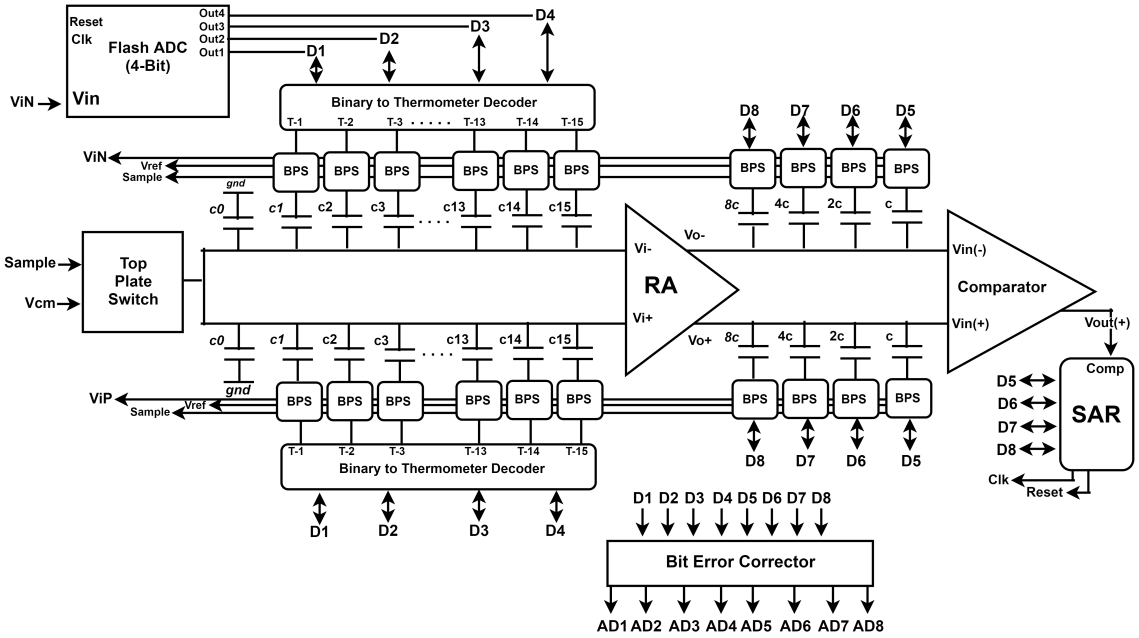

Fig. 1. Architecture of proposed 8-Bit Analog To Digital Converter

by coalescing a flash-ADC with a SAR-ADC. High-speed of flash-ADC and low power and good resolution of SAR-ADC is exploited by this proposed ADC design [19], [20].The flash-ADC is designed in a cosy manner for achieving high speed in the proposed design. On the cost of mild high power consumption and circuit complexity higher sampling speed is attained through this proposed design as compared to the general SAR-ADC structure. The initial conversion is executed by flash-ADC which determines top most significant bits and reduce the range which easily get converted through segmented DAC. The segmented DAC architecture constitute of two section where first is associated with flash-ADC and second with SAR. An equal strength of the signal is maintained by appropriately adjusting a residue amplifier in between these two sections [18]. This initial phase reduces the

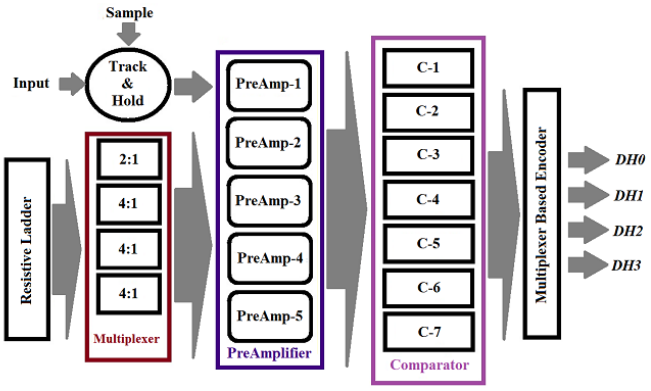

Fig. 2. Architecture of a flash ADC (4-Bit).

input voltage range for SAR-ADC which effectively performs the rest of the task. The significance of the proposed ADC architecture includes good resolution and optimum power consumption with improvements in speed and accuracy [19], [20], [21]. The complete block architecture of flash-ADC having a four-bit resolution is represented in figure 2 [3], [22]. The composite structure of flash ADC of 4-bit resolution incorporates one Track and hold circuit, a resistance ladder for reference voltage, five differential Pre-amplifiers, seven comparators, three 4:1 and one 2:1 multiplexer with one multiplexer-based encoder at the output segment. The track and hold, pre-amplifier, half adder and multiplexer blocks are structured by utilizing complementary MOS technology [23], [24].

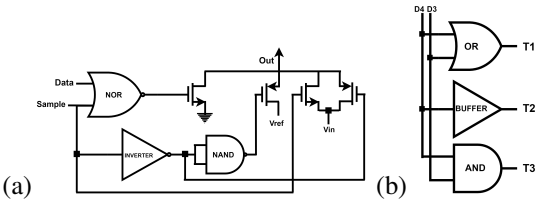

Fig. 3. (a) Bottom plate switch (b) 2-Bit Binary to Thermal Decoder.

It is through this top plate switch the capacitor rail get charged to the respected references. The structure of the bottom plate switch is detailed in figure 3(a). A 4-bit binary to thermal decoder is utilized in the proposed design. For simplification figure 3(b) illustrates the schematic of the 2-bit binary thermal decoder (BTD) circuit [25].

The comparator and DAC are classified as an essential and significant component in analog to digital data converter circuits [26]. Comparator equipped with common-mode feedback (current) with gain boosting techniques (CMFD-GB) is utilized for designing the ADC architecture [17], [27]. Figure 4(a) illustrates the entire construction of the comparator (CMFD-GB) structure employed in designing this proposed 8-bit ADC

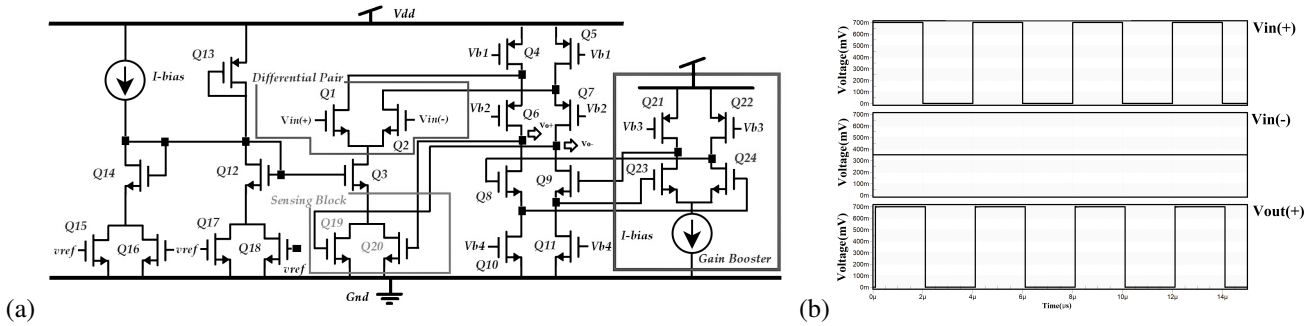

Fig. 4. (a) Design of CMOS CMFD-GB comparator. (b) Comparator waveforms.

circuit. The comparator is designed by utilizing the current mode feedback along with gain boosting technology [17], [28], [29]. An additional gain boosting block is attached at the output segment which ultimately enhance the output gain. The output waveforms of the comparator is depicted in figure4(b). A residue amplifier is employed for maintaining the equal signal strength through out capacitor rail in the segmented DAC. The utilization of 4-bit BTD has subsequently increases the

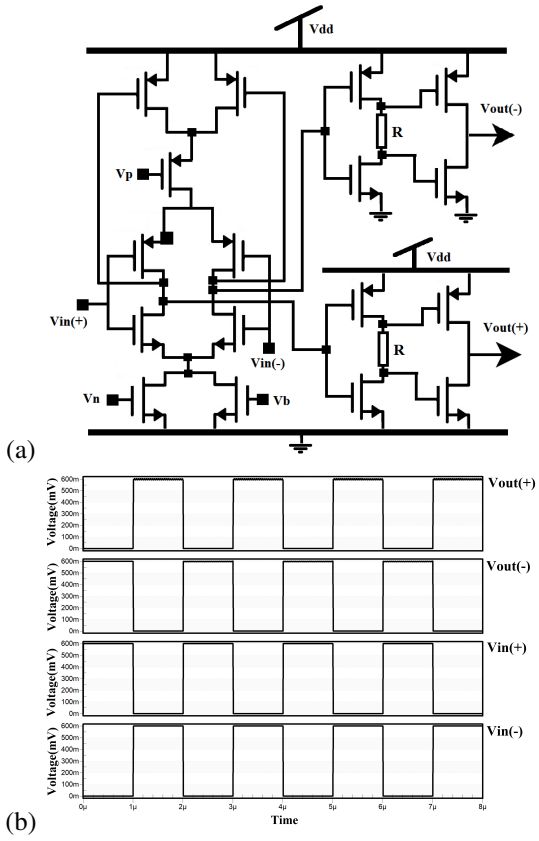

Fig. 5. (a) Residue Amplifier. (b) Input and output waveforms.

capacitor count in the capacitor rail which in turn decrease the signal strength as it travel to the comparator input. Thus the need of residue amplifier arises as it effectively maintain the signal strength in the capacitor rail which leads to correct ADC conversion [30], [31]. Figure 5(a) illustrates the schematic of the residue amplifier and figure 5(b) shows its corresponding waveforms. Figure 6 delineates the block level structure of a

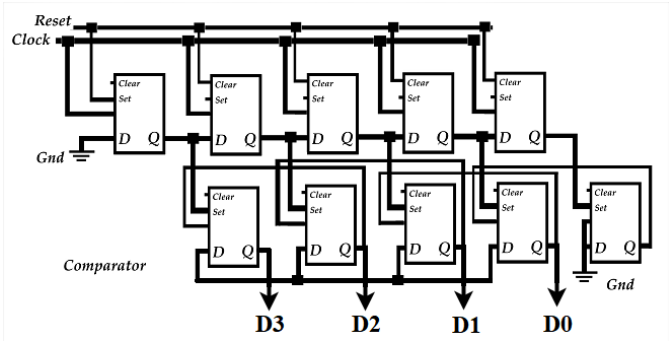

Fig. 6. Successive Approximation Register.

successive approximation register (SAR). This SAR structure constitutes of 10 delay type flip-flops which are in two rails one above the other. SAR block provides an interface between comparator and bottom plate switches [32].

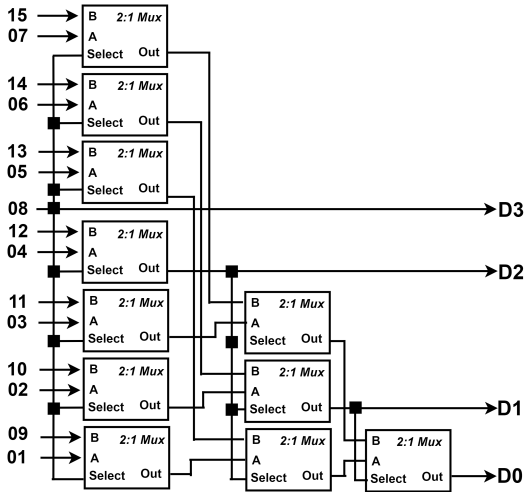

Fig. 7. Mux Based Encoder.

An encoder which utilizes multiplexers for encoding the output bits of flash ADC (4-bit) is illustrated in figure7. It is present in the last segment of flash ADC (4-bit) which is a significant block of the proposed ADC structure. Eleven 2:1 multiplexer

is deployed for structuring its architecture. A error bit corrector is utilized at the the output segment of proposed ADC which is illustrated in figure 8. It comprises of 7 half adders which are designed in CMOS technology. It helps in removing the redundancy in the ADC output bits [33], [34].

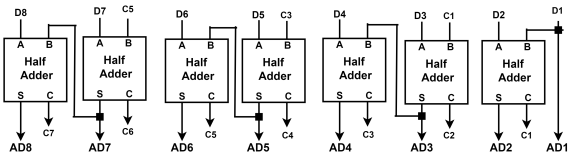

Fig. 8. Bit error corrector.

III. Results

The results of the proposed 8-bit ADC design are observed, recorded and analyzed in this section. Transient and AC analysis is executed on the proposed design by varying the performance parameters with Monte Carlo simulations techniques at 0.7 V supply voltage with 10 megahertz sampling frequency. Ideally, 90 nanometres channel-length and 1 µm

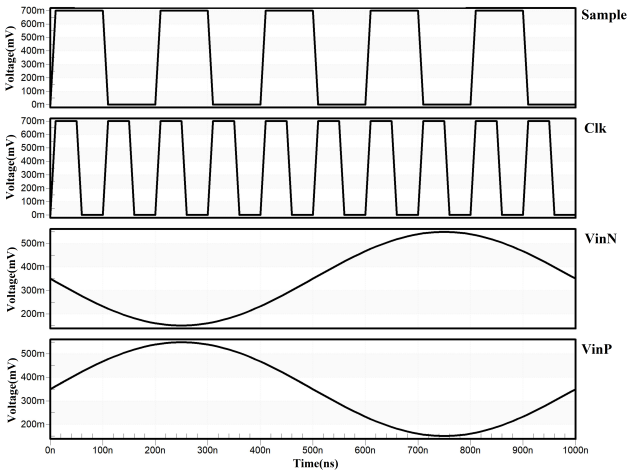

Fig. 9. Input waveforms.

channel-width are deployed as the MOS devices dimension. Figure9 illustrates the input waveforms of proposed ADC design and the corresponding output waveforms are shown in figure 10.

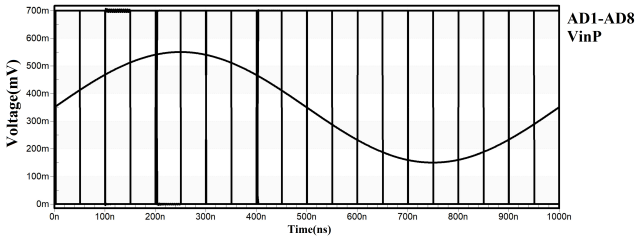

Fig. 10. Seven-bit output waveforms.

Table I illustrates the power dissipation and the conversion speed of the proposed ADC architecture at different channel-width. An alteration of 1 µm to 4 µm in the channel-width is done and then the variations in the parameters are recorded.

TABLE I
Power consumption (PC) and conversion time (CT) at different channel-widths (W)

W(µm)	PC (mW)	CT (ns)
1.0	1.24	0.98
1.5	1.74	43.31
2.0	2.41	100.72
2.5	2.89	101.15
3.0	3.43	101.16
3.5	5.17	101.01
4.0	5.46	100.26

The proposed ADC architecture dissipates maximum power of 1.24 mW at 1µm channel-width with the conversion time of 0.98 ns. Table II displays the alteration in power consumption, current drawn(maximum) and the conversion speed at different temperatures. The temperature is altered from 20° C to 50° C

TABLE II
Power consumption (PC), current drawn (CD), conversion time (CT) at different temperatures

Temp	PC (mW)	CD (mA)	CT (ns)
20°	1.33	1.90	0.39
25°	1.24	1.77	0.98
30°	1.17	1.67	0.66
35°	1.11	1.59	0.63
40°	1.52	2.17	0.45
45°	1.48	2.12	0.74
50°	1.31	1.88	0.99

and then the disparities in the parameters are recorded. The proposed architecture draws a minimum current of 1.59 mA by consuming the power of 1.11 mW at 35° C with the conversion

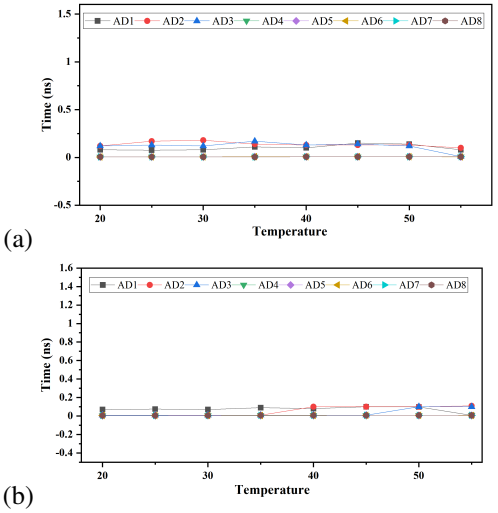

Fig. 11. (a)) Rise time (ns) (b) Fall time (ns).

speed of 0.63 ns. The maximum current of 2.17 mA is drawn

at 40° C while dissipating the power of 1.52 mW with a conversion time of 0.45 ns. Figure 11 (a) and (b) demonstrates the time duration of the rising edge and falling edge of the seven output bits of the proposed ADC architecture at different temperatures. The temperature is varied from 20° C to 55° C. A stable pattern of time duration for all seven output bits is

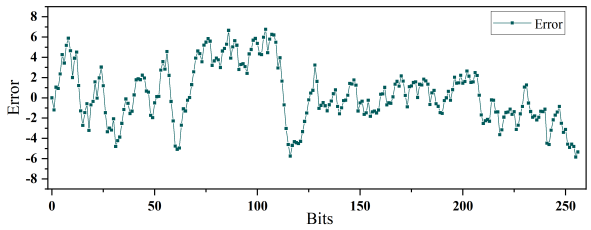

Fig. 12. Calculated error.

observed after simulations. The typical range for the rise time and fall time lies within 0 to 1 nanosecond. Figure12 depicts the magnitude of error which is calculated by subtracting the calculated values from the observed. The error lies within the range of -5.83 to 6.76.

$$DNL = [(V_i + 1 - V_i)/V_lsb] - 1 \quad (1)$$

$$INL = [[V_i - V_0]/V_lsb(ideal)] - i \quad (2)$$

Equation1 and 2 are utilized for calculating differential non-linearity (DNL) and integral non-linearity (INL) values of the proposed ADC. Figure 13 represents the DNL values for

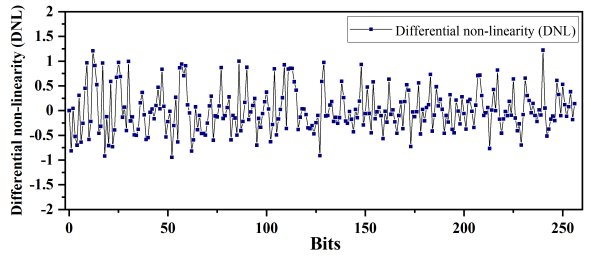

Fig. 13. DNL values for proposed ADC architecture.

the proposed architecture. The maximum and minimum DNL values for the proposed design is 1.22 and -0.94 respectively.

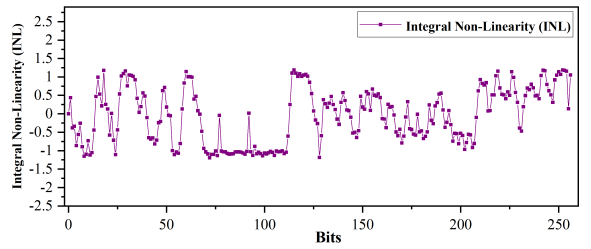

Fig. 14. INL values for proposed ADC architecture.

Figure 14 delineates the INL values which have maximum and minimum values of 1.19 and -1.19 respectively. The FFT plot for the input of 5 megahertz sampled at the rate of 70 MHz

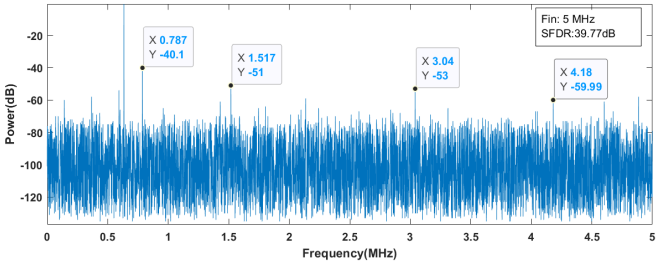

Fig. 15. FFT plot for a 5 MHz input signal at 70 MHz.

is illustrated in figure 15. The calculated magnitude of SFDR and SNR from the simulations at Nyquist input is 39.77 and 35.62 decibel respectively. The variations in the SFDR with

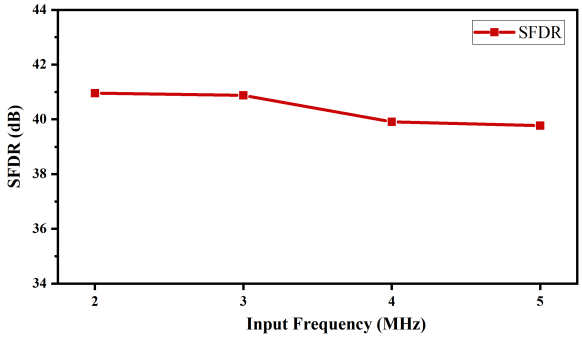

Fig. 16. SFDR at different input frequency.

respect to the input signal frequency is shown in figure 16. It is distinctively observed that the increase in input signal frequency reduces the SFDR magnitude. Figure 17 shows the variations in current drawn, power consumption and conversion time at four process corners (FF, SS, FS, SF).

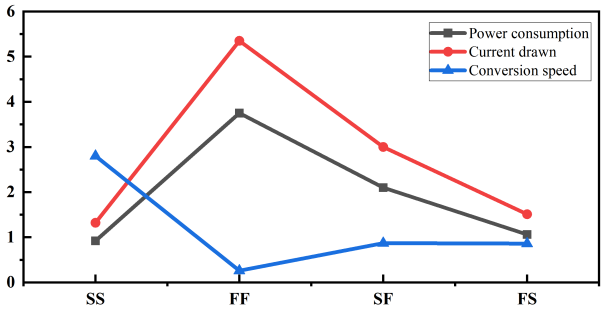

Fig. 17. Power consumption, current drawn and conversion time vs four process corner. .

The proposed ADC design attains 6.21 ENOB at 5 MHz input. The ENOB is calculated through equation3.

$$ENOB = (SINAD - 1.76dB)/6.02 \quad (3)$$

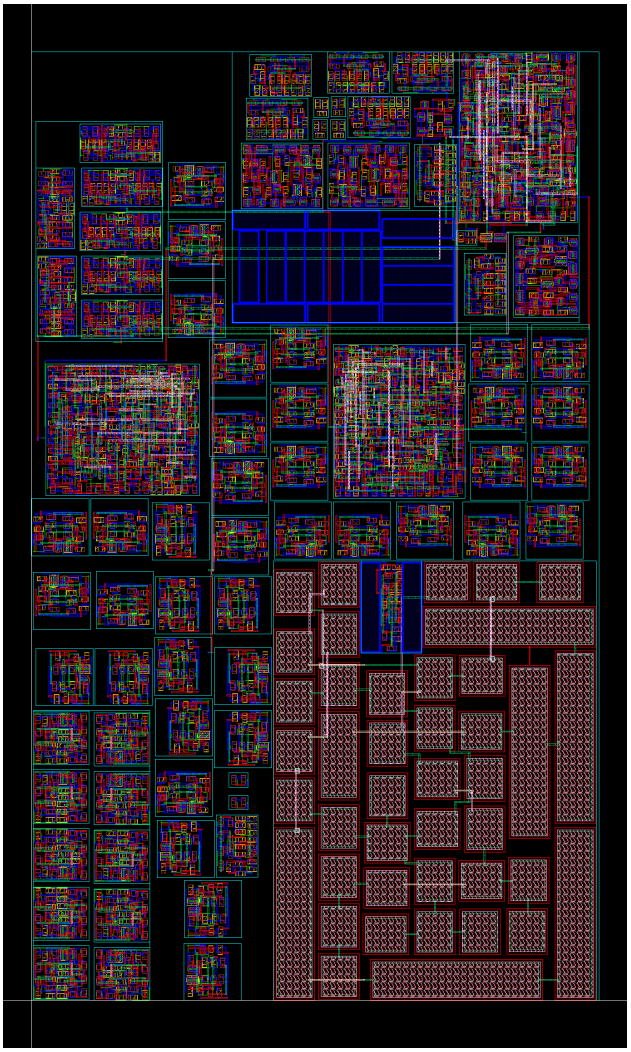

Fig. 18. Layout of the proposed ADC .

Layout and the placement of the individual blocks of the proposed 8-bit ADC are clearly illustrated figure18.The layout length and height are 74.5µm and 92.4 µm respectively which gives the total area occupation of 6883.8 µm square for the proposed ADC. Table III recapitulates the performance excellence of the proposed ADC architecture.The accomplishment and significance of the proposed ADC architecture are detailed in IV by comparing other states of the art ADC's.

IV. Conclusions

A 8-bit analog to digital converter architecture is proposed and investigated in this paper. Results show improvements regarding to resolution, linearity, speed and power consumption. The proposed design when simulated with CMFD-GB comparator in 90 nm CMOS technology shows optimum power dissipation of 1.24 mW at 0.7 V supply voltage. The maximum/minimum values of DNL and INL measured at nyquist input are -0.94/1.22 and -1.19/1.19 respectively. The SFDR and SNR values at Nyquist input is 39.77 and 35.62 decibel respectively. The ENOB and Figure of merit value at

TABLE III
Results summary of proposed ADC architecture

Temperature	25°
Design technology	CMOS
Resolution	8 Bit
MOSFET Count	1945
Channel-Length(nm)	90
Supply voltage (V)	0.7
Power consumption(mW)	1.24
Conversion time (ns)	0.98
Sampling frequency (mega-Hz)	10
Speed (mega-samples/ sec)	140
DNL	-0.94/1.22
INL	-1.19/1.19
SFDR (dB)	39.77
SNR (dB)	35.62
ENOB	6.21
FOM (pJ/step)	1.67

10 megahertz sampling frequency is 6.21 and 1.67 pJ/step. The sensitivity of the proposed design is further evaluated by simulating the proposed design at different temperatures where the observations shows the least variations for power consumption and conversion time. With these parametric values along with the abilities of calibration the proposed ADC architecture find a perfect space in Ultra Deep Submicron technologies where low- power, high-speed along with accuracy are significant factors for design.

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Conflicts of interest/Competing interests

There is no conflict of interest among the authors regarding to the publication of this paper.

Availability of data and material:

The data used to support the findings of this study are included within the paper.

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TABLE IV
COMPARISON

	Technology CMOS (nm)	Supply voltage (V)	Resolution (Bits)	Power consumption	Speed
[35]	65	1.0	10	18.9 mW	1 GS/s
[36]	180	1.2	6	20 mW	2.3 GS/s
[37]	180	1.8	10	5.0 mW	50 Ms/s
[38]	180	1.8	10	5.23 mW	100 Ms/s
[39]	180	0.4	10	30.4 nW	10-Ks/s
[40]	180	1.8	12	10.08 mW	50-Ms/s
[41]	180	3	10	590 µW	1-Ms/s
Proposed ADC	90	0.7	8	1.24 mW	140-Ms/s

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