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AN ARBITRARY WAVEFORM SYNTHESIS STRUCTURE WITH HIGH SAMPLING RATE AND LOW SPURIOUS

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Abstract

The arbitrary waveform generator is characterised by its flexible signal generation, high frequency resolution and rapid frequency switching speed and is wildly used in fields like communication, radar systems, quantum control, astronautics and biomedicine. With continuous development of technology, higher requirements are placed on to the arbitrary waveform generator. Sampling rate determines the bandwidth of the output signal, spurious-free dynamic range determines the quality of generated signal. Due to above, these two indicators' improvement is vital. However, the existing waveform generation methods cannot generate signals with quality good enough due to their technical limitations, and in order to realize a high system sampling rate, to accomplish waveform generation process in FPGA, multipath parallel structure is needed. Therefore, we proposed a parallel waveform synthesis structure based on digital resampling, which fixed the problems existing in the current methods effectively and achieved a high sampling rate as well as high quality arbitrary waveform synthesis. We also built up an experimental test bench to validate the proposed structure.

Keywords: arbitrary waveform generator, high sampling rate, low spurious, digital resampling, parallel structure.

1. Introduction

Arbitrary waveform generator (AWG) is a type of signal source that can flexibly generate various kinds of waveform signals according to user's need, it plays an important role in multiple fields like radar tests, communication, quantum control, astronautics, biomedicine and so on. For example, in the fifth generation of wireless communications (5G), Veyrac *et al.* applied the arbitrary waveform synthesis to the 5G handset transmitter [1]. In a radar test system, it can generate noise waveform for reference, signal detection and analog process [2]. In quantum control, Bowler *et al.* designed a multi-channel arbitrary waveform generator to process ion-based quantum information [3]. As for astronautics, it can be applied to chirp-transform spectrometer for planetary system research [4]. In biomedical field, the waveform signals generated by AWG can be used for ion isolation, excitation and ejection in mass spectrometers for biomolecular analysis [5].

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However, with the continuous improvement in electronic technology, higher requirements are placed on the AWG such as high bandwidth and high *spurious-free dynamic range* (SFDR) [6–8]. The only way to increase the bandwidth of an AWG is to synthesize waveforms in parallel through multiple DACs and now there are two structures available: *band interleaving digital-to-analog converter* (BI-DAC) and *time interleaving digital-to-analog converter* (TI-DAC). The two structures can be used to break through the DAC's performance limitation and increase the bandwidth of output signal [9, 10]. In recent years, there have been a large number of researches on BI-DAC and TI-DAC, and progress has been made in increasing the bandwidth of the AWG [9, 11–17].

SFDR is affected by the performance of the DAC and the synthesis method. At present, the SFDR of a DAC with high speed (1GSPS) can be as high as 80dBc [18]. However, the current digital waveform synthesis method brings redundant spectrum components due to technical limitations, which reduces the SFDR of output. In *direct digital frequency synthesis* (DDFS), due to the system sampling clock being fixed, in order to gain higher frequency resolution we need to increase the number of the the bits of the phase accumulator and this unfortunately brings in phase truncation error. Cordesses proposed some methods to reduce the influence of the phase truncation error on SFDR, including increasing the capacity of the waveform memory, the odd-number approach, the phase-dithering approach, and the noise-shaping approach [19, 20]. Although these methods expand SFDR to a certain extent, they still have limitations. The first method is limited by the performance of the memory, the odd-number approach can only improve the SFDR by 3 dB, the phase-dithering approach and the noise-shaping approach will increase noise floor. In [21], Zhang *et al.* proposed a design and FPGA implementation of a *direct digital synthesis* (DDS) based on waveform compression and the Taylor series, the SFDR can reach 114 dB. DDFS has a feature that it needs to read the samples from the memory at equal intervals according to the frequency control word. It makes DDFS impossible to use high-speed *synchronous dynamic random access memory* (SDRAM) which limits the realization of the high sampling rate.

Direct digital waveform synthesis (DDWS) changes the frequency of the output waveform by changing the sampling rate of the DAC, so the samples are read from the memory point by point. It makes the DDWS be the best choice for high sampling rate arbitrary waveform synthesis. Meanwhile, the variable sampling rate also makes the image components hard to be suppressed by a low-pass filter with a fixed cut-off frequency. Therefore, in order to achieve an arbitrary waveform synthesis method with a low spurious signal, we propose a parallel structure based on digital resampling. We devide the waveform synthesis process into digital waveform synthesis and digital-to-analog conversion. In the digital waveform synthesis part, we use a variable sampling clock and select suitable sampling clock according to the output signal's feature as well as to avoid phase truncation. In the digital-to-analog conversion part, in order to restrain the range of the image components, the DAC's sampling rate will be fixed. To ensure the match of the two parts' rate, we use a digital resampling module to realize sampling clock conversion. As the rate inside FPGA can only be hundreds of MHz, we need to process sample points via a parallel method to increase the rate, but the sample rate conversion module requires irregular interpolation of the input sample points and this cannot be achieved with the traditional multipath parallel method. Thus, we propose a structure for implementing digital resampling in multiplexed parallelism within FPGA, providing a high sampling rate for the system and ensuring a low spurious signal in the meantime. In Section 2, we present the limitations of the DDWS. In Section 3, we introduce our new method based on digital resampling and its implementation in the parallel structure. Finally, we give experimental results, proving that the digital waveform synthesis method based on digital resampling can effectively generate waveform with a low spurious signal.

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2. Current arbitrary waveform synthesis methods

For complex high-speed arbitrary waveforms, on-site sampled waveforms, and occasional waveforms, the DDWS is more suitable as this type of waveform usually requires the synthesis system to be able to output waveform samples point by point, and the system's rate is variable. The structure diagram of the DDWS is shown in Fig. 1. It consists of a variable clock generator, an address generator, a waveform lookup table, a DAC, and a low-pass filter. Under the control of the sampling clock, the output values of the address generator are incremented one by one. Then the waveform lookup table exports the stored waveform data to the DAC in a sequence.

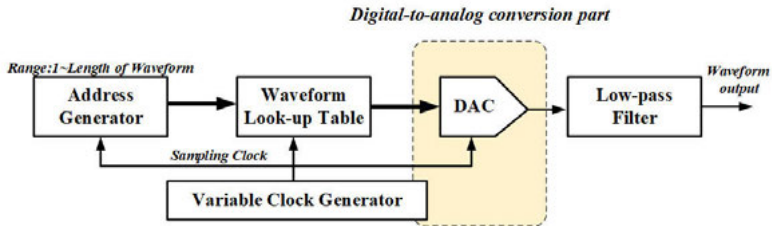

Fig. 1. Structure diagram of DDWS.

In the DDWS, the waveform samples are read sequentially in the order of storage, so there is no phase truncation error. The output waveform frequency is determined by the sampling clock frequency and the waveform period length:

$$f_o = \frac{f_s}{N\_\text{length}}, \tag{1}$$

where, N_length is the number of samples of a complete waveform.

However, the variable sampling rate of the DDWS also leads to a problem that the image components are difficult to suppress. In the digital sampling process, the image components exist at $f_s - f_o$ [22], so it an low-pass filter is needed with a cut-off frequency of $f_s/2$ to filter out the image components, as shown in Fig. 2a.

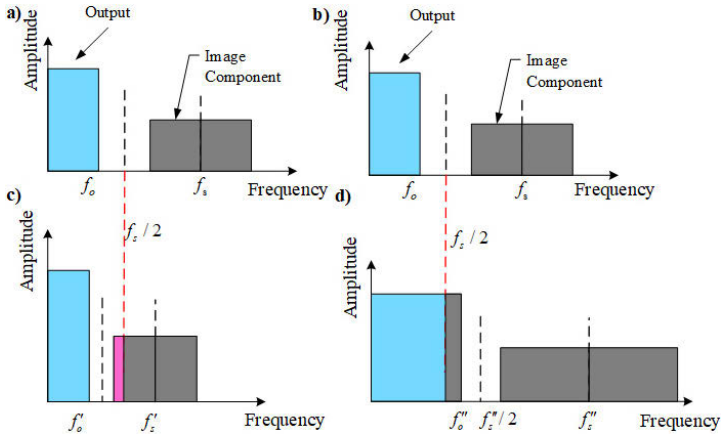

Fig. 2. Spectrum of the DDWS if a low-pass filter with a fixed cut-off frequency is applied.

However, as the sampling frequency decreases, the range of the image components will fall within $f_s/2$ when $f_s' - f_o < f_s/2$.

In result, the image components cannot be completely filtered out, as shown in Fig. 2c. Also, as the sampling rate increases, the effective components of the output signal will be in the cut-off band when $f_o > f_s/2$, causing the effective components to be filtered out, as shown in Fig. 2d. Therefore, in the DDWS, a large number of low-pass filters with different cut-off frequencies are needed to recover the waveform signal from the sampled signal better, which is difficult to achieve in the hardware.

3. Waveform synthesis method based on digital resampling

3.1. The waveform synthesis based on digital resampling

Following the discussion in Section 2, the variable sampling rate makes the image component difficult to suppress in the DDWS. The error of the DDWS occurs in the digital-to-analog conversion part. Therefore, fixing the sampling rate of the DAC can effectively reduce the spurious signal in the output waveforms. As shown in Fig. 3, in the digital-to-analog conversion part, we use a variable clock and process output waveform samples point by point to avoid phase truncation errors; in the digital-to-analog conversion part, we use a fixed sampling clock to limit the number of image components to a fixed range. In order to match the data rate of the two parts, a digital resampling module is added to realize the conversion of the sampling rate.

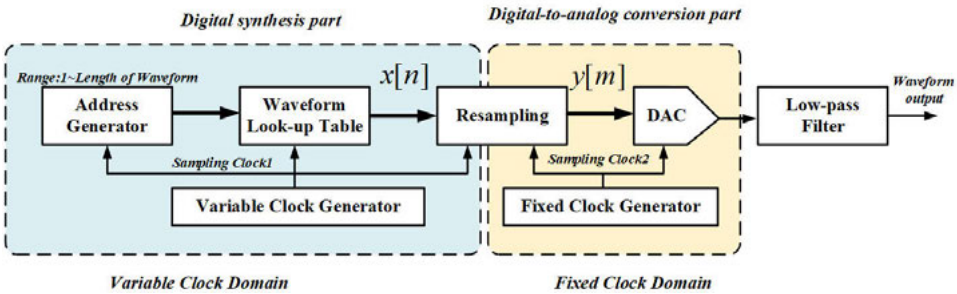

Fig. 3. Structure diagram of the digital resampling method.

Firstly, in the variable clock domain, we get the sampling rate f_s and the samples $x[i]$ according to the required waveform. Then the digital resampling module resamples samples $x[i]$ to get samples $y[j]$. As shown in Fig. 4, the resampled waveform samples $y[j]$ are determined by the original waveform samples $x[i]$ and the time interval $u[j]$. $x[i]$ and $y[j]$ are not in one-to-one correspondence. For example, $y[j+3]$ and $y[j+4]$ correspond to $x[i]$, but the time intervals $u[j+3]$ and $u[j+4]$ are different. We use the J to mark the position of the previous input sample closest to the current output sample $y[jT_{\mathrm{DAC}}]$. The resampled waveform samples $y[j]$ and the original waveform samples $x[i]$ have the following relationship:

$$\begin{aligned} y[jT_{\mathrm{DAC}}] &= y\big[(J+u[j])T_s\big] \\ &= \sum_{i=-\infty}^{\infty} x\big[(J-i)T_s\big] \cdot h\big[(u[j]+i)T_s\big], \end{aligned} \tag{2}$$

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where

$$J = \left\lfloor j\frac{T_{\mathrm{DAC}}}{T_s} \right\rfloor, \qquad u[j] = j\frac{T_{\mathrm{DAC}}}{T_s} - J.$$

Therefore, it is necessary to adjust the system function $h(t)$ in real time according to the change of $u[j]$. The variable delay FIR filter based on the Farrow structure meets the needs of real-time variable delay. Then, the transfer function of the filter can be expressed as:

$$H(z,\mu) = \sum_{n=-N}^{N} h(n,\mu)\cdot z^{-n} = \sum_{n=-N}^{N}\sum_{m=0}^{M} a(n,m)\cdot u^m \cdot z^{-n}, \tag{3}$$

where $a(n,m)$ is the coefficient of FIR filter bank, N is the filter's order, M is the number of FIR filters, u is the time interval. The filter coefficients can be obtained by referring to the design method based on the second-order cone programming proposed in [23] which can minimize the peak error of the variable-frequency response and yields a true minimax design. Therefore, Equation (2) can be written as:

$$y[jT_{\mathrm{DAC}}] = \sum_{n=-N}^{N}\sum_{m=0}^{M-1} a(n,m)\cdot u[j]^m \cdot x\left[(J-n)T_s\right]. \tag{4}$$

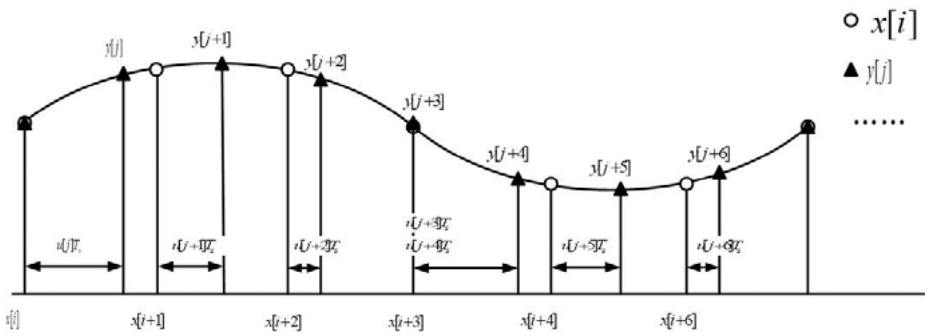

Fig. 4. Principle of digital resampling.

3.2. Parallel implementation

For design flexibility, digital waveform sample processing is usually implemented in FPGA. However, the maximum work speed of FPGA can only be up to several hundred MHz, which cannot meet the high sampling rate requirement of the waveform synthesis system. Therefore, the processing of a waveform sample in FPGA is performed in a parallel structure. In [24], Li et al. proposed a parallel resampling structure to realize sampling rate conversion effectively. However, it can only extract samples and cannot insert them, resulting in the fact that it can only realize the conversion from a high sampling rate to low one. In AWG, the sampling rate determines the bandwidth of the output waveform, so the sampling rate should be set to maximum, i.e. usually the maximum sampling rate of the DAC. As a result, we need a parallel resampling structure that can realize the conversion from a low sampling rate to a high one.

We proposed a parallel resampling structure as shown in Fig. 5, including waveform sample *First Input First Output* (FIFO), waveform sample registers, a phase controller and a k-path FIR filter bank. The waveform registers are used to provide the sample sequence for the filter, while the

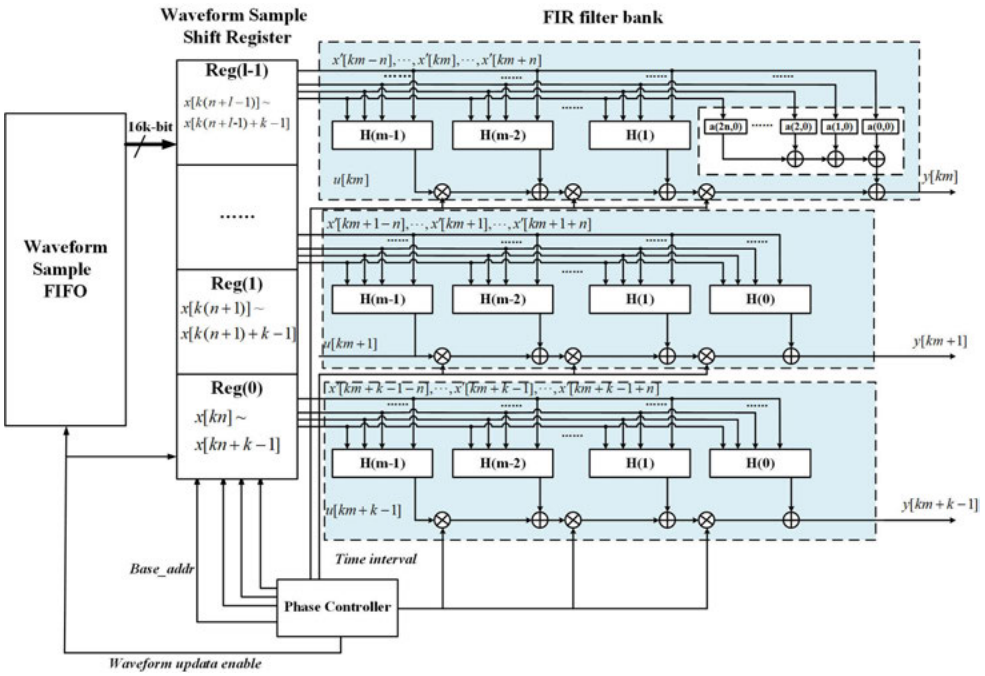

Fig. 5. Parallel resampling structure.

phase controller provides the position of the sample sequence in the registers, the time interval, and the enable signal to update the samples in FIFO and registers.

According to Section 3.2, the output sample $y[j]$ is determined by its corresponding input sample sequence and time interval $u[j]$, the input sample sequence is denoted as $x'[J-n],\ldots,x'[J],\ldots,x'[J+n]$. Assuming that the number of parallel paths is k, the FIFO outputs up to k samples per clock. However, k FIR filter banks need at most $2n+k$ input samples in a unit time. Therefore, we use registers to provide input samples for FIR filter banks. As shown in Fig. 5, Reg(0) ~ Reg($l-1$) are l registers with a storage capacity of k samples.

$$l = \left\lceil \frac{2n+k}{k} \right\rceil. \tag{5}$$

The phase controller evaluates the current input sample sequence and the time interval through the phase accumulator. The control word of the phase accumulator is determined by the ratio of the variable sampling frequency and the fixed sampling frequency of the DAC:

$$\omega = \frac{f_s}{f_{\mathrm{DAC}}} = \frac{T_{\mathrm{DAC}}}{T_s} < 1. \tag{6}$$

The phase of the output samples can be expressed as:

$$\begin{cases} \eta(km) = \eta(km-1) + \omega \\ \eta(km+1) = \eta(km-1) + 2\omega \\ \cdots \\ \eta(km+k-1) = \eta(km-1) + k\omega \end{cases}, \tag{7}$$

where $\eta(0) = 0$.

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In FPGA, we need to quantize and normalize ω and $\eta(m)$, and add a sign bit to the highest bit, we denote this process as $[\cdot]$. The change of the sign bit can determine whether the input sample sequence needs to be updated. As shown in Fig. 6, the $y[0]$ is the initial sample and its phase is 0, and the phases of $y[1]$, $y[2]$, $y[3]$ are $\frac{T_{\mathrm{DAC}}}{T_s}$, $\frac{2T_{\mathrm{DAC}}}{T_s}$, $\frac{3T_{\mathrm{DAC}}}{T_s}$ respectively. Because $2T_{\mathrm{DAC}} < T_s < 3T_{\mathrm{DAC}}$ in Fig. 6, the phase of $y[0]$, $y[1]$, $y[2]$ does not exceed 1, and the sign bit has not changed, so their corresponding input sample is $x[0]$; the phase of $y[3]$ exceeds 1, the sign bit changes, and the corresponding input sample is updated to $x[1]$.

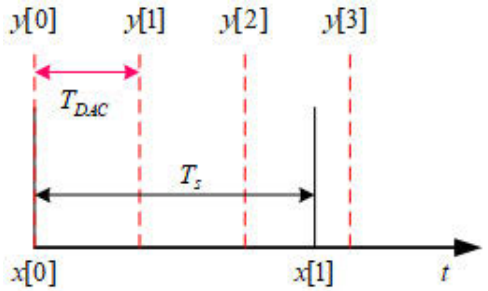

Fig. 6. Relationship between phase and input samples.

Enabling input sample update can be expressed as:

$$\begin{cases} en[km] = \mathrm{sgn}\,[\eta(km-1)] \oplus \mathrm{sgn}\,[\eta(km)] \\ en[km+1] = \mathrm{sgn}\,[\eta(km)] \oplus \mathrm{sgn}\,[\eta(km+1)] \\ \cdots \\ en[km+k-1] = \mathrm{sgn}\,[\eta(km+k-2)] \oplus \mathrm{sgn}\,[\eta(km+k-1)] \end{cases}, \tag{8}$$

where sgn denotes the sign bit and $\oplus$ represents exclusive OR (XOR).

Regarding l registers as waveform memories with a length of lk, the position of input sample $x'[m]$ in the register group is recorded as $base\,[m]$, then:

$$\begin{cases} base\,[km] = en\,[km]?base\,[km-1]+1 : base\,[km-1] \\ base\,[km+1] = en\,[km+1]?base\,[km]+1 : base\,[km] \\ \cdots \\ base\,[km+k-1] = en\,[km+k-1]?base\,[km+k-2]+1 : base\,[km+k-2] \end{cases}, \tag{9}$$

where "?" represents the logical condition judgement. In the next unit time, if the position of the first sample of the first path exceeds the position of the first register:

$$\text{if} \;\; base\,[km+1] - n > k-1. \tag{10}$$

It proves that the samples in the first register $Reg(l-1)$ are useless, so the samples in this register need to be updated. The shift registers implement shifting in steps of k samples, and the samples in the first register are replaced by k new samples output by FIFO. At the end, we obtain

the following update of the base address of the sample sequence:

$$\begin{cases} Reg(0) <= Reg(1) \\ Reg(1) <= Reg(2) \\ \cdots \\ Reg(l-1) <= FIFO\_out \\ base\,[k(m+1)] = base\,[km(m+1)] - k \end{cases}. \tag{11}$$

The above is the process through which the phase controller realizes the control of the input sample sequence through the sign bit of the phase. And the time interval is determined by the numerical bits of the phase as below:

$$\begin{cases} \mu[km] = num\,[\eta(km)] \\ \mu[km+1] = num\,[\eta(km+1)] \\ \cdots \\ \mu[km+k-1] = num\,[\eta(km+k-1)] \end{cases}. \tag{12}$$

4. Experiment

In order to verify the performance of the designed arbitrary waveform synthesis module based on digital resampling, we have designed an experimental test bench to measure its spurs as shown in Fig. 7. An RTO 1024 Rohde&Schwarz oscilloscope, with a 2 GHz bandwidth and a sampling rate up to 10 GSa/s was used to observe the time-domain diagram of the output waveform. A 53230A Keysight Cymometer, with a bandwidth of 6 GHz and 11-bit measurement resolution, was used to measure the frequency of the output waveform. An N9010A Agilent EXA Signal Analyzer, with a frequency measurement range from 10 Hz to 26.5 GHz was used to measure the spur performance. The designed waveform synthesis circuit board, shown in Fig. 8, is connected to the industrial computer through a PCI-e gold finger interface and integrated in the chassis called the designed circuit module. And an external screen is used to display the user interface of the waveform editing software, which is used to edit the waveform samples and generate control commands. The designed circuit board includes six parts: Power module, DDR3 SDRAM, FPGA,

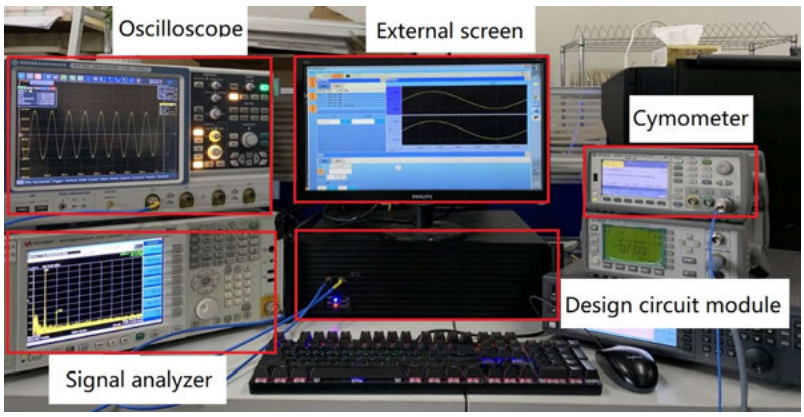

Fig. 7. Experimental test bench.

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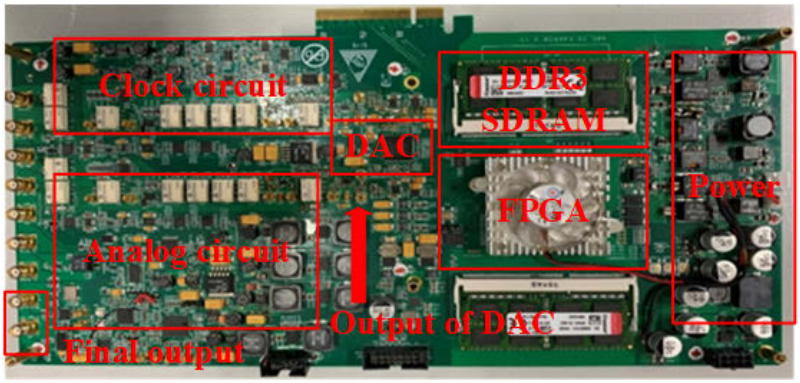


Fig. 8. Waveform synthesis circuit board.

DAC, clock module and analog module. The power module provides energy for the entire circuit board. DDR3 SDRAM is used to store data of waveform samples. FPGA is the core of the entire circuit board. Its functions include obtaining waveform samples and control instructions from an industrial computer, completing digital waveform synthesis, digital resampling, and finally transmitting the waveform samples to the DAC (AD9136) through a high-speed interface. The FPGA we chose is XCKU060-FFVA1156-2E of the Xilinx company, and the resource utilization are shown in the below Table 1:

Table 1. Output frequency after resampling test results.

Resource	BRAM	LUT	Slice flip flops
Number	42	12120	24240
Percentage	7%	5%	5%

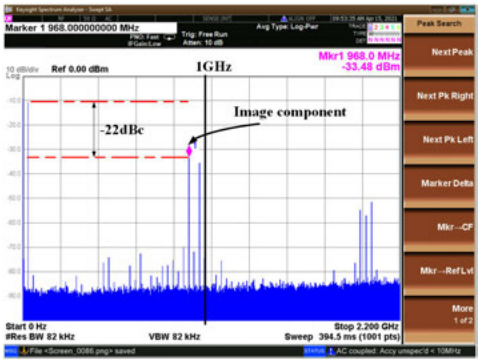
Firstly, we verify the quality of the single tone waveform generated by the proposed waveform synthesis system. In order to facilitate the comparison of experimental results, we have set up two modes, with digital resampling (proposed in this paper as shown in Fig. 3) and without digital resampling (DDWS). In the digital resampling mode, the fixed sampling rate of the DAC is set to 2 GSPS and the resampling module is a FIR filter bank with 11 5th order filters according to [23]. In the mode without digital resampling, the sampling rate of the DAC is set to the sampling rate in variable clock domain. We acquire a sine waveform samples with a period length of 64 samples through the calculation formula equation (4) and set the variable sampling rate to 983 MSPS, 1.228 GSPS, and 1.474 GSPS respectively. Therefore, the frequency of the generated waveforms should be 15.359375 MHz, 19.1875 MHz, and 23.03125 MHz. The accuracy of the crystal clock source we chose is 1ppm, so the output frequency should be within the range of 15.359359640625 MHz ~ 15.359390359375 MHz, 19.1874808125 MHz ~ 19.1875191875 MHz, and 23.03122696875 MHz ~ 23.03127303125 MHz. The frequencies of the output waveforms measured by the cymometer are shown in Table 2, all within the effective range. Therefore, digital resampling does not change the frequency characteristics of the generated waveform.

Then, we verify the improved effect of digital resampling on the spur. We compare the spectrums of the waveforms generated by the two modes. Figure 9 is a spectrum test diagram of

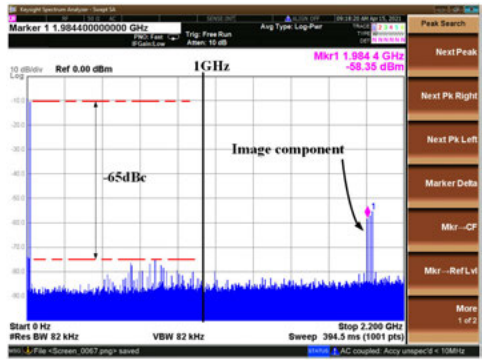
Table 2. Output frequency after resampling test results.

Waveform Period	Sampling rate before resampling	Sampling rate of the DAC	Frequency of output
64 Samples	983 MSPS	2 GSPS	15.35938 MHz
64 Samples	1.228 GSPS	2 GSPS	19.18751 MHz
64 Samples	1.474 GSPS	2 GSPS	23.03127 MHz

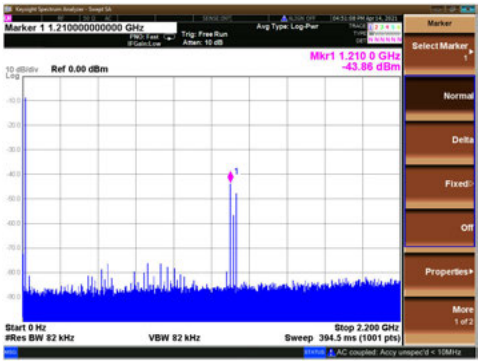
a) mode with digital resampling (f_{s1} = 983 MSPS)



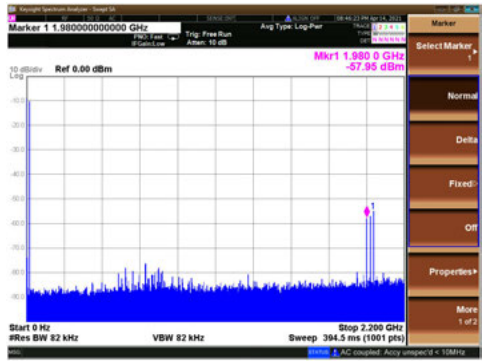
b) mode without digital resampling (f_{s2} = 2 GSPS)



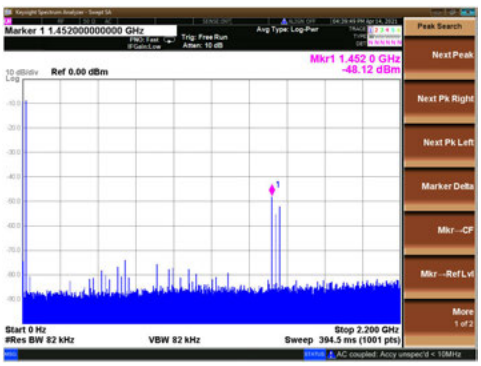
c) mode with digital resampling (f_{s1} = 1.228 GSPS)



d) mode without digital resampling (f_{s2} = 2 GSPS)



e) mode with digital resampling (f_{s1} = 1.474 GSPS)



f) mode without digital resampling (f_{s2} = 2 GSPS)

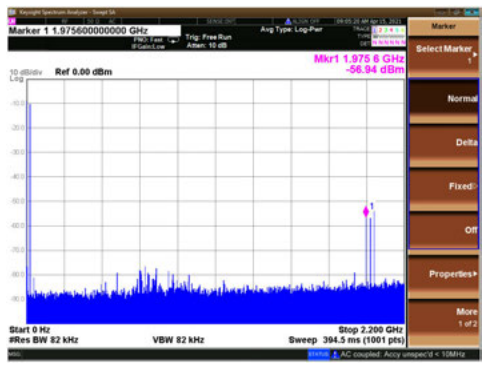


Fig. 9. Spectrums of the output waveforms generated by two modes.

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sine waveforms of 15.35938 MHz generated by the two modes. If we set the low-pass filter cut-off frequency to 1 GHz (half of the DAC's maximum sampling rate), in the mode without digital resampling (DDWS), the image component is in the passband of the low-pass filter and cannot be filtered out, the measurement result for the SFDR is 22 dBc in Fig. 9a. In the digital resampling mode, the sampling rate is 2 GSPS, so the image component is at 1986.4062 MHz ($f_s - f_o$), i.e.in the cut-off band of the low-pass filter, the measurement result for the SFDR is 65 dBc in Fig. 9b. Additionally, in Fig. 9c, 9e, it can be seen that the position of the image component will change remarkably due to the different sampling rate. In Fig. 9d, 9f, the image component of the output waveform after digital resampling appears at 1.980 GHz and 1.9756 GHz, respectively. Because the frequency measurement of the signal analyzer is not very accurate, the frequency point of the image component basically satisfies the equation 2 GHz $- f_o$. Therefore, the arbitrary waveform synthesis structure based on digital resampling can make the sampling rate of the DAC a fixed value. According to the Nyquist's theorem, the effective component of output is at the range of $0 \sim 0.5 f_s$, which is about $0 \sim 0.4 f_s$ in practical applications. And the frequency of the image component is at $f_s - f_o$. Therefore, if the cut-off frequency of the filter is set to half of the sampling frequency, the effective component can be effectively retained and the image component can be filtered out. The SFDR of the output signal will not be affected by the image component, and is only related to the performance of the DAC.

The experiment above proves that the proposed waveform synthesis method based on digital resampling can realize the generation of single tone waveform effectively. Subsequently, we will verify the method's ability to synthesize a multi-tone waveform. First, with, we obtained sweep waveform samples at the 2 GSPS sampling rate with a variation range of 10 MHz ~ 114.4 MHz. The test results in the time and frequency domains are shown in Fig. 10.

a) sweep waveform in the time domain (f_s = 2 GSPS) b) weep waveform in the frequency domain ($f\,s$ = 2 GSPS)

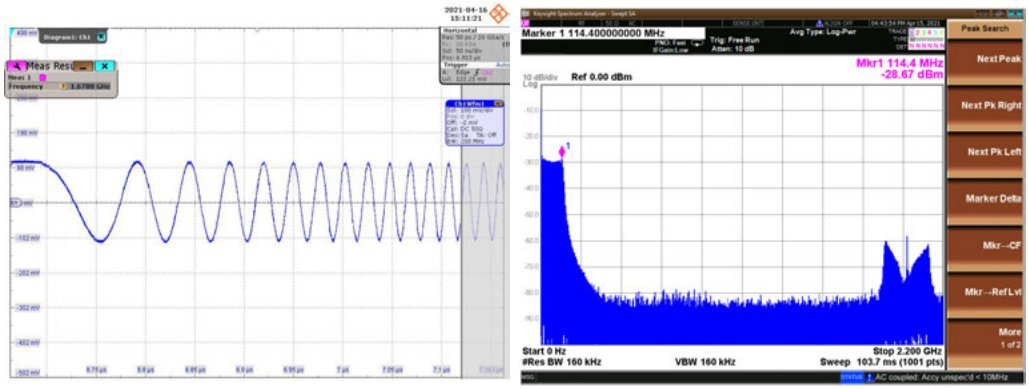

Fig. 10. Test results for the sweep waveform.

Then, under the mode without digital resampling, we set the sampling rate to 983 MSPS, 1.228 GSPS and 1.474 GSPS. and the resulting spectrums are shown in Fig. 11.

With digital resampling enabled, the spectrums were as shown in Fig. 12.

We can see from Fig. 11 that the image components are at 1.0428 GHz, 1.298 GHz, 1.5576 GHz before resampling and at 2.0584 GHz, 2.0724 GHz, 2.0856 GHz, 2.1164 GHz after it, which fits the theoretical values. We can conclude from the results that the digital resampling module can

a) f_s = 983 MSPS b) f_s = 1.228 GSPS c) f_s = 1.474 GSPS

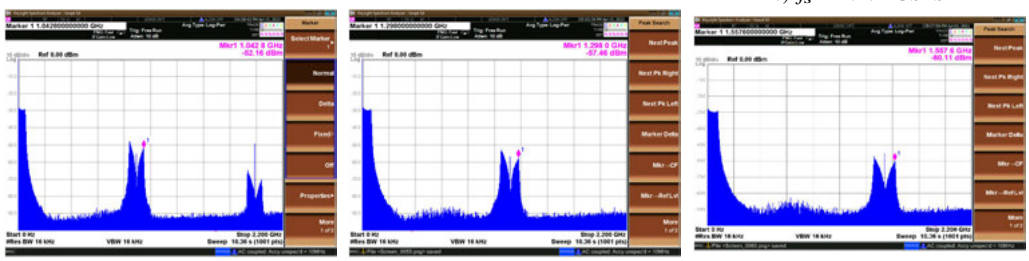

Fig. 11. Spectrums without digital resampling.

a) f_s = 983 MSPS b) f_s = 1.228 GSPS c) f_s = 1.474 GSPS

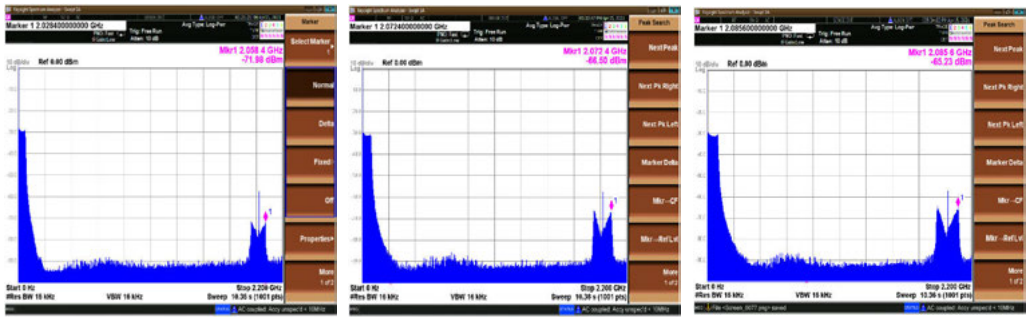

Fig. 12. Spectrums with digital resampling.

alter waveform samples while applying variable sampling rates to waveform samples under fixed sampling rate of 2 GSPS without changing the output frequency. The image components can be moved from a relatively low frequency to the vicinity of 2 GHz for the subsequent low-pass filter to filter it out and improve the spectrum purity of the output waveforms.

5. Conclusions

We realized an arbitrary waveform synthesis method based on digital resampling, avoiding the limitations existing in both DDFS and DDWS. We separated the waveform synthesis process into two parts and used a variable delay filter based on the Farrow structure in the digital waveform synthesis part to realize the conversion of sampling rate so as to avoid the phase truncation error that appears in the DDFS. The digital-to-analog conversion part was realized at a fixed sampling rate, as compared to the DDWS, it restrained the image components in a fixed range. At the same time, in order to improve the sampling rate of the system, the waveform sample shift register and phase controller were used in the FPGA to realize the parallel output of non-uniform resampling samples. As a result, we improved the SFDR by 43 dBc as well as the output waveform's spectrum purity, as compared to the DDWS. The effectiveness of the proposed arbitrary waveform synthesis structure was verified and it is clear that this new method can be applied to generating waveforms with much lower spur and a high sampling rate.

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