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# Research on topology of a novel three-phase four-leg fault-tolerant NPC inverter

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**Abstract:** Diode neutral point clamped (NPC) three-level converters have been widely used in recent years. Aiming at the problems of the high device failure rate and unstable neutral point potential of NPC three-level converters, an NPC three-level circuit with fourth bridge arm redundancy is proposed based on the traditional NPC three-level converter. The redundant fourth bridge arm is used to realize the function of stabilizing voltage when there is no fault and replacing the fault half-bridge arm to maintain the continuous operation of the converter when there is a fault. By analyzing the working principle of space vector pulse width modulation (SVPWM) and the power loss of the switch, it is of particular significance to the design and control of NPC three-level converters in the future. Matlab/Simulink verifies the feasibility of the fault-tolerant circuit structure.

**Key words:** fault tolerant operation, midpoint potential equilibrium, NPC inverter, topology reconstruction

## 1. Introduction

The diode neutral point clamped (NPC) type three-level inverter has the advantages of enormous output power, output voltage close to a sine wave, and a small output current total harmonic distortion factor. It has been widely used in aerospace, rail transit, new energy vehicles, and so on. Compared with two-level inverters, three-level inverters use more than twice as many power electronics devices, so the failure probability is higher for three-level inverters [1, 2]. In practical application, the reliability requirements of the inverters are getting higher and higher. Therefore, the application and promotion of three-level fault-tolerant inverters are of great significance [3, 4].

According to the different number of bridge arms, the fault-tolerant control methods of NPC inverters can be divided into two categories: the first one is the topology reconstruction based on

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three-phase and three-arm structure; the other is the method to replace the fault bridge arm with the three-phase four bridge arm. Compared with the traditional three-phase three bridge arm, the three-phase four bridge arm has one more bridge arm, which can realize the balance control of neutral point potential and the replacement function of the fault bridge arm. Reference [5] proposed a two-level fourth-arm NPC inverter. The two-level fourth leg replaces the fault leg to operate normally in the fault state, and fewer switches are used in this structure. Reference [6] proposed a structure that uses a dimensionality reduction strategy and uses the fourth bridge arm to suppress the midpoint drift. The patent in [7] proposes to replace the fourth bridge arm with a T-type three-level bridge arm. Through different combinations of switches of the fourth bridge arm, the voltage on the lower DC bus capacitor is adjusted to maintain the stability of the bus midpoint voltage. Compared with the traditional three-level four-leg structure, this structure reduces the use of two clamping diodes, reduces cost, better compensates for loss, has higher efficiency, and so on.

However, although the above NPC inverter can carry out fault-tolerant control, there are still problems of the neutral point potential instability and imbalance. At present, many scholars have proposed a variety of modulation strategies based on the neutral point possible imbalance. In References [8–11], the Pulse Width Modulation (PWM) method was adopted, by injecting zero-sequence voltage, the average value of neutral point current flowing through the capacitor in a single sampling period is zero. In References [12, 13], a method based on SVPWM was proposed, introducing a balance factor to reasonably select the action time of small and medium vectors. The above techniques need to sample the voltage and current values, and the balance effect is directly related to the load power factor and modulation ratio. In reference [14], fuzzy control was adopted, and in references [15–17], the method of an adjacent long vector and synthetic medium vector was adopted, which has a good balance effect. The above balance method is mainly improved in its modulation part, primarily focusing on the problem of the neutral point potential imbalance of a three-phase three-leg inverter, which is more suitable for that three-phase three-leg inverter. So, a neutral point potential balance control method of a three-phase four-leg structure is proposed in this paper. The neutral point potential balance is adjusted through the control of the fourth leg. The simulation results show that this method is reasonable and can effectively modulate the neutral point potential of a three-phase four-leg inverter [18, 19].

## 2. Three-level NPC inverter modulation strategy and fault-tolerant topology

### 2.1. Main circuit of traditional three-level NPC inverter

A circuit diagram of the traditional three-level NPC inverter is shown in Fig. 1. It is composed of the DC side, AC measuring bridge, and inverter bridge. The inverter bridge is composed of three bridge arms. Each bridge arm is divided into upper and lower bridge arms, including 2 insulated gate bipolar transistors (IGBTs), two clamping diodes, and one freewheeling diode. Taking a phase as an example, the upper bridge arm includes two switches $S_{a1}$ and $S_{a2}$; two freewheeling diodes $VD_{a1}$, $VD_{a2}$, and one clamping diode $VD_{a5}$. The lower bridge arm comprises two switch tubes, $S_{a3}$ and $S_{a4}$; two freewheeling diodes $VD_{a3}$, $VD_{a4}$, and one clamping diode $VD_{a6}$. The three-phase output currents are, respectively, $i_a$, $i_b$, and $i_c$; the three-phase output voltages are, respectively, $u_a$, $u_b$, and $u_c$.

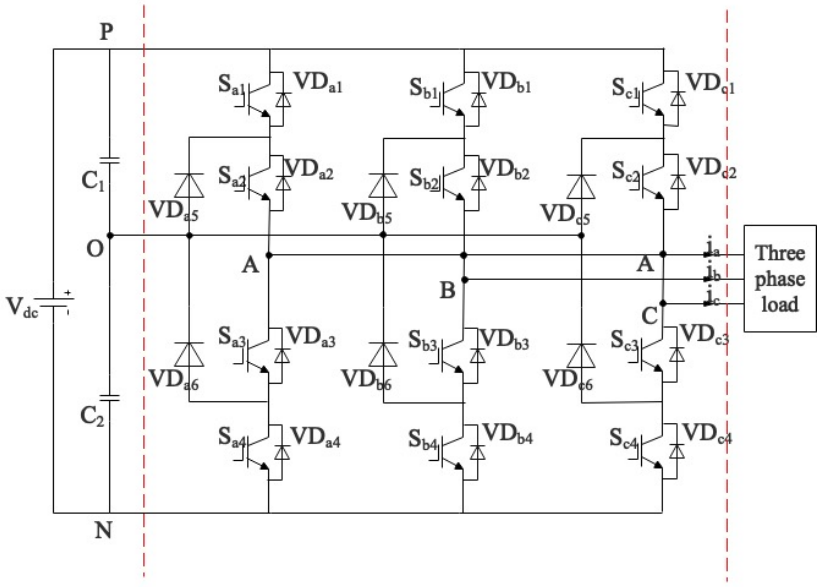


Fig. 1. Main circuit diagram of three-level NPC inverter

Each phase voltage of NPC type three-level inverters has three-level states: $+1/2V_{\mathrm{dc}}$, 0, $-1/2V_{\mathrm{dc}}$. The corresponding output of each phase is expressed as positive (P), zero (0), negative (N), three switch states.

### 2.2. SVPWM control strategy of NPC type three-level inverter

In a three-phase symmetrical circuit system with an AC motor as a load, when the motor is connected to a three-phase voltage, the output voltage of the NPC type inverter is the standard phase voltage. Therefore, the output voltages $u_a$, $u_b$, and $u_c$ can be regarded as three voltage vectors, and the space voltage vector can be obtained as shown in Eq. (1):

$$V = \frac{2}{3}\left(u_a + e^{j\frac{2\pi}{3}}u_b + e^{j\frac{4\pi}{3}}u_c\right). \tag{1}$$

NPC inverters can output three levels per phase, namely $V_{\mathrm{dc}}/2$, 0, $-V_{\mathrm{dc}}/2$, which represent positive (P), zero (0), and negative (N) levels. The expression of the phase voltage of each phase bridge arm is shown in Eq. (2):

$$u_a = \frac{V_{\mathrm{dc}}}{2}S_a\,, \qquad u_b = \frac{V_{\mathrm{dc}}}{2}S_b\,, \qquad u_c = \frac{V_{\mathrm{dc}}}{2}S_c\,. \tag{2}$$

The three-level inverter has three output states for each phase bridge arm, so a total of $3^3 = 27$ working states can be output, corresponding to different inverter switching states. Bring Eq. (2) into Eq. (1), the voltage space vector can be represented by the switch state, as shown in Eq. (3):

$$\vec{V} = \frac{V_{\mathrm{dc}}}{6}\left[(2S_a - S_b - S_c) + j\sqrt{3}\,(S_b - S_c)\right]. \tag{3}$$

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According to all working conditions, four voltage vectors with different amplitudes can be obtained, long vector $\frac{2}{3}V_{dc}$, medium vector $\frac{\sqrt{3}}{3}V_{dc}$, short vector $\frac{1}{3}V_{dc}$, and zero vector. The 27 voltage vectors in the $\alpha-\beta$ plane are shown in Fig. 2.

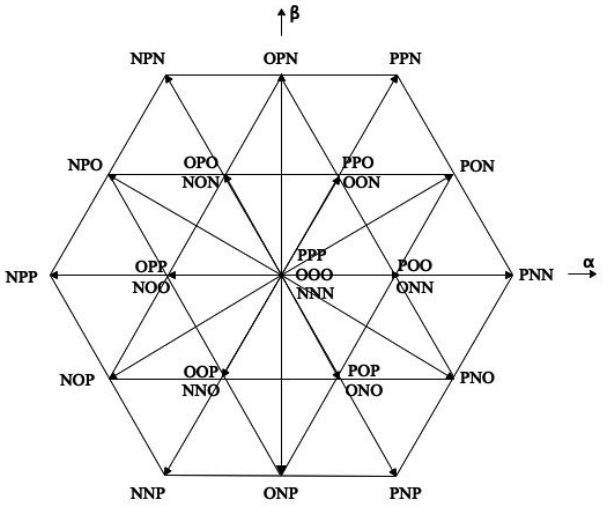


Fig. 2. Space vector distribution of three-level inverter

It can be seen from the SVPWM vector diagram that to make the NPC type, the three-level inverter outputs a nearly circular voltage vector to obtain a circular magnetic flux. It is necessary to linearly combine the basic voltage vectors to construct arbitrary angles and amplitudes.

Through the above requirements, to realize the control of the NPC type three-level SVPWM inverter, three steps need to be completed in one sampling period:

1. Large sector judgment and inter-district judgment determine the three basic vectors synthesized by the reference voltage vector.
2. Calculation of the basic vector action time to determine the action time of each basic voltage vector of the synthesized reference voltage vector in a sampling period.
3. Time state allocation, determines the switch sequence and the switch state of each vector, and allocates the calculated action time to the corresponding switch state.

### 2.3. Fourth bridge arm fault tolerant topology

Based on the traditional three-level inverter in Fig. 1, the fourth bridge arm is introduced to form a new fault-tolerant topology. It can stabilize the neutral point potential under regular operation and provide fault tolerance of the inverter under fault operation. The topology is shown in Fig 3. The three phases a, b and c are the three primary arms of the inverter, and the fourth arm on the right is the redundant arm. Among them, a 75A /600 V IGBT and fast recovery diode are selected as the intermediate commutation link, and the midpoint clamp diode is composed of an SiC diode. The practice has proved that the application of new power devices to the inverter system reduces the loss of the inverter.

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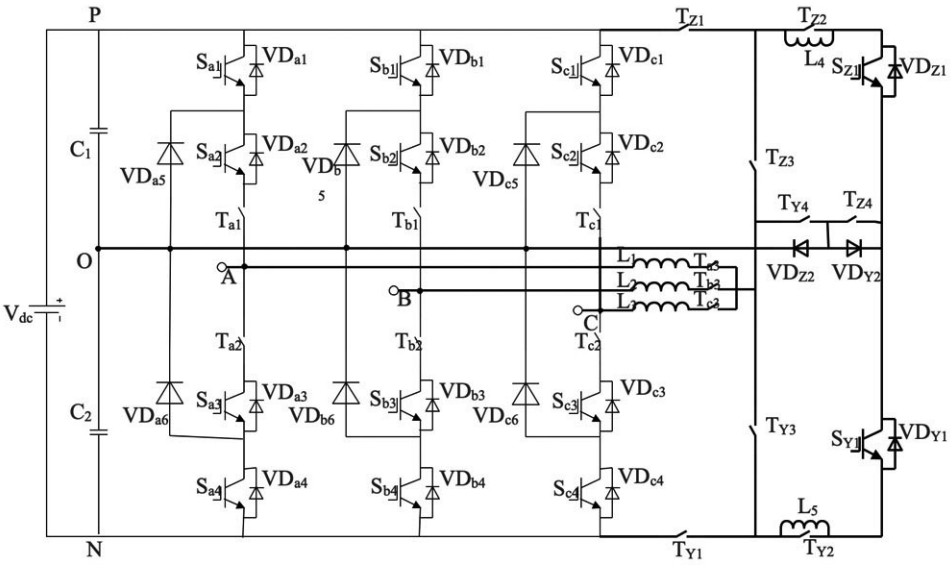


Fig. 3. Three-level NPC inverter fault-tolerant topology

Circuit breakers $T_{X1}$ and $T_{X2}$ $(X = a, b, c)$ disconnect the upper or lower bridge arms when three-bridge arms, $a$ or $b$ or $c$, fail. Inductors $L_4$ and $L_5$ are the stable neutral point potential of the inverter under normal operation. Circuit breaker $T_{Z1}, T_{Z2}, T_{Z3}, T_{Z4}, T_{Y1}, T_{Y2}, T_{Y3}$, and $T_{Y4}$ are selectively turned on and off after the fourth bridge arm of the inverter fails to replace the failed bridge arm and make the inverter operate continuously and normally. Inductors $L_1$, $L_2$, $L_3$ are used to stabilize the midpoint potential and reduce the generation of harmonics when the inverters are fault-tolerant. IGBTs $S_{Z1}$ and $S_{Y1}$ provide freewheeling status under regular operation and replace the fault-tolerant operation of the fault bridge arm under fault conditions.

## 3. Fault tolerant topology and neutral point potential balance analysis under different working states

### 3.1. Fault tolerant topology for fault free operation

When an NPC inverter operates without fault, the switching states of each circuit breaker: $T_{X1}$, $T_{X2}$ $(X = a, b, c)$, $T_{Z1}$, $T_{Y1}$, $T_{Z4}$, and $T_{Y4}$ are all on; $T_{X3}$ $(X = a, b, c)$, $T_{Z2}$, $T_{Z3}$, $T_{Y2}$, $T_{Y3}$ are all disconnected; IGBTs $S_{Z1}$ and $S_{Y1}$ are on. The fault-tolerant topology of the inverter under fault-free operation is shown in Fig. 4.

During fault-free operation, the added fourth arm adds an inductance branch to adjust the midpoint voltage of the DC bus. By controlling the switching states of IGBTs $S_{Z1}$ and $S_{Y1}$, the neutral point voltage of the DC bus can be adjusted. At this time, the adjustment circuit model can be simplified, as shown in Fig. 5.

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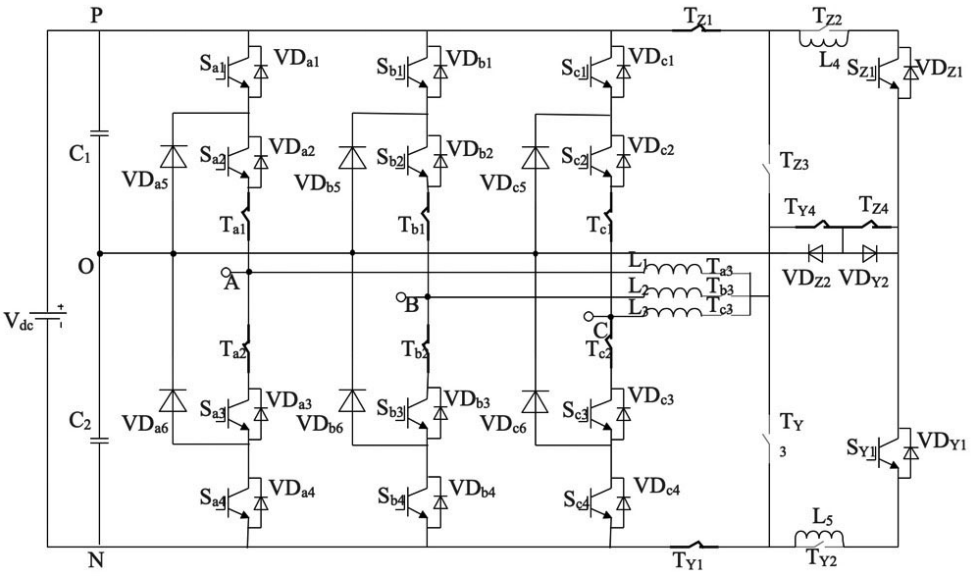


Fig. 4. Fault-tolerant topology of NPC inverter without failure

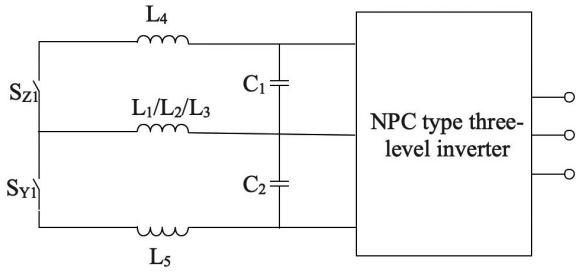


Fig. 5. Simplified circuit model in fault-free state

As shown in Fig. 5 above, the fourth T-arm provides one discharge path for the two supporting capacitors on the DC bus. The corresponding switch will be conducted when the voltage value on the supporting capacitance $C_1$ and $C_2$ is too high. Then it can discharge, reduce the voltage, and maintain the voltage balance between the upper and lower supporting capacitors. If the voltage of the support capacitor $C_1$ is too high, the switch $S_{Z1}$ is turned on to discharge the support capacitor $C_1$, which can reduce its voltage and maintain the voltage balance of $C_1$ and $C_2$.

Compared with the traditional inductance injection circuit, the inductance is placed differently between the fourth bridge arm's midpoint and the DC bus's midpoint. This article uses two inductance branches to be located outside the IGBT. The method proposed in this article uses fewer electronic components and saves a particular cost. When an IGBT on the fourth bridge arm is turned on, another non-conductive IGBT needs to withstand the voltage $V_{dc}$ of the entire DC bus. Therefore, higher requirements are put forward for the voltage resistance of the IGBT.

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The neutral point balance control strategy used in the circuit is easy to realize. By comparing the voltage difference between the upper and lower capacitors, when the voltage difference between the two support capacitors exceeds a specific set value, the IGBT on the higher voltage side works to discharge and depressurize the corresponding capacitor. The control block diagram is shown in Fig. 6.

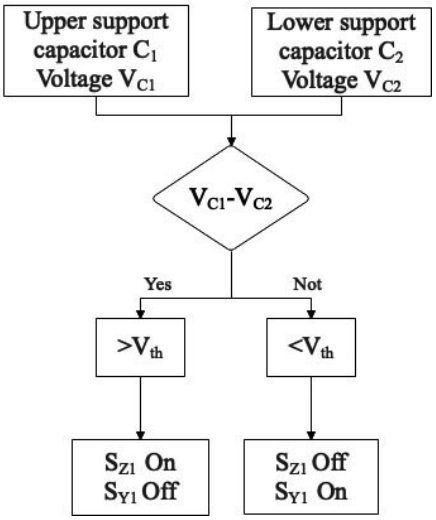


Fig. 6. Midpoint voltage balance control strategy control block diagram

The selection of the appropriate inductance size in the fourth bridge arm can ensure that when the main circuit flows (in) from the midpoint, the current can flow (out) at the same speed so that the midpoint potential is stabilized. Now take the primary circuit drawing current from the midpoint as an example to analyze the choice of inductance. If the midpoint potential $V_{C1} > V_{\mathrm{dc}}/2$, the fourth upper bridge arm $T_{Z1}$ is turned on to maintain the midpoint potential balance, and the fourth lower bridge arm $T_{Y1}$ is turned off.

Suppose the sampling period in the primary circuit is $T_s$, and the switching period of the fourth bridge arm is $T_a$, and $T_s = nT_a$ (for convenience, an integer). Take the extreme case; the current flows from the midpoint when the sampling starts. Since the sampling frequency $(1/T_s)$ of the primary circuit is higher than the output frequency of the introductory course, it can be considered that in a sampling period, the three-phase output current is unchanged. Therefore, the maximum charge flowing out from the midpoint is $\sqrt{2}I \cdot T_s$ in a sampling period. If the fourth bridge arm can control flow to the midpoint at the same speed, it can be considered that the midpoint potential remains unchanged. Currently, turn on $T_{Z1}$ with a particular duty cycle to inject charge into the midpoint. In a period, $T_a$, the waveform of the inductor current may be as shown in Fig. 7.

Assuming that the midpoint voltage is unchanged during the $T_{Z1}$ turn-on period ($t_{\mathrm{on}}$), the voltage applied across the inductor is the capacitor voltage $V_{C1}$, and the inductor current rises at the slope of $V_{C1}/L$ (let $L = L_4$). During the $T_{Y1}$ turn-off period ($t_{\mathrm{off}}$), the voltage across the inductor is the capacitor voltage $V_{C2}$, and the inductor current decreases with a negative slope of

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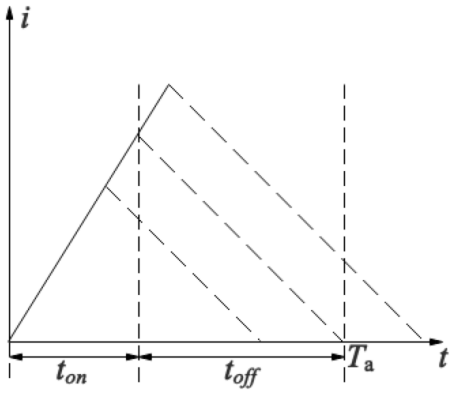


Fig. 7. Trend of the current of inductance

$-V_{C2}/L$. Depending on the turn-on time, the turn-off time also changes proportionally. When the inductor current waveform is exactly as shown by the broken line, it turns off at just one $T_a$ cycle, as shown in Eq. (4):

$$\frac{V_{C1}}{L} \cdot t_{\text{on}} = \frac{V_{C2}}{L} \cdot t_{\text{off}} \quad \Rightarrow \quad \frac{t_{\text{on}}}{t_{\text{off}}} = \frac{V_{C2}}{V_{C1}} . \tag{4}$$

The available critical value is shown in Eq. (5):

$$t_{\text{on}} = \frac{V_{C2}}{V_{\text{dc}}} T_a . \tag{5}$$

When $t_{\text{on}} \leq \frac{V_{C2}}{V_{\text{dc}}} T_a$, the switch can be turned off, provided that the initial current on the inductor is zero. The following discusses the situation that the wind can be turned off in a $T_a$ cycle, and Eq. (6) can be obtained from Eq. (4):

$$t_{\text{off}} = \frac{V_{C1}}{V_{C2}} t_{\text{on}} . \tag{6}$$

$T_{Z1}$ turns on and passes through $t_{\text{on}}$, and the turn-on ends. At this time, the one-phase current connected to the midpoint is the maximum value of the phase current, as shown in Eq. (7):

$$i_{\text{max}} = \frac{V_{C1}}{L} \int_0^{t_{\text{on}}} \mathrm{d}t = \frac{V_{C1} \cdot t_{\text{on}}}{L} . \tag{7}$$

Then the maximum amount of the charge injected during $t_{\text{on}}$ is as shown in Eq. (8):

$$Q_{\text{on}} = \int_0^{t_{\text{on}}} \frac{V_{C1} \cdot t_{\text{on}}}{L} \mathrm{d}t = \frac{V_{C1}}{L} t_{\text{on}}^2 . \tag{8}$$

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In the same way, when it is turned off, as shown in Eq. (9):

$$Q_{\text{off}} = \frac{V_{C1}^2}{L \cdot V_{C2}} t_{\text{on}}^2 \,. \tag{9}$$

In a sampling period $T_a$, the injected and extracted charges are equal, that is, $n \cdot (Q_{\text{on}} + Q_{\text{off}}) = \sqrt{2} I \cdot T_s$, it can be inferred, as shown in Eq. (10):

$$L = \frac{t_{\text{on}}^2 \cdot V_{C1} \cdot V_{\text{dc}}}{\sqrt{2} I \cdot T_a \cdot V_{C2}} \,. \tag{10}$$

At this time, $T_s$, the midpoint, can be compensated within one sampling period.

From Eq. (10), it can be found that the inductance of the fourth bridge arm is related to $t_{\text{on}}$, $V_{C1}$, $V_{\text{dc}}$, $I$, and $T_a$. Among them, $V_{C1}$, $V_{\text{dc}}$, $I$ are the characteristics of the primary circuit, and $t_{\text{on}}$, $T_a$ are related to the fourth bridge arm circuit. The switching frequency of the fourth bridge arm circuit is 2 to 4 times the sampling frequency of the primary course. In addition, the duty ratio of the fourth bridge arm circuit cannot be too small. Otherwise, the rate of rising of the current is too large. It can't be too large; otherwise, the electric energy of each switching cycle will not be released ultimately, which will quickly saturate the inductance. Generally, the fluctuation of the midpoint potential is within 5%, and the duty cycle of the fourth bridge arm circuit can be about 50%.

The above strategy for controlling the neutral point potential balance of the hardware circuit has a simple control principle and simple control realization. The control effect has nothing to do with the system's modulation ratio and power factor. In theory, the fluctuation of the midpoint potential can be controlled within a relatively small range. However, additional hardware investment is required. The increased investment is considerable because the three-level inverter is generally used in high-voltage and high-power applications.

### 3.2. Fault tolerant topology for single-phase half bridge arm fault

In inverters, the two most common fault types for IGBT power devices are open-circuit faults and short-circuit faults. After an IGBT power device has a short-circuit fault, a large amount of heat generated burns it and converts it into an open-circuit fault. Therefore, this paper mainly studies the fault-tolerant control under the open-circuit fault.

When the single-phase half-bridge arm of the main inverter circuit fails, the fourth bridge arm performs fault-tolerant control. Taking the fault of the upper bridge arm of phases as an example, the switches: $T_{a2}$, $T_{b1}$, $T_{b2}$, $T_{c1}$, $T_{c2}$, $T_{a3}$, $T_{Z1}$, $T_{Z2}$, $T_{Y2}$, $T_{Y3}$, $T_{Y4}$ are all connected; $T_{a1}$, $T_{b2}$, $T_{b3}$, $T_{Z3}$, $T_{Z4}$, $T_{Y1}$ are all disconnected; switch tubes $S_{Z1}$, $S_{Z2}$ operate fault-tolerantly instead of switch tubes $S_{a1}$, $S_{a2}$, as shown in Fig. 8.

After fault-tolerant control, the inverter does not need derivation operation, and $VD_{Y2}$ acts as a clamping diode. The $L_1$ inductance in the figure can suppress harmonic generation and reduce harmonic distortion after switching to the fourth bridge arm. The proposed method of the T-type fourth bridge arm in reference [20] realizes the reuse of functions through the on-off control of switches on the clamping branch, but this method increases the number of switches and the risk of failure.

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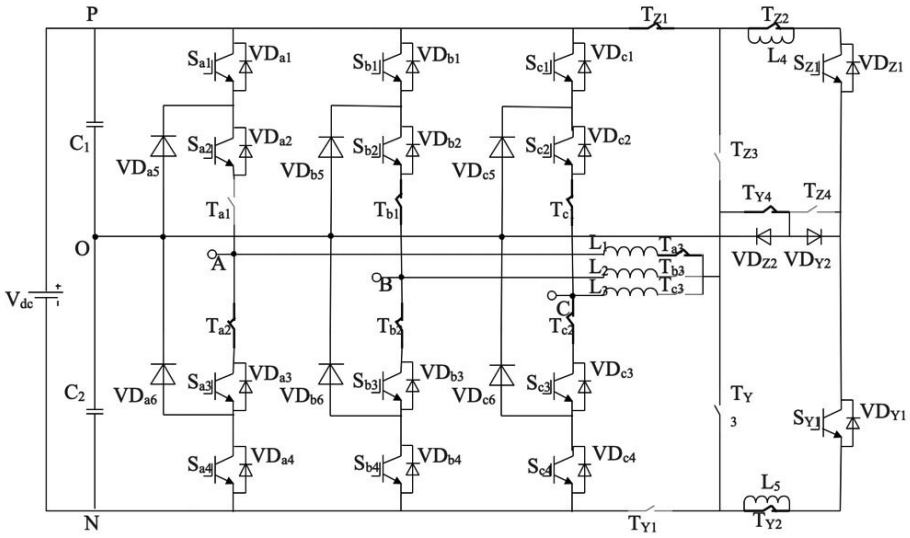


Fig. 8. Fault tolerant topology of NPC inverter a-phase upper bridge arm

## 4. Analysis of power loss of NPC three-level inverter

### 4.1. IGBT loss calculation model

What is given in the IGBT datasheet is the relation curve of the turn-on voltage drop and its turn-on current. Using the straight-line fitting method, the expression of the conduction pressure drop can be obtained, as shown in Eq. (11):

$$v_{CE}(i_c) = v_{CE0} + R_{CE} i_c \,. \tag{11}$$

Then the conduction loss of the IGBT is shown in Eq. (12):

$$P_{\text{con}} = \frac{1}{2\pi} \int_0^{\pi} v_{CE}(i_c(t)) \cdot i_c(t) \, \mathrm{d}t. \tag{12}$$

According to the IGBT datasheet, the parameter values of the switching characteristics in the typical state can be obtained. It is generally considered that there are $E \propto V_{cc}$ and $E \propto I_c$ (among $E$ refers to $E_{\text{on}}$ or $E_{\text{off}}$) in a specific voltage and current range. Therefore, the switching loss of the IGBT is approximated by Eq. (13):

$$P_{\text{swi}} = \frac{1}{2\pi} \int_0^{\pi} \left[ E_{\text{on}} \frac{v_{CE}(t_{\text{on}}) i_c(t)}{V_{CE} I_c} + E_{\text{off}} \frac{v_{CE}(t_{\text{off}}) i_c(t)}{V_{CE} I_c} \right] \mathrm{d}t \cdot f_s \,, \tag{13}$$

where $V_{CE}$ $(t_{\text{on}})$ and $V_{CE}$ $(t_{\text{off}})$, respectively, refer to the withstand voltage at the turn-on and turn-off moments of the IGBT. $V_{CE}$ and $I_c$ are the test conditions for $E_{\text{on}}$ and $E_{\text{off}}$ in the datasheet, respectively.

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### 4.2. Diode loss calculation model

The diode datasheet shows the curve of the forward voltage drop and its conduction current. Using the straight-line fitting method, the expression of the conduction pressure drop can be obtained as Eq. (14):

$$v_F(i_F) = v_{F0} + R_F i_F \,. \tag{14}$$

Then the conduction loss of the diode is Eq. (15):

$$P_{D\text{con}} = \frac{1}{2\pi}\int_0^{\pi} v_F(i_F(t)) \cdot i_F(t)\,\mathrm{d}t. \tag{15}$$

The general expression of the diode's reverse recovery loss is Eq. (16):

$$P_{D\text{rev}} = Q_{rr} V_R \,, \tag{16}$$

where: $Q_{rr}$ is the reverse recovery charge; $V_R$ is the reverse bias voltage it bears. Since $Q_{rr}$ is related to $I_f$ and $\mathrm{d}i_F/\mathrm{d}t$, the diode multi-reverse recovery loss is Eq. (17):

$$P_{D\text{rev}} = \frac{1}{2\pi}\int_0^{\pi} \frac{i_{F(t)}}{I_f} Q_{rr} V_R\,\mathrm{d}t \cdot f_s \,, \tag{17}$$

where $I_f$ is the test condition of $Q_{rr}$ in the data sheet.

### 4.3. Loss calculation model of NPC type three-level inverter

The equivalent duty ratio $D$ of the bridge arm output voltage and the instantaneous value $i_o$ of the output current of the NPC type three-level inverter are expressed as Eqs. (18)–(19):

$$D(V_{\text{in}} V_o t) = \frac{\sqrt{2} V_o \sin t}{V_{\text{in}}/2} \,, \tag{18}$$

$$i_o(V_o t) = \frac{\sqrt{2} P_o \sin t}{V_o} \,, \tag{19}$$

where: $V_{\text{in}}$ is the input voltage; $V_o$ is the effective value of the output voltage; $P_o$ is the output power.

The NPC type inverter adopts SVPWM modulation strategy. The current distribution relationship of each device is shown in Table 1. All the switching tubes are IGBTs, and the diodes are recovery diodes. The power loss of the fourth bridge arm is calculated as follows (taking a-phase bridge arm failure as an example).

Table 1 and Eqs. (18)–(19) show that the loss of each switching device in the fourth bridge arm can be obtained as:

1. Upper bridge arm $S_{Z1}$

$$P_{S_{Z1}\text{con}}(V_{\text{in}}, V_o) = \frac{1}{2\pi}\int_0^{\pi} v_{CE}(i_o(V_o, t)) \cdot i_o(V_o, t) \cdot D(V_{\text{in}}, V_o, t)\,\mathrm{d}t, \tag{20}$$

Table 1. The current distribution relationship of each device under SVPWM modulation of NPC type three-level inverter

| NPC | Positive half cycle | | Negative half cycle | | Loss |
|---|---|---|---|---|---|
| | IGBT | Diode | IGBT | Diode | |
| Upper bridge arm $S_{Z1}$ | $i_o(t) \cdot D(t)$ | 0 | 0 | 0 | con swi |
| Lower bridge arm $S_{Y1}$ | $i_o(t) \cdot D(t) + \frac{i_o(t)}{2} \cdot [n1 - D(t)]$ | 0 | 0 | $\frac{i_o(t)}{2} \cdot [n1 - D(t)]$ | con Dcon Drev |
| Clamp diode $VD_{Y2}$ | / | $\frac{i_o(t)}{2} \cdot [n1 - D(t)]$ | / | $\frac{i_o(t)}{2} \cdot [n1 - D(t)]$ | con Dcon Drev |

Note: con means the IGBT conduction loss; swi means the IGBT switching loss; $D$con means the diode conduction loss; $D$rev means the diode recovery loss.

$$P_{S_{Z1}\text{swi}}(V_{\text{in}}, V_o) = \frac{1}{2\pi} \int_0^{\pi} \left[ E_{\text{on}} \frac{v_{CE}(t_{\text{on}}) i_o(V_o, t)}{V_{CE} I_c} + E_{\text{off}} \frac{v_{CE}(t_{\text{off}}) i_o(V_o, t)}{V_{CE} I_c} \right] \mathrm{d}t \cdot f_s \,, \tag{21}$$

where $v_{CE}(t_{\text{on}}) = v_{CE}(t_{\text{off}}) = \frac{V_{\text{in}}}{2}$.

2. Lower bridge arm $S_{Y2}$

$$P_{S_{Y1}\text{con}}(V_{\text{in}}, V_o) = \frac{1}{2\pi} \int_0^{\pi} \Bigg[ v_{CE}(i_o(V_o, t)) \cdot i_o(V_o t) \cdot D(t) + v_{CE}\left(\frac{i_o(V_o, t)}{2}\right) \cdot \left(\frac{i_o(V_o, t)}{2}\right) \cdot (1 - D(t)) \Bigg] \mathrm{d}t, \tag{22}$$

$$P_{S_{Y1}D\text{con}}(V_{\text{in}}, V_o) = \frac{1}{2\pi} \int_0^{\pi} \left[ v_F\left(\frac{i_o(V_o, t)}{2}\right) \cdot \left(\frac{i_o(V_o, t)}{2}\right) \cdot (1 - D(t)) \right] \mathrm{d}t, \tag{23}$$

$$P_{S_{Y1}D\text{rev}}(V_{\text{in}}, V_o) = \frac{1}{2\pi} \int_0^{\pi} \left[ \frac{i_o(V_o, t)}{2\sqrt{2} \cdot I_F} \cdot Q_{rr} \cdot V_R \right] \mathrm{d}t \cdot f_s \,, \tag{24}$$

where $V_R = \frac{V_{\text{in}}}{2}$.

3. Clamp diode $VD_{Z2}$

$$P_{VD_{z2}D\text{con}}(V_{\text{in}}, V_o) = \frac{1}{2\pi} \int_0^{\pi} \left[ v_F\left(\frac{i_o(V_o, t)}{2}\right) \cdot \left(\frac{i_o(V_o, t)}{2}\right) \cdot (1 - D(t)) \right] \mathrm{d}t, \tag{25}$$

where $V_R = \frac{V_{\text{in}}}{2}$.

# 5. Simulation study

## 5.1. Simulation model

In MATLAB/Simulink, the corresponding model of NPC three-level four-arm inverters with a fault-tolerant function is built, as shown in Fig. 3, to verify the feasibility of the fault-tolerant topology. The related parameter settings are shown in Table 2.

Table 2. Part of the project simulation parameter settings

| Project | Parameter settings |
|---|---|
| Load resistance | 12 Ω |
| Load inductance | 1 mH |
| DC voltage | 400 V |
| Midpoint capacitance | 0.0056 F |
| Fundamental frequency | 50 Hz |
| Inductance $L_1$–$L_5$ | $10^{-3}$ mH |

The insulated gate bipolar transistor (IGBT) is selected in the model, and three-level space vector pulse width modulation (SVPWM) is selected as the modulation method. This modulation method has the advantages of simple algorithm implementation, small AC ripple, and high voltage utilization. Selecting three-phase symmetrical resistance loads and parameters are shown in Table 1, the simulation time is set to $T = 0.2$ s, a-phase upper bridge arm breakdown occurs when $T = 0.08$ s, and fault-tolerant control occurs when $T = 0.1$ s.

## 5.2. Analysis of simulation results

### 5.2.1. Capacitor voltage balance simulation analysis

Figure 9 shows the waveform of the voltage difference between the upper and lower capacitors on the DC bus obtained during simulation. It can be seen from the figure that the upper and lower

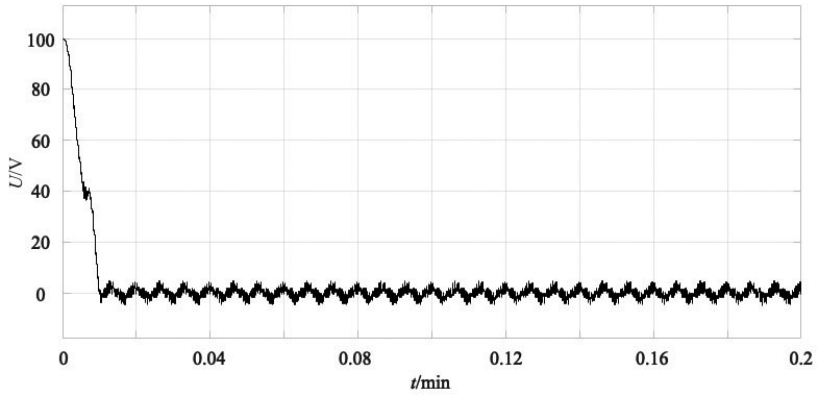


Fig. 9. Capacitance voltage difference

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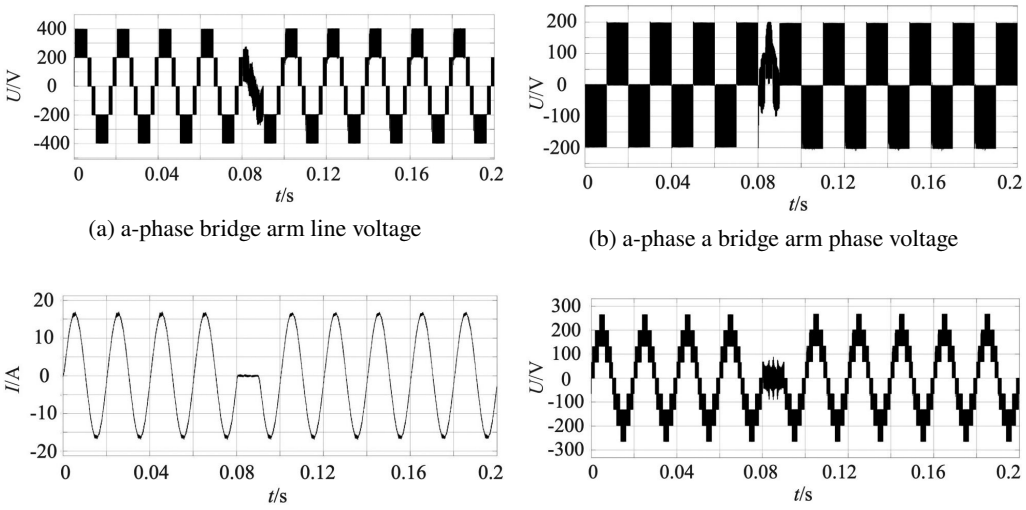
capacitor voltages are unbalanced at the initial time. When the module that suppresses the midpoint drift is connected at $T = 0.01$ s, the capacitor voltage gradually balances. The midpoint voltage balance strategy of the fourth bridge arm is good. The effect of balance controlling the drift phenomenon in the circuit is obviously suppressed.

#### 5.2.2. Voltage current simulation analysis

To analyze and compare the output waveforms before and after the fault, the waveforms in different states are intercepted during simulation more clearly. From Fig 10, the phase voltage forms a distinct step waveform, and the width of the various voltage steps changes with time, conforming to the regularity of sinusoidal waves and forming a current waveform with a high sinusoidal degree.




(a) a-phase bridge arm line voltage

(b) a-phase a bridge arm phase voltage

(c) a-phase bridge arm wire current

(d) a-phase load phase voltage

Fig. 10. Simulation waveform when a-phase bridge arm fails

Take the failure of the a-phase's upper half-bridge arm as an example, simulate the failure at $T = 0.08$ s, cut off the failed bridge arm at $T = 0.1$ s, and connect to the fourth bridge arm. Figure 10(a) shows the simulated waveform of the a-phase bridge arm line voltage, and Fig. 10(b) shows the simulated waveform of the a-phase bridge arm phase voltage. Figures 10(a)–10(b) shows that NPC type three-level inverters usually operate before $T = 0.08$ s. Currently, the output bridge arm voltage is five, and the bridge arm phase voltage is three. The open failure of a phase arm occurs at $T = 0.08$ s when the arm line voltage and phase voltage are obviously distorted. When the fourth bridge arm is connected at $T = 0.1$ s, and the inverter is fault-tolerantly controlled, the line voltage and phase voltage output waveforms return to normal and are the same as those during regular operation.

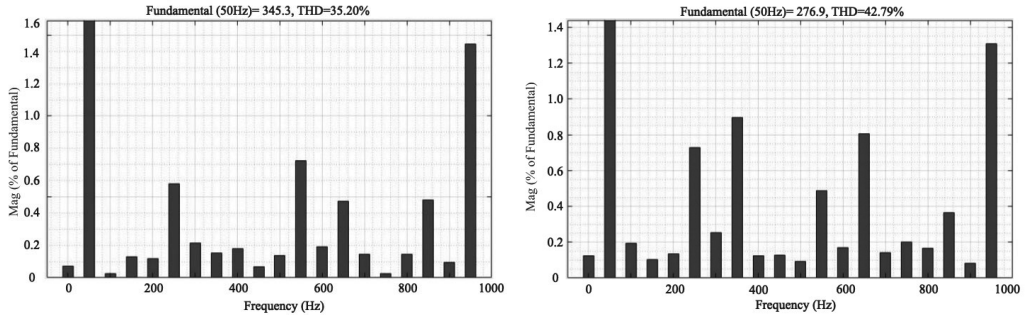
Figure 10(d) shows the simulated waveform of the arm line current of a-phase bridge. The NPC three-level inverter usually works, and the output line current is a sinusoidal waveform.

When $T = 0.08$ s, the open-circuit fault of the upper arm of a-phase bridge occurs. Currently, the positive half-cycle waveform of the line current becomes 0, it is distorted. When $T = 0.1$ s, the fourth bridge arm is connected to perform fault-tolerant control of the inverter, and the line current waveform returns to normal, which is the same as during regular operation.

Figure 10(d) shows the simulated waveform of a-phase loading phase voltage. The NPC type three-level inverter usually works, and the output load phase voltage is nine levels. When $T = 0.08$ s, the open-circuit failure of the upper arm of the a-phase bridge occurs; when the positive half-wave periodic output of the load phase voltage changes to 0, a period of zero level occurs. When $T = 0.1$ s, the fourth bridge arm is connected to perform fault-tolerant control of the inverter, and the load phase voltage returns to normal, which is the same as during regular operation.

#### 5.2.3. Output line voltage spectrum analysis

The spectrum analysis of the output phase voltage waveform before and after the fault tolerance is shown in Fig. 11. Figure 11(a) is the spectrum analysis diagram of the output line voltage before the fault-tolerant control. At this time, the inverter is in the normal operation stage and has not failed. Currently, THD = 35.20%. Figure 11(b) is the output line voltage spectrum analysis diagram after fault-tolerant control. At this time, the inverter fails, and the fourth bridge arm is connected for fault-tolerant operation. Currently, the THD = 42.79%. Before and after the fault-tolerant operation, its THD increased from 35.20% to 42.79%. The total harmonic of the output phase voltage does not change much, and it has a specific suppression effect on the harmonic distortion of the output line voltage.



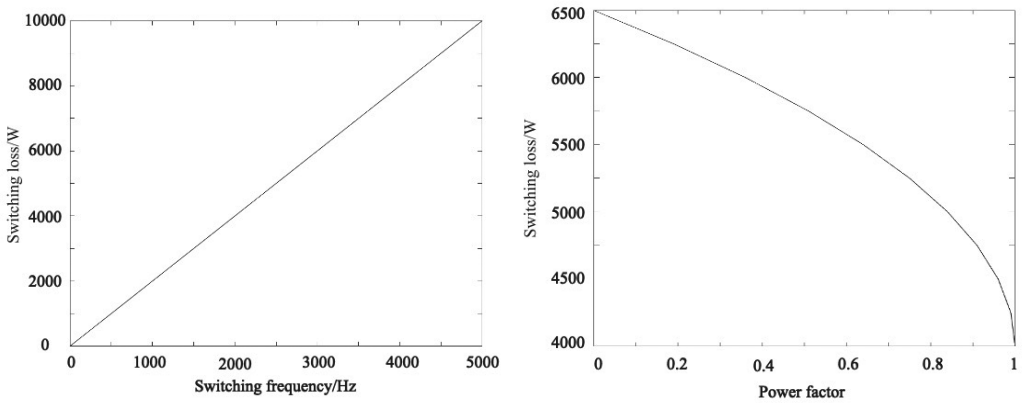

(a) Voltage spectrum during normal operation (b) Voltage spectrum during fault-tolerant operation

Fig. 11. Output phase voltage spectrum analysis

#### 5.2.4. Power loss analysis

Through simulation, the power loss is analyzed. The switching loss calculation model shows that the switching loss of a three-level inverter is related to the load, switching frequency, power factor, and dynamic characteristics of power devices. The new topological structure and diode material (SiC) change the dynamic features of the device to reduce losses. According to the switching loss calculation model, the relationship between the switching loss, switching

frequency, and power factor is established in Fig. 12. Figure 12(a) shows that the switching loss has a linear relationship with the switching frequency, and Fig. 12(b) shows that the switching loss decreases as the power factor increases.




(a) Switching frequency changes

(b) Power factor changes

Fig. 12. The relationship between switching loss, switching frequency and power factor

According to the conduction loss calculation model, it can be seen that the conduction loss has nothing to do with the switching frequency. According to the calculation model, the inverter's relationship between the conduction loss and the power factor is obtained when the inverter is working. The impact of the failure is not significant (Fig. 13).

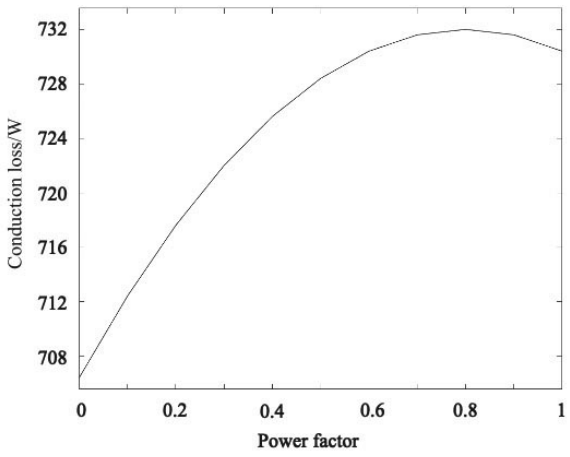



Fig. 13. The relationship between conduction loss and power factor

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## 6. Conclusion

A new three-level four-leg topology of the NPC inverter proposed in this paper can realize regular operation, adjust the neutral point voltage, and switch the half leg for fault-tolerant control after failure. The simulation results verify its rationality, but experiments have not confirmed it, and further investigations are needed to verify its feasibility and reliability. Although the added fourth bridge arm increases the cost, it makes the corresponding SVPWM strategy simpler and can effectively reduce the switching loss of the IGBT. The IGBT in the fourth bridge arm needs to bear a higher voltage, so it is put forward higher requirements for the withstand voltage of the IGBT. If the structure can be optimized, its voltage would be further reduced and the value of the fault-tolerant topology will be improved.

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