Metrol. Meas. Syst., Vol. 31 (2024) No. 3, pp. 547–564
DOI: 10.24425/mms.2024.150285

PAN POLSKA AKADEMIA NAUK

METROLOGY AND MEASUREMENT SYSTEMS
Index 330930, ISSN 0860-8229
www.metrology.wat.edu.pl

M&MS

HIGH-RESOLUTION WAVEFORM SYNTHESIS BASED ON PHASE-AMPLITUDE MAPPING

Xin Ai, Zaiming Fu, Hanglin Liu, Dexuan Kong

University of Electronic Science and Technology of China, School of Automation Engineering, Chengdu 611731, China
(✉ *fuzaimin@163.com*)

Abstract

With rapid updating of semiconductor technology and continuous development of large-scale integrated circuits, the device under test has higher and higher requirements for the resolution, accuracy, and waveform modulation of the stimulation signal source. The traditional method of creating digital waveforms involves employing direct digital synthesis technology. However, the sampling rate and memory depth easily limit the adjustment range and resolution of its waveform timing parameters, and it is not easy to adjust the internal parameters of the waveform. Therefore, it is essential for modern electronic technology to further improve the programmability of synthesized waveforms under the condition of a limited sampling rate and memory. This paper presents a real-time waveform synthesis method using phase-amplitude mapping. The proposed method allows for arbitrary waveform generation without memory constraints and improved timing resolution. The sampling rate no longer limits the resolution of the device. It offers amplitude, frequency, phase, and pulse-width modulation for the test device. In addition, a low-cost, no-memory, full-phase, parallel waveform synthesizer is realized on the hardware platform of "FPGA+DAC". Finally, in this paper, the resolution of the synthesized waveforms based on a Xilinx FPGA and a DAC is improved by a factor of 4 compared to the sampling time.

Keywords: waveform synthesis, real-time computation, waveform modulation, timing resolution.

1. Introduction

Electronic equipment plays an important role in our world, and the stimulation signal source, as an important testing tool in the field of electronic testing, plays a very important role in semiconductor testing, electronic countermeasure systems, quantum physics experiments, automatic control fields, and communication systems [1–6]. With continuous development of semiconductor processes and integrated circuits, new requirements have been put forward for the accuracy, resolution, and modulation function of stimulation signals [3, 6–9].

The traditional analog method of synthesizing waveforms is mainly based on resonance circuits, shaping technology, and special semiconductor devices, which are the basis of the pulse waveform

Article history: received January 25, 2024; revised March 14, 2024; accepted March 21, 2024; available online June 12, 2024.

synthesis method. The analog synthesis method first generates a rectangular pulse waveform from the main oscillator circuit and then adjusts the signal delay time through "signal timing". "Waveform shaping" is the manipulation of rectangular pulse signal parameters for control and shaping. Finally, through the output channel signal conditioning, the control of the pulse waveform amplitude and level is completed [10]. The circuit design of this method is extremely complex, and it is not easy to realize the high-resolution adjustment of pulse waveform parameters. At the same time, its waveform programmability is insufficient, and it is not easy to realize the diversity and complexity of the pulse waveform.

The current digital synthesis waveform modulation method is mainly based on the *direct digital synthesis* (DDS) technology [11, 12], which is divided into *direct digital frequency synthesis* (DDFS) and *direct digital waveform synthesis* (DDWS), with the structure shown in Fig. 1.

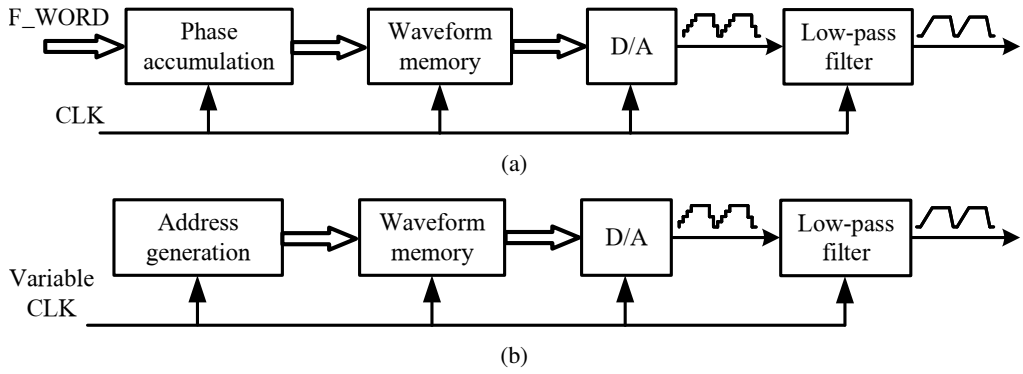


Fig. 1. (a) DDFS architecture, (b) DDWS architecture.

A fixed-frequency sampling clock drives the DDFS, and a bit-width N-phase accumulator accumulates steps of the frequency control word F_WORD at each sampling clock. For each sampling clock, the high M bits of the summed result are intercepted as the address for addressing the waveform memory, which outputs the waveform samples and feeds them into the DAC. The frequency resolution in a synthesized and modulated signal depends on the frequency of the sampling clock and the number of bits used in the phase accumulator. However, the phase accumulator can only alter the frequency of the pulsed waveform and cannot modify the stored waveform samples. It is impossible to achieve fast modulation of the rise/fall time or pulse width using the phase accumulator.

DDWS ensures that the waveform samples in the memory are output point by point by changing the fixed clock in DDFS into a variable clock. The variable clock guarantees the output waveform frequency. The modulation to generate a new frequency must be realized by changing the frequency of the sampling clock or the number of data points in the waveform memory. Thus, the method is subject to significant limitations to achieve a high resolution [13]. That is, the traditional method of digital waveform synthesis involves addressing the output of waveform sample points to obtain a digital waveform sample point [14]. However, this method has certain limitations. The performance of the synthesized waveform is limited by the capacity of the lookup table, which can affect the timing resolution of the synthesized waveform and result in waveform jitter. Additionally, it is impossible to adjust the waveform's internal parameters using this method. In actual engineering applications, the waveform lookup table will also increase the complexity of the hardware circuit structure [15, 16].

This paper proposes a real-time calculation method for waveforms, which generates them in real time by mapping their amplitude and phase. This method is not limited by the memory depth, can accurately get the sample point value of each phase without phase truncation error, improves the waveform timing resolution, can accurately reconstruct high-quality waveforms, and is easier to realize the modulation of the waveform.

The rest of the paper is organized in the following sections. In Section 2, the waveform computational synthesis technique is described. In Section 3, waveform modulation based on this method is investigated. Section 4 verifies the feasibility and effectiveness of this method. Finally, conclusions are drawn in Section 5.

2. Research on waveform synthesis techniques

Traditional digital waveform synthesis involves using memory addresses to generate waveform data and producing analog waveforms via a DAC. However, this method requires a large storage capacity to capture waveform details, and the DAC's sampling rate limits the waveform resolution. Increasing storage capacity and improving the sampling rate of the DAC can be costly and difficult. On the other hand, DACs usually have high vertical resolution. Therefore, this paper proposes a real-time waveform calculation method based on phase-amplitude mapping. This method sacrifices amplitude resolution for time resolution, reducing computational resource consumption and improving real-time calculation efficiency.

2.1. Principle of waveform synthesis based on phase-amplitude mapping

Any periodic signal can be expressed as $f(t) = f(t + kT)$. In order to accurately describe the waveform, t and T in the expression should be of infinite precision, but it is impossible to realize the infinite precision calculation and representation of the numbers in the actual design, *i.e.*, there is a certain error in both. In order to reduce the complexity and error caused by the large number of multiplication and division operations involved in the time domain calculation of the waveform, the time t is mapped to phase φ. The periodic signal phase value is $0 \sim 2\pi 0 \sim 2\pi$, *i.e.*, the periodic signal can be expressed as:

$$f\left(\frac{\varphi \times T}{2\pi}\right) = f\left(\frac{\varphi \times T}{2\pi} + kT\right). \tag{1}$$

To realize this in a digital system, phase 2π is quantized to 2^N, *i.e.*, it is the equalization of the signal period T into 2^N with a time domain resolution:

$$T_{\text{res}} = \frac{T}{2^N}. \tag{2}$$

The signal is mapped and quantized as described above, and it can be represented as:

$$f(t) \to f\left(\frac{T}{2^N} \cdot p\right) \to f\left(\frac{2\pi}{2^N} \cdot p\right) \to g(p), \tag{3}$$

where p is the mapped quantized phase value, and N is the phase quantization bit width in binary. The waveform amplitude is transformed with time in the time domain, *i.e.*, the corresponding amplitude is transformed by the phase value p. The time t is accumulated under the sampling

clock by $t = N_s \times T_s$, where T_s is the sampling period, $N_s = 0, 1, 2...$, and the phase value p is accumulated under the control of the sampling clock by FTW:

$$p_{n+1} = p_n + FTW, \tag{4}$$

where $FTW = \dfrac{2^N}{T f_s}$. The waveform phase-amplitude mapping relationship is shown in Fig. 2.

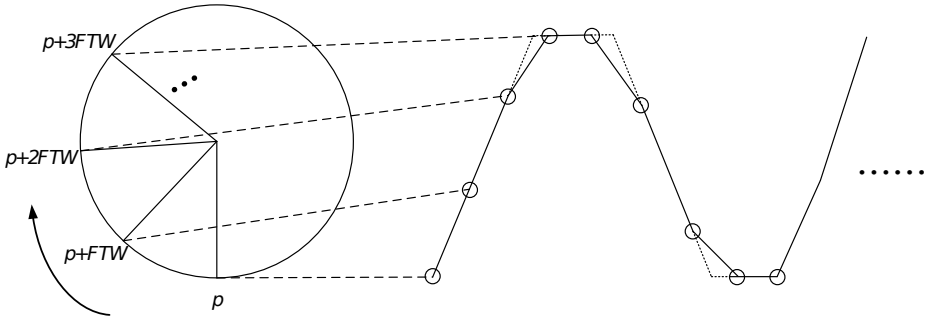


Fig. 2. Waveform phase-amplitude mapping relation.

The phase value p, in the phase-amplitude mapping method, is accumulated by FTW. An overflow is generated when p reaches 2^N. The overflow is automatically accomplished with a truncation of the bit width N, *i.e.*, it can be expressed as the residual portion of the p-value when it is accumulated over in the binary calculation. For example, when $N = 4$, $FTW = 3$, and $p_0 = 0$ are analysed with a sine wave of amplitude 1 and initial phase 0°, the schematic is shown in Fig. 3.

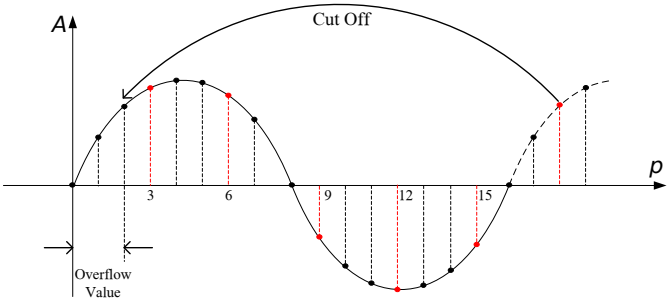


Fig. 3. Diagram of the phase overflow.

Fig. 4 shows a block diagram of the waveform synthesis principle based on phase-amplitude mapping, in which the phase control module is used to calculate the phase value p, and the phase-amplitude mapping calculation module maps p to an amplitude value through (3), which is finally converted to an analog waveform by the digital to analog converter module.

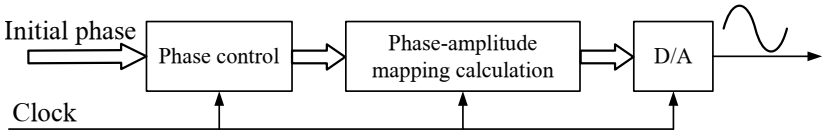


Fig. 4. Block diagram of the phase-amplitude mapping waveform synthesis principle.

Metrol. Meas. Syst., Vol. 31 (2024), No. 3, pp. 547–564
DOI: 10.24425/mms.2024.150285

It can be analysed from the principle elaboration above that, in the principle of waveform synthesis based on phase-amplitude mapping, the maximum phase value 2^N and the sampling clock frequency f_s determine the frequency resolution f_{res}, and the frequency f of the waveform is controlled by the frequency control word FTW and the sampling clock frequency f_s together, and its relation equation is:

$$f = \frac{FTW}{2^N} \cdot f_s \rightarrow f_{\text{res}} = \frac{f_s}{2^N}. \tag{5}$$

2.2. Periodic waveform synthesis method based on phase-amplitude mapping

As a periodic waveform, the pulse signal has very typical timing characteristics. As an example, the pulse signal is analysed using the phase-amplitude mapping method proposed in Section 2.1. Fig. 5 shows the pulse waveform definition and the pulse waveform after phase-amplitude mapping, where the high and low levels of the pulse signal are V_H and V_L, respectively; the period of the pulse signal is T; the rise time T_r is the time when the level transitions from 10% to 90% of the amplitude; the fall time T_f is the time when the level transitions from 90% to 10% of the amplitude; the pulse width T_w is the time when the high level of the pulse is included in the transition from 50% amplitude in the rising edge to 50% amplitude in the falling edge.

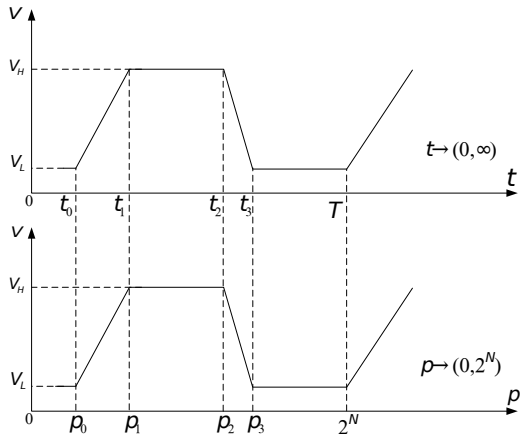


Fig. 5. Pulse waveform state transfer phase diagram.

As can be seen from Fig. 5, the expression of the pulse signal waveform in the time domain is a segmented function, which contains several segmentation points, the beginning of the period of the pulse waveform t_0, the end of the rising edge t_1, the end of the high level t_2, the end of the falling edge t_3, and the end of the period of the pulse waveform T. Adjacent segmentation points divide the pulse waveform into four segments: the rising edge, the high level, the falling edge, and the low level. Therefore, state judgment is needed to select the correct functional equation when calculating the amplitude value according to the phase.

According to the functional relationship of the pulse waveform in the time domain in Fig. 5, the following mathematical expressions for each state can be obtained.

Rising edge:

$$Y_1 = K_r \cdot t, \tag{6}$$

where $K_r = \dfrac{V_H - V_L}{t_1 - t_0}$, $t \in [t_0, t_1)$

High level:

$$Y_2 = V_H, \quad t \in [t_1, t_2). \tag{7}$$

Falling edge:

$$Y_3 = K_f \cdot t - K_f \cdot t_2 + V_H, \tag{8}$$

where $K_f = \dfrac{V_H - V_L}{t_2 - t_3}$, $t \in [t_2, t_3)$.

Low level:

$$Y_4 = V_L, \quad t \in [t_3, T) \tag{9}$$

Mapping time to phase, t_0, t_1, t_2 and t_3 are mapped to p_0, p_1, p_2 and p_3. The mapping relation is as in (10).

$$p = \frac{2^N}{T} \cdot t \rightarrow T = \frac{2^N}{FTW} \cdot T_s \tag{10}$$

From the pulse parameter definitions, it is possible to calculate the time domain interval markers in relation to the pulse parameters, as shown below:

$$\begin{cases} t_1 = \dfrac{T_r}{80\%} + t_0 \\ t_2 = T_w + t_0 + \dfrac{T_r}{1.6} - \dfrac{T_f}{1.6} \\ t_3 = T_w + t_0 + \dfrac{T_r}{1.6} + \dfrac{T_f}{1.6} \end{cases} \tag{11}$$

Substituting (11) into (6) to (9), the expression of the function based on the phase-amplitude mapping of the pulse waveform in the time domain is calculated as follows.

Rising edge:

$$Y_1 = K_{pr} \cdot p, \tag{12}$$

where $K_{pr} = \dfrac{V_H - V_L}{p_1 - p_0}$, $p \in [p_0, p_1) \rightarrow \dfrac{2^N}{T} \cdot t_0 \le p < \dfrac{2^N}{T} \cdot \left(\dfrac{T_r}{80\%} + t_0 \right)$

High level:

$$Y_2 = V_H, \quad p \in [p_1, p_2) \rightarrow \frac{2^N}{T} \cdot \left(\frac{T_r}{80\%} + t_0 \right) \le p < \frac{2^N}{T} \cdot \left(T_W + t_0 + \frac{T_r}{1.6} - \frac{T_f}{1.6} \right) \tag{13}$$

Falling edge:

$$Y_3 = K_{pf} \cdot p - K_{pf} \cdot p_2 + V_H K_{pf} = \frac{V_H - V_L}{p_2 - p_3} p \in [p_2, p_3)$$

$$\downarrow$$

$$\frac{2^N}{T} \cdot \left(T_W + t_0 + \frac{T_r}{1.6} - \frac{T_f}{1.6} \right) \le p < \frac{2^N}{T} \cdot \left(T_W + t_0 + \frac{T_r}{1.6} + \frac{T_f}{1.6} \right) \tag{14}$$

Low level:

$$Y_4 = V_L, \quad p \in \left[p_3, 2^N \right) \rightarrow \frac{2^N}{T} \cdot \left(T_W + t_0 + \frac{T_r}{1.6} + \frac{T_f}{1.6} \right) \le p < 2^N \tag{15}$$

The phase p in (12) to (15) is generated by accumulating in steps of FTW driven by the sampling clock, and the phase generated by accumulating overflows due to the phase bit width

Metrol. Meas. Syst., Vol. 31 (2024), No. 3, pp. 547–564
DOI: 10.24425/mms.2024.150285

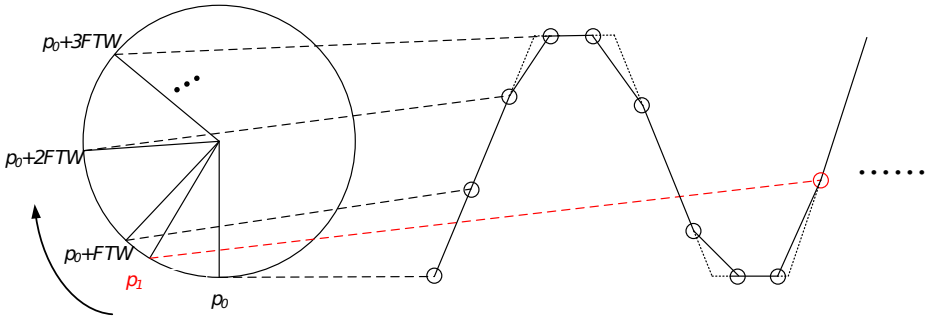


Fig. 6. Schematic of pulse waveform with the non-integer multiple sampling rate.

of N. After truncation, it becomes the initial phase of the next cycle. As shown in Fig. 6, when the sampling frequency is a non-integer multiple of the pulse frequency, the phase of the first waveform sample point of each cycle of the digital waveform is not the same, and p_0 in the figure is the first cycle starting sample point, and p_1 is the second cycle starting sample point.

Based on the waveform synthesis block diagram shown in Fig. 4, the phase-amplitude mapping calculation module is expanded in accordance with the pulse waveform function expression to obtain the phase-amplitude mapping-based pulse waveform synthesis block diagram shown in Fig. 7.

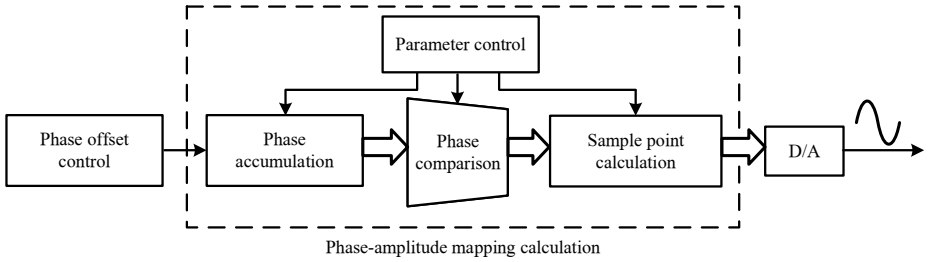


Fig. 7. Block diagram of the pulse waveform synthesis principle.

The phase accumulation module is used to accumulate the phase values in steps *FTW* at each clock cycle after the waveform is mapped from time domain t to phase φ. The phase comparison module is used to determine the waveform segment to which the sampled points belong according to the phase of the sampled points. The phase comparison module is used to determine the waveform segment according to the phase of the sampling points. The parameters required in the pulse waveform synthesis process are generated by the waveform parameter control module, which generates the phase interval markers p_0, p_1, p_2, p_3 and the frequency control word *FTW* based on the calculation of the pulse waveform parameters, and the corresponding calculation formula is shown in (10).

3. Waveform modulation techniques based on phase-amplitude mapping

The phase-amplitude mapping-based waveform generation method generates waveforms in real time with the use of phase-amplitude mapping, and does not require pre-storage of waveform sample data. The synthesized waveform parameters are variable and can be modified during the

waveform sample point synthesis without interrupting or resetting the process. In other words, the phase-amplitude mapping method can generate not only waveforms in real time but also complete waveform modulation in real time. The following is an example to illustrate the modulation waveform synthesis method based on phase-amplitude mapping for pulse waveforms.

Finally, this paper presents amplitude modulation, frequency modulation, and phase modulation based on the phase-amplitude mapping waveform modulation technique, and its modulation principle block diagram is shown in Fig. 8.

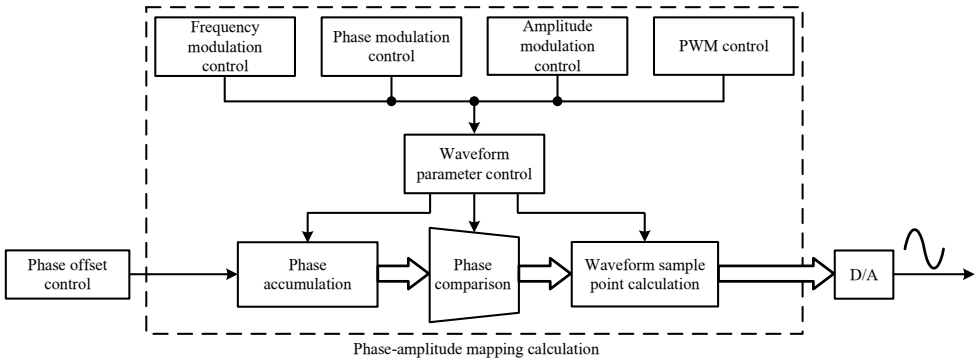


Fig. 8. Block diagram of the phase-amplitude mapping based waveform modulation principle.

3.1. Amplitude modulation

In amplitude modulation, the amplitude of the carrier is required to transform with the modulating signal [17,18]. For example, a sinusoidal carrier with a frequency of f_c and an amplitude of A: $S_c(n) = A_c \cdot \cos(2\pi f_c n + \phi_c)$. The modulating waveform is $S_m(n) = A_m \cdot \cos(2\pi f_m n + \phi_m)$. The modulation result $S_{AM}(n) = [1 + k_a \cdot \cos(2\pi f_m n + \phi_m)] \cdot A_c \cdot \cos(2\pi f_c n + \phi_c)$, where $k_a = \dfrac{A_m}{A_c}$ is a constant, is called the modulation sensitivity that generates the amplitude modulation signal, the mathematical model shown in Fig. 9.

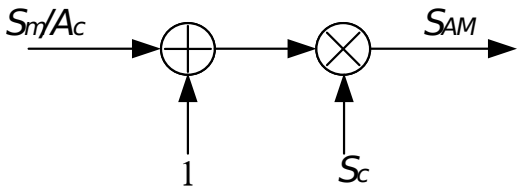


Fig. 9. Amplitude modulation mathematical model.

Amplitude modulation means multiplying with the modulating waveform after the waveform samples are generated, and its expression is shown in (16).

$$S_{AM}(n) = \left[1 + \frac{S_m(n)}{A_c}\right] \cdot S_c(n) = [1 + k_a \cdot S_m(n)] \cdot S_c(n) \tag{16}$$

The amplitude modulation process will make the digital waveform sample points generated by the phase-amplitude mapping module calculation exceed the quantization range of the digital to analog converter, and thus the mapping should be normalized again after multiplying with the modulation wave, and the amplitude modulation structure block diagram is shown in Fig. 10.

Metrol. Meas. Syst., Vol. 31 (2024), No. 3, pp. 547–564
DOI: 10.24425/mms.2024.150285

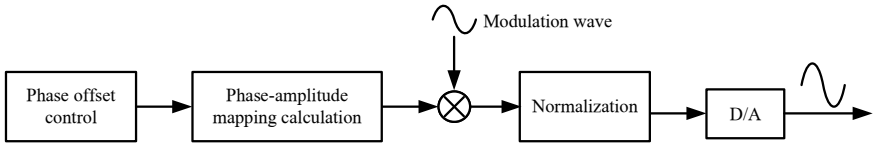


Fig. 10. Block diagram of the amplitude modulation structure.

3.2. Frequency modulation

In frequency modulation, the frequency of the carrier is required to follow the amplitude of the modulating signal in equal proportions [19], as shown schematically in Fig. 11. The modulating source signal $S_m(t)$ is digitized, and its digitized expression is shown in (17).

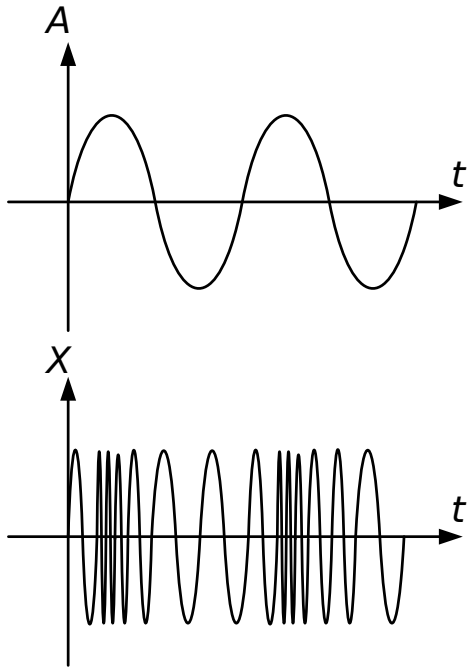


Fig. 11. Frequency modulation diagram.

$$S_m(n) = A[A_{\text{offset}} + f(n)], \tag{17}$$

where A represents the amplitude of the modulation source signal, and A_{offset} represents the phase offset of the modulation source signal, the mathematical expression for frequency modulation is shown in (18).

$$\begin{cases} S_{\text{FM}}(n) = A_c \cos[(2\pi f_c + k_{\text{FM}} S_m(n))n + \phi_c] \\ f_{\text{FM}} = f_c + \Delta f \cdot S_m(n) = f_c + \dfrac{k_{\text{FM}} \cdot S_m(n)}{2\pi} \end{cases}, \tag{18}$$

where f_{FM} is the frequency of the modulated waveform, f_c is the carrier centre frequency, and Δf is the maximum frequency deviation in the same direction with respect to f_c. The modulation mathematical expression in the phase-amplitude mapping method transforms to (19). The frequency

control word in (19) is obtained from the frequency calculation, and the FTW_{FM} and ΔFTW are calculated with respect to the frequency in the same way as the FTW calculation, as shown in (20).

$$FTW_{\mathrm{FM}} = FTW + \Delta FTW \cdot S_m(n) \tag{19}$$

$$\Delta FTW = \frac{\Delta f}{f_s} 2^N = 2^N \frac{f_c + (k_{\mathrm{FM}}/2\pi)[A(A_{\mathrm{offset}} + f(n))]}{f_s} \tag{20}$$

3.3. Phase modulation

In phase modulation, it is required that the deviation of the carrier's phase from its reference phase varies proportionally with the instantaneous value of the modulating signal [20, 21]. When $S_m(n)$ is the modulating signal, and the carrier is $S_c(n) = A_c \cos(2\pi f_c n + \phi_c)$, the mathematical expression after phase modulation is shown in (21).

$$S_{\mathrm{PM}}(n) = A_c \cos(2\pi f_c n + k_{\mathrm{PM}} S_m(n) + \phi_c), \tag{21}$$

where k_{PM} is the phase deviation coefficient.

The phase modulation in the phase-magnitude mapping may correspond to the process of calculating the phase p in the phase-magnitude mapping calculation module, as shown in (22).

$$p_{n+1} = p_n + FTW + \Delta p_m \cdot S_m(t), \tag{22}$$

where Δp_m corresponds to a quantization calculation at the N bit, calculated as shown in (23).

$$\Delta p_m = \frac{\Delta p}{2\pi} \cdot 2^N = 2^N \frac{\phi_c + k_{\mathrm{PM}}[A(A_{\mathrm{offset}} + f(n))]}{2\pi} = \phi_1 + \phi_2 f(n), \tag{23}$$

where ϕ_1 is the initial phase value, and $\phi_2 f(n)$ is varied according to the trend of the amplitude of the modulation source signal by a factor of ϕ_2, which can be called the phase step parameter.

3.4. Pulse-width modulation

In addition to amplitude modulation, frequency modulation, and phase modulation, which are the three basic signal modulations, *pulse-width modulation* (PWM) is also used for pulse waveforms. PWM is a type of modulation that changes the pulse width according to the modulating signal [22, 23], which is shown schematically in Fig. 12.

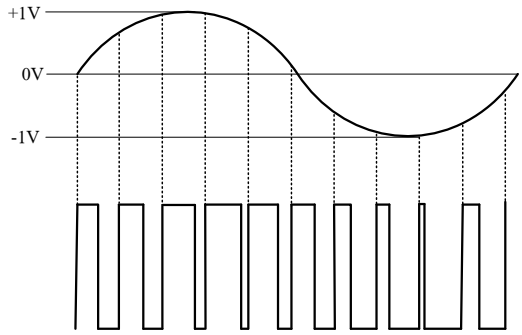


Fig. 12. Schematic diagram of the PWM waveform.

The PWM function is completed by using the framework of "storage + real-time calculation", as shown in Fig. 13, which mainly consists of the PWM parameter addressing module, PWM parameter storage module, parameter passing judgment module, and waveform calculation module.

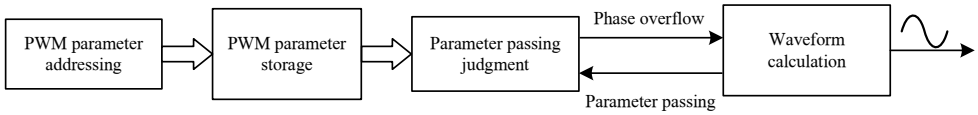


Fig. 13. Block diagram of PWM realization.

When the PWM parameter addressing module addresses the PWM parameter storage module, the address p_{pwm} is cumulative with the frequency control word FTW_{pwm}. The formula for FTW_{pwm} is shown in (24).

$$FTW_{\text{pwm}} = \frac{f_{\text{pwm}} \times 2^{D}}{f_s}, \tag{24}$$

where f_{pwm} is the modulating waveform frequency, f_s is the sampling frequency, and D is the memory address binary bit width. The formula for addressing address p_{pwm} is shown in (25).

$$p_{\text{pwmn+1}} = p_{\text{pwmn}} + FTW_{\text{pwm}} \tag{25}$$

The PWM parameter storage module stores the PWM parameters required for the pulse in real time according to the parameter settings; the parameter passing judgment module is used to determine whether the PWM parameters are transferred to the waveform calculation module.

4. Method validation

4.1. Waveform synthesis general scheme

As shown in Fig. 14, the overall scheme design of the waveform synthesis module consists of a host computer, FIFO, clock management, waveform calculation module, high-speed data parallel-serial conversion module, DAC, and low-pass filter.

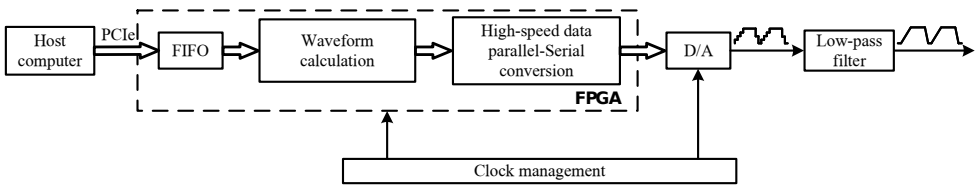


Fig. 14. System block diagram.

The FPGA receives detailed information about waveform frequency, rise time, fall time, pulse width, and other parameters from the host for logical processing. This communication takes place via the PCIe interface, and the information is then transferred across the clock domain through a FIFO. The waveform calculation module performs logical processing on the pulse waveform parameters under the system clock and calculates the digital samples of the pulse waveform. The clock management generates the clock required for FPGA operation. The high-speed data parallel-serial conversion module converts the parallel-computed waveform data into serial data.

The digital to analog converter implements the analog signal output. The low-pass filter filters out the mirror frequency and other spurious signals to obtain a relatively pure pulse waveform. The final system realizes a waveform sampling rate of 2.5 GSa/s, using 8-channel parallel computing, and the FPGA works at 156.25 MHz.

4.2. Simulation verification

The correctness of the phase-amplitude mapping method is verified by a Vivado simulation. The simulation target waveform is a pulse signal with a rise time $T_r = 20ns$, pulse width $T_w = 50ns$, and fall time $T_f = 20ns$. The simulation results are shown in Fig. 15. By comparing Fig. 15 and Fig. 16, it can be seen that the phase-amplitude mapping method is able to realize the waveform modulation.

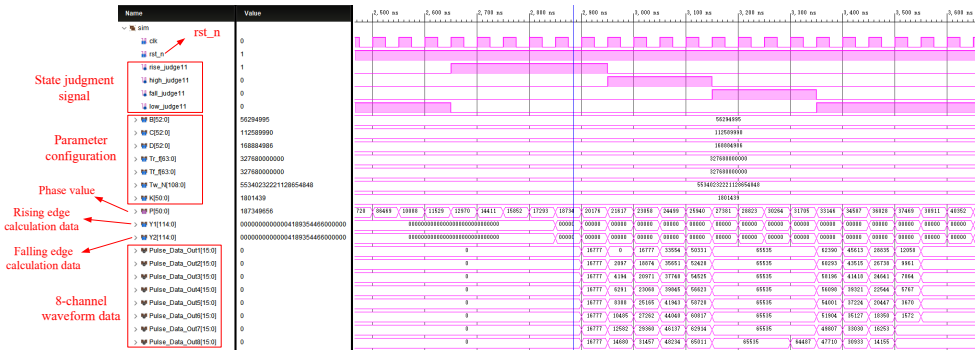


Fig. 15. 50 ns pulse width simulation.

As can be seen from the figure, when the corresponding waveform parameters are input, the phase value p will be accumulated continuously, the current state of the waveform is judged by p, and the target waveform parameters and the waveform data are calculated in real by segmentation. The final output is 8-channel parallel waveform data.

When the pulse width T_w is changed, the rise time and fall time remain unchanged, and the final simulation result is shown in Fig. 16.

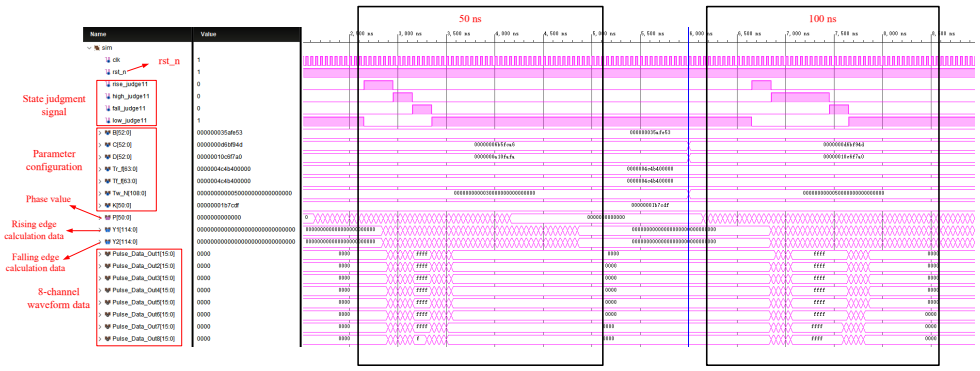


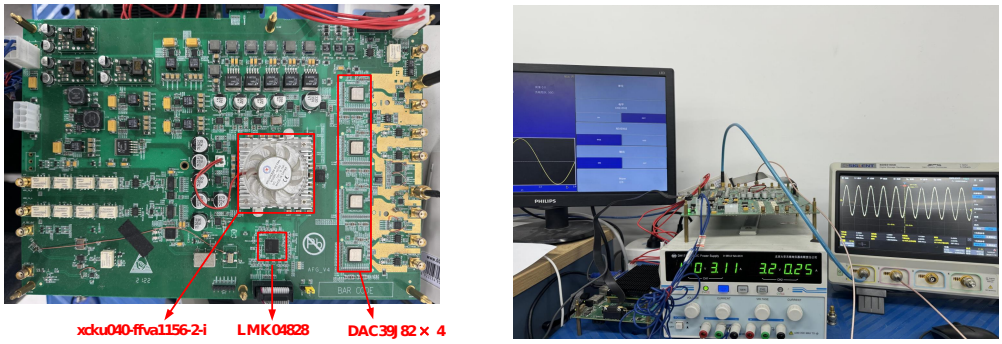
Fig. 16. 50 ns to 100 ns pulse width simulation.

Metrol. Meas. Syst., Vol. 31 (2024), No. 3, pp. 547–564
DOI: 10.24425/mms.2024.150285

4.3. Testing and analysis

As per the program's design, this paper utilizes Xilinx's Kintex UltraScale series xcku040-ffva1156-2-i as the FPGA. The DAC chip used is TI's DAC39J82, the clock management chip is TI's LMK04828, as displayed in Fig. 17a. The primary modules' resource occupancy is shown in Table 1.

A hardware testbed was created to assess the feasibility of the method. Fig. 17b shows the setup used for testing. The test platform consisted of an SDS5104X oscilloscope with a 1 GHz bandwidth and 5 GSa/s sampling rate. Additionally, an industrial control computer equipped with an MIO-3260LZ22GS8A1E motherboard was utilized. A traditional DDS was also implemented under the same conditions to compare the performance for harmonic problems and synthesized waveforms.



(a) (b)

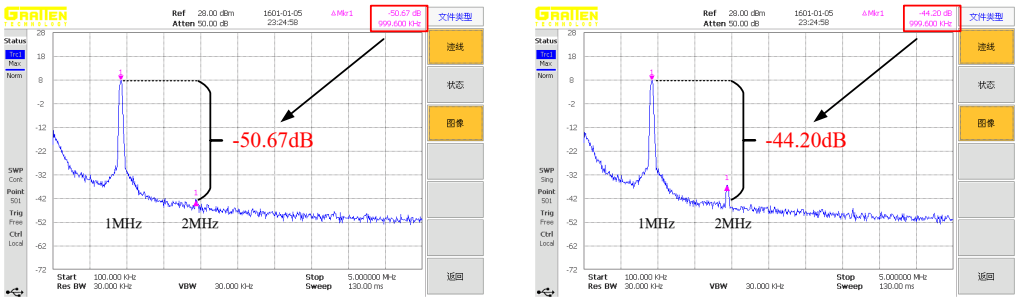
Fig. 17. (a) Hardware platform, (b) test platform.

Table 1. Consumption of logic resources of the FPGA device.

	Total LUTs	Logic LUTs	LUTRAMs	SRLs	FFs	RAMB36	RAMB18	URAM	DSP48 Blocks
Wave_syn	6822	4289	0	2533	8655	0	0	0	192
Modulation	42	222	8	198	1150	6	0	0	29
Pcie_top	22360	19231	3113	16	17940	20	12	0	0
Jesd204_top	3232	3195	0	37	3372	0	0	0	0

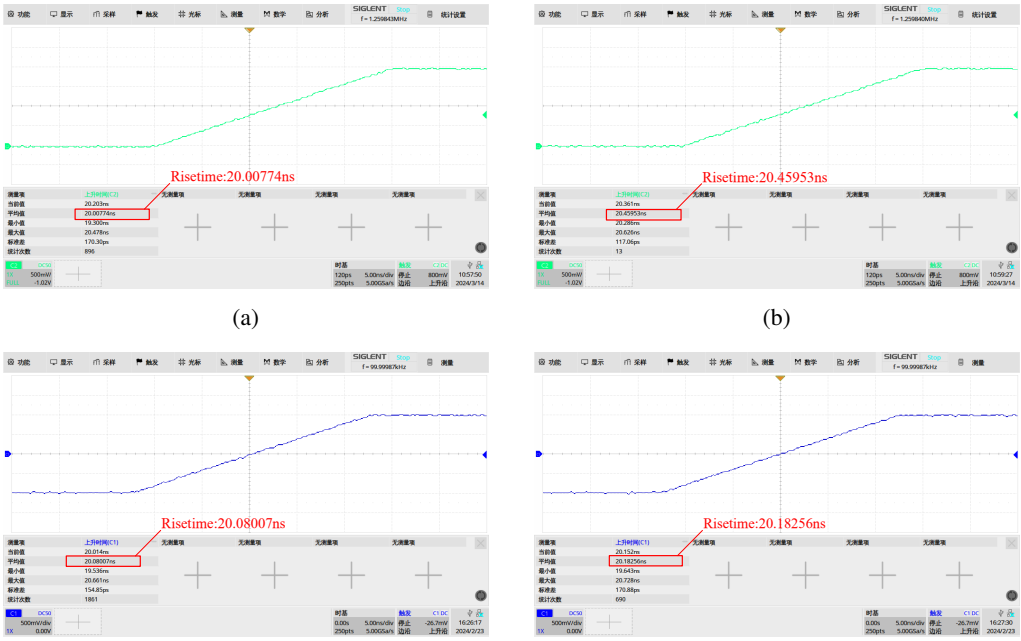
Direct digital synthesis techniques suffer from harmonic distortion due to their discrete, limited sampling rate, phase truncation, and limited waveform memory capacity. Real-time computation based on phase-amplitude mapping can significantly reduce the harmonics of the synthesized waveforms compared to the traditional DDS method. Fig. 18 shows the spectrum of a sine wave with a frequency of 1 MHz synthesized by conventional DDS and a method based on phase-amplitude mapping.

When using the same hardware and software platform and test conditions, a conventional DDS achieves a step from 20 ns to 20.4 ns on the rising edge. However, this method requires a large memory capacity to achieve a resolution of 400 ps. On the other hand, the phase-amplitude mapping-based method achieves a step from 20 ns to 20.1 ns on the rising edge, resulting in a final resolution of 100 ps. This demonstrates the superiority of this method. The test results are shown in Figure 19.



(a) (b)

Fig. 18. (a) Waveform synthesis based on phase-amplitude mapping, (b) traditional DDS.



(a) (b)

(c) (d)

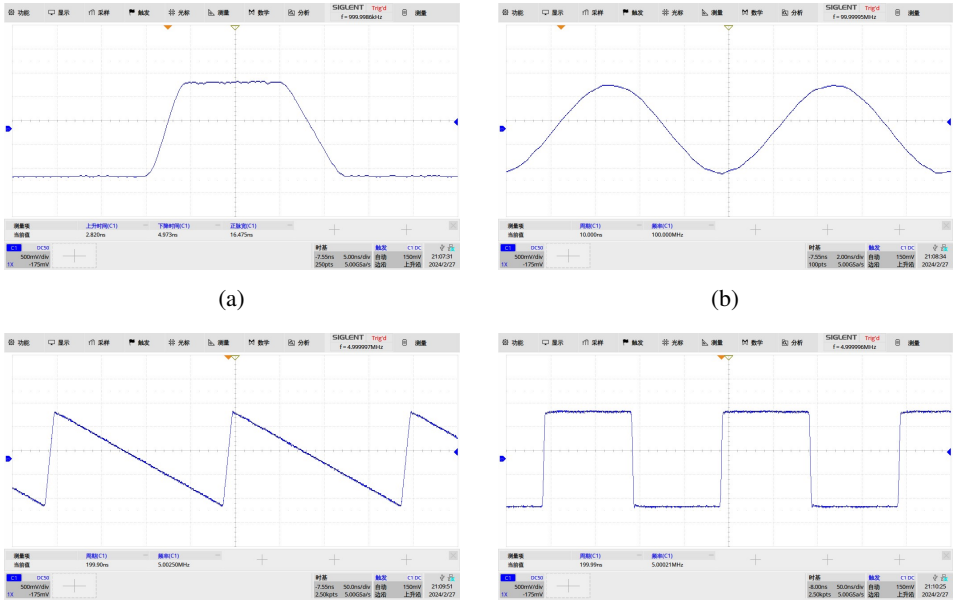
Fig. 19. (a) Traditional DDS 20.00774 ns rise time, (b) traditional DDS 20.45953 ns rise time, (c) mapping method 20.08007 ns rise time, (d) mapping method 20.18256 ns rise time.

In order to verify the feasibility of this method, tests were conducted to synthesize pulse, sine wave, ramp wave, and square wave, as shown in Figure 20.

Figure 21 shows four modulated waves, amplitude modulation, frequency modulation, phase modulation, and PWM, to verify the feasibility of this method of waveform modulation.

The test results prove the feasibility and effectiveness of waveform synthesis and modulation based on phase-amplitude mapping. The final waveform resolution is improved by a factor of 4 compared to the sampling rate.

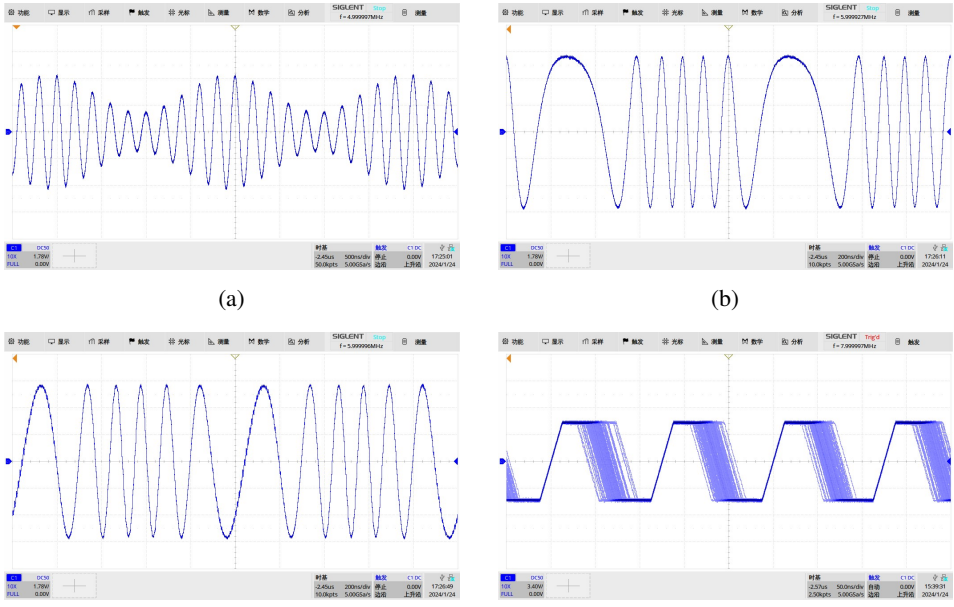
Metrol. Meas. Syst., Vol. 31 (2024), No. 3, pp. 547–564
DOI: 10.24425/mms.2024.150285



(a) (b)

(c) (d)

Fig. 20. (a) Pulse, (b) sine, (c) ramp, (d) square.



(a) (b)

(c) (d)

Fig. 21. (a) Amplitude modulation, (b) frequency modulation, (c) phase modulation, (d) PWM.

5. Conclusions

Traditional waveform synthesis techniques are limited by sampling rate and memory in improving timing resolution. This paper proposes a waveform synthesis method based on phase-amplitude mapping. The waveform is reconstructed by accurately calculating the waveform sampling points. When the waveform parameters change, there is no need to update the waveform lookup table. Real-time calculation can generate waveform data under new parameters. However, the essence of this method is to utilize the DAC with high vertical resolution, sacrificing the amplitude resolution for the time resolution, which will result in the upper limit of the resolution of the synthesized waveform depending on the DAC vertical resolution. On this basis, the accuracy and resolution of the waveform's internal timing parameters (rising edge, falling edge, pulse width, and other parameters) are simultaneously determined by the phase resolution and the calculation accuracy of the waveform expression.

In this paper, we utilize the "FPGA+DAC" hardware platform to compare with the traditional DDS under the same conditions to verify the feasibility and superiority of the method. Finally, the synthesized waveform achieves a timing resolution of 4 times relative to the DAC sampling rate, and modulation is realized. The method can realize a test stimulus signal source with high timing resolution, and produce stimulus signals with variable frequency, editable shape, and precise control.

References

[1] Bowler, R., Warring, U., Britton, J. W., Sawyer, B. C., & Amini, J. (2013). Arbitrary waveform generator for quantum information processing with trapped ions. *Review of Scientific Instruments*, *84*(3), 033108. https://doi.org/10.1063/1.4795552

[2] Lukin, K. A., Zemlyaniy, O. V., Tatyanko, D. N., Lukin, S., & Pascazio, V. (2017). Noise radar design based on FPGA technology: On-board digital waveform generation and real-time correlation processing. *2017 18th International Radar Symposium (IRS)*, 1–7. https://doi.org/10.23919/IRS.2017.8008223

[3] Qin, X., Zhang, W., Wang, L., Zhao, Y., Tong, Y., Rong, X., & Du, J. (2020). An FPGA-Based Hardware Platform for the Control of Spin-Based Quantum Systems. *IEEE Transactions on Instrumentation and Measurement*, *69*(4), 1127–1139. https://doi.org/10.1109/TIM.2019.2910921

[4] Sarnago, H., Burdio, J. M., Garcia-Sanchez, T., Mir, L. M., Alvarez-Gariburo, I., & Lucia, O. (2020). GaN-Based Versatile Waveform Generator for Biomedical Applications of Electroporation. *IEEE Access*, *8*, 97196–97203. https://doi.org/10.1109/ACCESS.2020.2996426

[5] Veyrac, Y., Rivet, F., Deval, Y., Dallet, D., Garrec, P., & Montigny, R. (2016). A 65-nm CMOS DAC Based on a Differentiating Arbitrary Waveform Generator Architecture for 5G Handset Transmitter. *IEEE Transactions on Circuits and Systems II: Express Briefs*, *63*(1), 104–108. https://doi.org/10.1109/TCSII.2015.2504947

[6] Yao, C., Zhang, X., Guo, F., Dong, S., Mi, Y., & Sun, C. (2012). FPGA-Controlled All-Solid-State Nanosecond Pulse Generator for Biological Applications. *IEEE Transactions on Plasma Science*, *40*(8), 2366–2372. https://doi.org/10.1109/TPS.2012.2188908

[7] Chen, P.-T., Zeng, F.-Y., Zhang, X.-H., Chung, R.-J., Yang, C.-J., & Huang, K. D. (2020). Composite Sinusoidal Waveform Generated by Direct Digital Synthesis for Healthy Charging of Lithium-Ion Batteries. *Energies*, *13*(4), 814. https://doi.org/10.3390/en13040814

[8] Marini, F., Bellato, M., Bergnoli, A., Brugnera, R., dal Corso, F., Corti, D., Dong, J., Garfagnini, A., Giaz, A., Gong, G., Hu, J., Isocrate, R., Jiang, X., Lippi, I., von Sturm, K., Aiello, S., Andronico,

G., Antonelli, V., Bandini, W., . . . Votano, L. (2021). FPGA Implementation of an NCO Based CDR for the JUNO Front-End Electronics. *IEEE Transactions on Nuclear Science*, *68*(8), 1952–1960. https://doi.org/10.1109/TNS.2021.3084446

[9] Xiao, Y., Chen, Y., Liu, K., Huang, L., & Yang, X. (2019). A Sampling Rate Selecting Algorithm for the Arbitrary Waveform Generator. *IEEE Access*, *7*, 83761–83770. https://doi.org/10.1109/ACCESS.2019.2922989

[10] Shao, Y. Z., Zhang, H., & Ge, Y. H. (2013). Design of Signal Generator Based on DDS Technology. *Advanced Materials Research*, *846–847*, 488–492. https://doi.org/10.4028/www.scientific.net/AMR.846-847.488

[11] Muanenda, Y., Faralli, S., Oton, C. J., Velha, P., & Di Pasquale, F. D. (2022). Adaptable Pulse Compression in ϕ-OTDR with Direct Digital Synthesis of Probe Waveforms and Rigorously Defined Nonlinear Chirping. *IEEE Photonics Journal*, *14*(2), 1–10. https://doi.org/10.1109/JPHOT.2022.3152816

[12] Samila, A., Hotra, O., & Majewski, J. (2021). Implementation of the Configuration Structure of an Integrated Computational Core of a Pulsed NQR Sensor Based on FPGA. *Sensors*, *21*(15), 6029. https://doi.org/10.3390/s21186029

[13] Zhao, W., Tian, S., Guo, G., You, J., Wu, Q., & Liu, K. (2023). An arbitrary waveform synthesis structure with high sampling rate and low spurious. *Metrology and Measurement Systems*. https://doi.org/10.24425/mms.2022.140027

[14] Narayan Sinha, S., Chatterjee, S., & Palani, R. K. (2022). A 2-GHz Two-Tone Direct Digital Frequency Synthesizer. *IEEE Transactions on Circuits and Systems II: Express Briefs*, *69*(12), 5109–5113. https://doi.org/10.1109/TCSII.2022.3202903

[15] Liu, H., Fu, Z., Kong, D., Wang, H., & Xiao, Y. (2023). Method of high timing resolution pulse synthesis based on virtual sampling. *Metrology and Measurement Systems*. https://doi.org/10.24425/mms.2022.140034

[16] Sharma, A., Sun, Y., & Simpson, O. (2021). Design and Implementation of a Re-Configurable Versatile Direct Digital Synthesis-Based Pulse Generator. *IEEE Transactions on Instrumentation and Measurement*, *70*, 1–14. https://doi.org/10.1109/TIM.2021.3094240

[17] Chen, L., Weng, Q., Chen, J., & Gu, J.-F. (2020). A Novel Amplitude Modulation Architecture via Time-Varying Programmable Metasurface for Wireless Communication Systems. *IEEE Access*, *8*, 75127–75134. https://doi.org/10.1109/ACCESS.2020.2988769

[18] Crovetti, P. S. (2021). Spectral characteristics of DDPM streams and their application to all-digital amplitude modulation. *Electronics Letters*, *57*(5), 212–215. https://doi.org/10.1049/ell2.12050

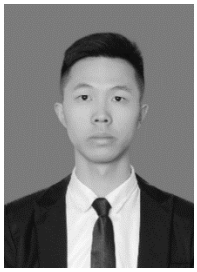
[19] Williams, W. D., Herd, M. T., & Cook, E. C. (2020). Pulsed triple frequency modulation for frequency stabilization and control of two lasers to an optical cavity. *Review of Scientific Instruments*, *91*(8), 085116. https://doi.org/10.1063/5.0010085

[20] Hati, A., & Nelson, C. W. (2022). A Simple Optimization Method for Generating High-Purity Amplitude and Phase Modulation. *IEEE Transactions on Instrumentation and Measurement*, *71*, 1–9. https://doi.org/10.1109/TIM.2022.3186367

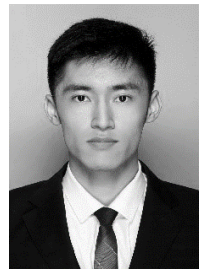
[21] Liu, Q., Xu, F., Peng, W., Xia, W., Wu, D., & Luo, J. (2021). A new displacement demodulation algorithm for the phase-modulated self-mixing interferometer based on FPGA. *Procedia Computer Science*, *183*, 379–388. https://doi.org/10.1016/j.procs.2021.02.074

[22] Koutroulis, E., Dollas, A., & Kalaitzakis, K. (2006). High-frequency pulse width modulation implementation using FPGA and CPLD ICs. *Journal of Systems Architecture*, *52*(6), 332–344. https://doi.org/10.1016/j.sysarc.2005.09.001

[23] Sarker, R., Datta, A., & Debnath, S. (2021). FPGA-Based High-Definition SPWM Generation with Harmonic Mitigation Property for Voltage Source Inverter Applications. *IEEE Transactions on Industrial Informatics*, *17*(2), 1352–1362. https://doi.org/10.1109/TII.2020.2983844



Xin Ai e is currently pursuing is M.Sc. degree in Instrumentation Science and Technology at Chengdu University of Electronic Science and Technology, Chengdu, China. His research interests include pulse waveform synthesis and arbitrary waveform generator and pulse waveform generating technology and the like.



Hanglin Liu received the B.S. and M.Sc. degrees in instrumentation engineering, in 2015 and 2018, respectively from the University of Electronic Science and Technology of China, (UESTC), Chengdu, China, where he is currently working toward the Ph.D. degree in instrument science and technology. His main research interest is automatic digital testing technology and systems.

Zaiming Fu received his both M.Sc. and PhD degrees both from the University of Electronic Science and Technology of China (UESTC), Chengdu, China, in 2004 and 2010 respectively. Now, he is a professor in school of automation engineering, UESTC. His research interests include data generators and pulse generators, measurement and instruments, signal processing and on the like.

Dexuan Kong is currently working toward the Ph.D. degree in instrument science and technology at the University of Electronic Science and Technology of China, Chengdu, China. His research interests include instrument science and technology, automatic testing and system integration technology, arbitrary and pulse waveform generating technology and the like.