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New ternary decoders using hybrid memristor-MOS logic

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***Abstract*—Integrating memristor technology with traditional CMOS has led to innovative designs for ternary logic, significantly enhancing the performance and efficiency of digital integrated circuits. This hybrid approach takes advantage of the unique properties of memristors, including low power consumption, compact size, and non-volatility, to develop ternary logic circuits that outperform conventional binary systems in terms of area and energy efficiency. This article presents two new low-power ternary decoders designed using a hybrid memristor-MOS logic approach. The decoders were simulated and analyzed using SPICE, and their performance was compared with existing circuits. The results indicate that the power-efficient decoder uses 44.44% fewer transistors and dissipates 97.78% less power than previously documented circuits.**

***Keywords*—Ternary logic; Memristor; Ternary Decoder; MVL; MOS**

I. Introduction

TERNARY logic, using three states, offers advantages over traditional binary logic and provides a higher information density of approximately 1.5 times the information, which means a more compact and efficient data representation [1]. Another crucial parameter for low-power design is energy efficiency. Ternary systems often require fewer state transitions, which reduces dynamic power consumption and gives operational energy savings [2]. In addition, ternary logic also supports error detection and correction, which is essential for reliable computing. It is also closer to quantum computing and neuromorphic systems, where more than one state is a natural phenomenon. The above two facts reassure the audience about the applicability of ternary logic in this rapidly evolving field of computing [3]. Moreover, fabricating the ternary design requires a highly complex fabrication process and a lack of standardized tools in the present binary-dominated systems [4].

Ternary logic is utilized for high computing speed, increased storage density, and low-power applications. It has a base 3, and each of its digits is called a trit. Each trit is equal to 0, 1, or 2, which represents 0 (false), $V_{dd/2}$ (intermediates), and V_{dd} (true), respectively. A ternary digit can encode and store much more information than a binary digit. In addition, the three-state processing capability of ternary logic makes it capable of faster computation and energy-efficient designs, making it a promising alternative in future low-power, high-speed digital systems [5]. Ternary logic simplifies complex state machines and memory-addressing schemes; its applications in high-performance computation make it a candidate of high relevance in developing sophisticated systems and suitable for designing combinational circuits, programmable logic arrays (PLAs), memory circuits, decoder processing elements for error correction scheme and wireless sensors [5], [6], [7].

Ref. [8] reported that ternary logic circuit design uses key elements like metal oxide field effect transistor (MOSFET), FinFET, and carbon nano-tube field effect transistor (CNFET). MOSFETs retain the advantages over CNFETs because of their maturity, ease of integration, and proven reliability. Key strengths include a well-established and optimized manufacturing process, seamless compatibility with existing CMOS technology, and advantageous threshold voltage behavior at reduced channel lengths for high-speed applications [9]. In some cases, MOSFETs also have lower power consumption, especially in larger geometries [10]. Paper [11] reported a ternary decoder designed using 12 transistors with a power dissipation of 0.44nW. Although CNFETs are better suited to nanoscale applications and provide reduced leakage power while increasing performance, MOSFETs' maturity and practicality are the core of current semiconductor technology [12]. This competition will keep these technologies going, at least for the time it takes to perfect hybrid approaches. While providing an edge over the MOSFETs, specifically in power efficiency and nanoscale performance, the CNFET has faced issues with threshold voltage variability and complex process fabrication [13]. Moreover, incorporating CNFETs in the existing semiconductor technology is challenging because of differences in processing techniques [14]. While promising for low-power and high-performance applications, such challenges may limit their wider adoption compared to well-established MOSFETs [15].

MOS transistors offer fast switching and substantial control over logic; the memristor introduces non-volatility memory and state-dependent resistance [16]. Configuring memristors with specific voltage thresholds allows the circuit to distinguish between these states [17]. The hybrid use of MOS and memristor technologies in the ternary logic circuits opens avenues for innovative circuit designs that can support emerging paradigms for computation, including neuromorphic and quantum computing. Integrating memristor and MOS technology opens up an interesting avenue for implementing ternary decoders. Combining these technologies, hybrid memristor-MOS

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circuits can obtain compact, efficient, and reliable ternary decoders [18].

A memristor in digital applications is a non-volatile memory element that offers data storage with low power consumption and high-density integration, which may also advance neuromorphic computing and reconfigurable logic circuits [16]. Memristors, which store multiple levels of resistance, allow for the representation of ternary values, whereas MOS transistors control signals. The memristor employed can be used for computation or storage purposes. With their ability to implement ternary logic, Memristor-CMOS circuits offer practical benefits beyond theoretical concepts. These circuits, including multiple states, allow for more efficient data representation than binary systems, which are particularly beneficial for active matrix microdisplays, where pixel density is prioritized over speed [19]. Ref. [18], [20] reported ternary decoders with improved data density by factors of 3.6 to 8.5.

This paper introduces hybrid memristor MOS-based ternary decoder circuits. The SPICE tool was utilized to conduct simulations, and the results were compared with those of the existing decoder architecture to demonstrate the effectiveness of the performance parameters. The theoretical background presents the basic building blocks discussed in Section II and Section III proposing the ternary decoder circuits using hybrid memristor MOS logic. Section IV provides results and discusses them. Finally, in Section V conclusions are drawn.

II. Background

A. Overview of Ternary logic

Ternary logic is an interesting three-valued system that allows variables to take on one of three values. In unbalanced ternary logic, these values are often represented as 0, 1, and 2, whereas balanced ternary logic uses -1, 0, and 1. This capability differs from traditional binary logic, which limits values to 0 and 1 and offers a more efficient way to represent data and process information [21]. In this work, unbalanced positive ternary logic (0, 1, 2) = (GND, $V_{dd/2}$, V_{dd}) is used. A binary logic can implement OR, AND, and NOT be used to create any combinational logic. Ternary logic efficiently creates an implementation of a set of basic logic gates and will, therefore, easily enable combinational logic circuits to implement functions. Equations (1)-(5) show the different ternary logic gate functions for the inputs Z_i and Z_j, where (i,j) = 0, 1, or 2.

$$\text{NOT:} \quad \overline{Z_i} = 2 - Z_i, \tag{1}$$

$$\text{AND:} \quad Z_i \cdot Z_j = \min\{Z_i, Z_j\}, \tag{2}$$

$$\text{OR:} \quad Z_i + Z_j = \max\{Z_i, Z_j\}, \tag{3}$$

$$\text{NAND:} \quad \overline{Z_i \cdot Z_j} = \overline{\min\{Z_i, Z_j\}}, \tag{4}$$

$$\text{NOR:} \quad \overline{Z_i + Z_j} = \overline{\max\{Z_i, Z_j\}}, \tag{5}$$

Ternary inverters (TI), Ternary-OR (TOR), and Ternary-AND (TAND) are the basic building blocks for designing other functional ternary logic or designs. A TI gate evolves complementary outputs and uses voltage thresholds, reducing circuit complexity and interconnections. Conventional Ternary Inverters (TI) can be Standard or Simple Ternary Inverter (STI) [11], [20], Negative Ternary Inverters (NTI) and Positive Ternary Inverter (PTI). These conventional designs look promising for making more efficient systems requiring high data representation with compact designs [22]. Resistors and transistors can be used to design TAND and TOR circuits. In [20], using hybrid-memristor MOS logic, TAND and TOR are implemented with the Memristor-Ratioed Logic (MRL) technique [23].

B. Ternary Decoder circuit

A ternary decoder is a key circuit in multi-valued logic meant to take in three different states and return unique output signals. In this respect, ternary decoders prove useful primarily in memory systems, arithmetic operations, and neuromorphic computing. A ternary decoder is a digital circuit, a combinational circuit that transforms ternary input signals into unique output combinations to process and store more efficient data in a ternary logic system. The response of the ternary decoder with the input variable Z has three outputs, Z_0, Z_1, and Z_2, respectively; the input and output relation of a ternary decoder is represented by equation (6).

$$Z_{i,i\in\{0,1,2\}} = \begin{cases} 2, & \text{if } z = i, \\ 0, & \text{if } z \neq i. \end{cases} \tag{6}$$

The value i can be 0, 1, or 2. The ternary decoder uses the logic shown in Table I. A ternary decoder can be designed using NTI, PTI, and TNOR, which requires impedance matching between the NTI output and the TNOR gate input [19].

TABLE I
TERNARY DECODER LOGIC

Z	Z_0	Z_1	Z_2
0	2	0	0
1	0	2	0
2	0	0	2

C. Memristor-based logic

The memristor is a two-terminal electrical component invented by Leon O. Chua [16]. It is the fourth fundamental circuit element, alongside the resistor, capacitor, and inductor. Numerous research studies have been conducted on memristor-based systems after developing a solid-state memristor in HP Laboratories. The memristor-ratio logic (MRL) technique is used to construct a hybrid memristor-MOS-based digital circuit [23]. This paper adopts the KNOWM memristor model [24], widely used in the literature for its robustness and suitability for ternary logic. The memristor model specifications used in the literature are given in Table. III. The memristor-based OR gate is shown in Fig.1. Input voltage levels represent the logic state. In this circuit, MRL is employed, whereas a voltage-divide circuit is performed to get the output response of this circuit. The memristor-based OR logic is given in Table II.

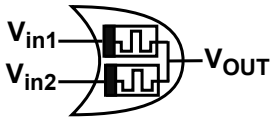

Fig. 1. Memristor-based OR gate

TABLE II
OR LOGIC

V_{in1}	V_{in2}	V_{OUT}
0	0	0
0	2	2
2	0	2
2	2	2

The inverter circuit is a fundamental requirement for any decoder circuit. A conventional CMOS inverter uses two MOS transistors, NMOS and PMOS . This article uses a hybrid memristor-MOS-based inverter circuit, which enables the MRL logic. A hybrid memristor-MOS-based inverter shown in Fig. 2 (a) is designed by replacing the PMOS transistor of a CMOS inverter with a memristor. Symbols of NTI and PTI are shown in Fig. 2 (b) and Fig. 2 (c), respectively. NTI and PTI logic is determined by maintaining the proper threshold voltage of the NMOS transistor $N1$ and utilizing the memristor [20]. For NTI, the threshold voltage of $N1$ must be taken below $V_{dd/2}$, whereas for PTI above $V_{dd/2}$. Figure 2 (d) shows the symbol of a Memristor-Ratioed logic inverter (MLI). For NTI and PTI, the input switching conditions are determined by examining the transitions of $0 \rightarrow 2$, $2 \rightarrow 0$, $1 \rightarrow 0$, and $1 \rightarrow 2$ respectively. For MLI inverter, the R_{ON} and R_{OFF} resistance of memristor is taken 10Ω and $11\text{k}\Omega$ whereas, for ternary inverter, its value is taken as per the specification given in Table III. The MLI inverter uses an NMOS-memristor combination working as pull-up and pull-down devices [23]. When the input voltage given at MLI is high, the transistor N_1 turns ON, and the output voltage is given as:

$$V_{out} = \frac{R_{ON}}{R_{ON} + R_{Tran}} \cdot V_{dd} \simeq 0 \tag{7}$$

When the input voltage is low, the N_1 is OFF, and the output voltage is given as:

$$V_{out} = \frac{R_{ON}}{R_{ON} + R_{Tran}} \cdot V_{dd} \simeq V_{dd} \tag{8}$$

The fastest transition for MLI inverter logic was found during a low resistance state when the input changes from low (0) to high (2). The average rise and fall time delays are then used to calculate the propagation delay for the CMOS and MLI types inverters. Table V presents the Propagation delays measured for various inverters under different input switching conditions.

D. Noise Margin (NM)

Noise margin (NM) is critical for ternary circuits to keep their signal levels intact because smaller NM values cause faulty output due to interference. There are four kinds of noise margins in the case of ternary logic gates: one for levels 0 and 2 and two for level 2; the noise margin of an STI is obtained with the help of the VTC curve [11]. The power consumption and delay also improve with the improvement of NM, wherein high NM improvement is noticed while optimizing other parameters of interest. The enhancement in NM is obtained if the transistors are appropriately sized. While the emphasis on NM is critical to improving the robustness of ternary logic circuits, the trade-offs have to be considered, such as complexity in design and area delay. A balance of such factors is crucial for pragmatic implementations in low-power devices.

TABLE III
MEMRISTOR MODEL SPECIFICATION

Model Parameter	Physical significance	Value
R_{ON}	ON Resistance	100Ω
R_{OFF}	OFF Resistance	$10\text{k}\Omega$
V_{ON}	Set threshold voltage	$0.35V$
V_{OFF}	Reset threshold voltage	$0.35V$
τ	State variable time constant	$500ps$
T	Temperature	298.5K
x_0	State variable initial condition	0

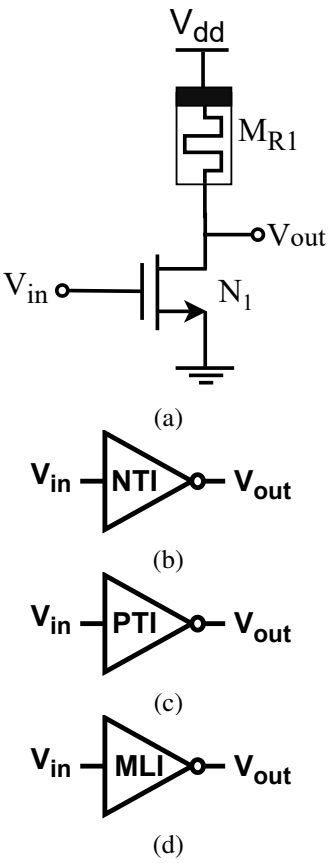

Fig. 2. Hybrid memristor-MOS-based: (a) Inverter (b) Negative Ternary Inverter (NTI) (c) Positive Ternary Inverter (PTI) (d) MRL-based Inverter (MLI)

TABLE IV
DIFFERENT INVERTERS LOGIC

$(Logic)$ V_{IN}	(STI) V_{OUT}	(NTI) V_{OUT}	(PTI) V_{OUT}	(MLI) V_{OUT}
0	2	2	2	2
1	1	0	2	0
2	0	0	0	0

TABLE V
DIFFERENT INVERTERS DELAY

Inverter Type	*Number of Transistor*	*Number of Memristor*	*Delay (ps)*
NTI	1	1	57
PTI	1	1	51
INV	2	-	36
MLI	1	1	48

III. PROPOSED TERNARY DECODER CIRCUITS

The paper focuses on two designed ternary decoder circuits, both implemented using memristor-MOS-based transistor logic. The authors propose two designs, Ternary Decoder I (TDI) and Ternary Decoder II (TDII), depicted in Fig. 3 (a) and Fig. 3 (c) respectively. The proposed TD1 in Fig. 3 (a) uses one NTI, one PTI, one inverter (M1-M2), and five MOS transistors (M3-M7).Transistors M1, M3, and M4 are of PMOS type, while M2, M5, M6 and M7 are of NMOS type. The working of the proposed TDI is described as follows: The result at Z_0 is simply the output of NTI, output at Z_1 is determined based on the working of transistors (M3-M7), whereas PTI and the inverter (M1-M2) determine the result of Z_2. Meanwhile, the result at Z_2 is the inverter output (M1-M2), which takes the input from PTI. Input at transistors M3-M7 determines the Z_1 output. The result at Z_2 is high only when the input Z is $V_{dd/2}$. In this situation, transistors M3-M5 are on, and transistor M7 is off. Figure 3 (b) shows the gate-level schematic of the proposed TDII, which uses one NTI, one PTI, one CMOS inverter (M10–M11), one memristor-ratioed logic inverter (MLI), and a two-input memristor-based OR gate.

As depicted in Fig. 3 (c), the output at Z1 is obtained from a NOR logic operation, which combines the two-input memristor-based OR gate and the MLI inverter.

IV. EXPERIMENT

The designs TDI and TDII were simulated in SPICE using 50nm BSIM technology with a supply voltage of 1V. The NMOS transistors utilized in our proposed designs, width (W), and length (L) are taken as 1μm and 50nm, respectively, whereas PMOS transistors utilize width (W) and length (L) as 2μm and 50nm, respectively. TDI and TDII take a ternary input and generate either GND or $V_{dd/2}$ outputs. The memristor model parameters used are provided in Table III. Figure 4 shows the simulation result of the proposed power-optimized Ternary Decoder. The proposed design's power,

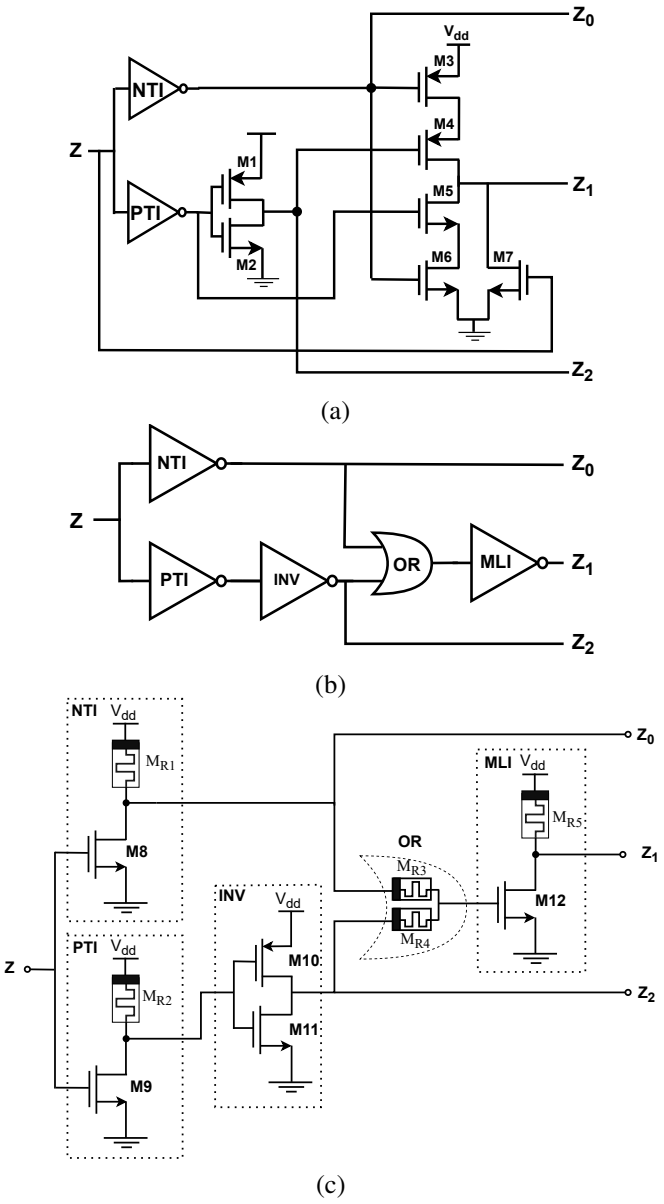

Fig. 3. Proposed hybrid memristor-MOS-based: (a) Ternary Decoder-I (TDI) (b) Gate level schematic of Ternary Decoder-II (TDII) (c) Schematic of proposed TDII

delay, and power delay product (PDP) are compared with previous reports as shown in Table VII. The proposed design TDI employs more transistors to achieve distinct logic levels. The second design, TDII, integrates ternary, binary, and MLI inverters to achieve the same functionality as the first. The second design substantially reduces the transistor count compared to the first design. This optimization results in a more compact and power-efficient circuit, making it highly suitable in applications where power constraints are critical. The delay associated with each ternary inverter design should, however, be incorporated into the overall performance of the decoder. The memristor-MOS-based ternary inverters exhibit varying delays depending on their configurations, memristor switching times, and transistor arrangements. The memristor-based design can be advantageous if minimizing power con-

sumption is the priority and the memristor is used effectively for state retention, as in the case of the proposed design TDII. If minimizing delay is the priority, then the MOS-only design would be better, like the proposed design TDI. Again, the delay depends on how ternary inverters are precisely located and utilized within the hybrid circuit. Though not the emphasis in this case, memristor-MOS-based designs intrinsically yield designs that have a lower power dissipation compared with CMOS-only designs. The second design's reduced transistor count minimizes the power dissipation.

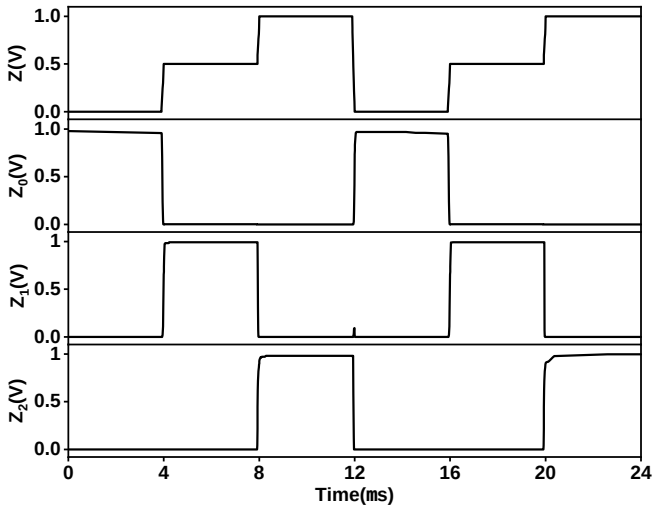

Fig. 4. Transient response of the proposed power optimized Ternary Decoder

TABLE VI
PROPOSED TERNARY DECODER-II LOGIC

Z	NTI	PTI	INV	OR	MLI
0	2	2	0	2	0
1	0	2	0	0	2
2	0	0	2	2	0

TABLE VII
PERFORMANCE PARAMETERS

Ternary Decoder	Device Type	Transistor count	Power (μW)	Delay (ps)	PDP (aJ)
[25]	MOSFET	12	13	140	1820
[26]	CNTFET	9	9.1	4.18	38.2
TDI	Memristor-MOS	9	11.5	112	1128
TDII	Memristor-MOS	5	0.202	134	27.06

The proposed ternary decoder TDII results use 44.44% less transistors and show 97.78% less power dissipation than previous literature [26]. The temperature variation of the proposed decoders is analyzed based on previous literature. Figure 5(a) and Fig. 5(b), compares temperature variations at temperature -10°C, 20°C, 30°C, 50°C and 70°C, for the PDP of the proposed TDI and TDII respectively.

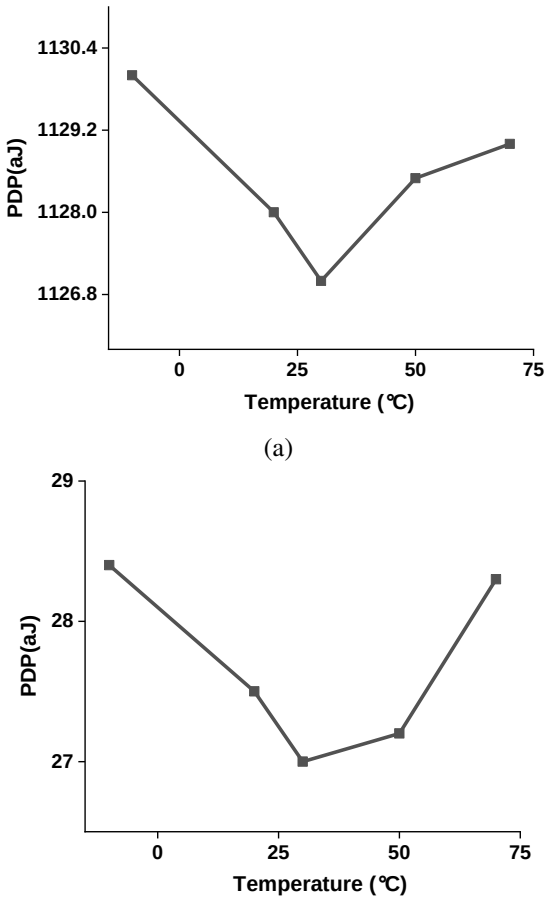

Fig. 5. Comparison of temperature variation for PDP of proposed: (a) TDI and (b) TDII

V. CONCLUSION

This paper introduces two new designs for a ternary decoder based on hybrid memristor-MOS technology, emphasizing transistor count, delay, and overall performance. The proposed designs utilize NTI gates, PTI gates, an OR gate, and MLI inverters. The proposed design TDII reduces the number of gates to achieve optimization. The first design, which uses ternary inverters, has a higher transistor count and more significant delay. The second design, which uses both ternary and MLI inverters, achieves similar functionality with fewer transistors and less power dissipation. Simulation results indicate that the power delay product (PDP) of the proposed design (TDII) is lower than that of the proposed design (TDI). This design can be useful for constructing low-power, high-speed, stable arithmetic logic units and other electronic devices. Using memristor-MOS-based inverters in both designs has resulted in circuits that consume relatively low power and are thus quite suitable for low-power applications. Future efforts could be targeted toward further delay optimization and integration at the system level to make these designs more applicable.

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