ELECTRONICS

SI-Studio – environment for SI circuits design automation

S. SZCZĘSNY*, M. NAUMOWICZ, and A.HANDKIEWICZ

Faculty of Computing, Poznań University of Technology, 3A Piotrowo St., 60-965 Poznań, Poland

Abstract. The current work is an answer to the problem of designing switched-current (SI) circuits, which is usually a complex issue in the field of microelectronics. The mentioned task is a source of many mistakes and takes a lot of time for designers, therefore authors of the article decided to propose a software solution. This article presents an environment for design automation of analogue circuits in the switched currents technique. It points out the utility advantages of the described tools, which make the work of a VLSI designer much easier, moreover offering a possibility to parameterise the design process considering power consumption, chip area usage and its working speed. It also presents results of an automatic generation of a filter pair circuit, as well as a DCT circuit – automatically generated with the proposed SI-Studio software tools.

Key words: SI circuits, layout, AMPLE, analogue circuits, design automation.

1. Introduction

Digital circuits are widely used in image processing and their design processes are strongly-automated. Although characterised by high data precision and easy to design, they do not offer so good parameters of power consumption, chip area occupancy and work speed as their analogue substitutes. Due to the miniaturisation trend in the modern microelectronics the necessity of adapting analogue circuits to the realisation of tasks like image pre-processing appears. Unfortunately the analogue circuit design process is much more difficult than designing digital circuits, takes a lot of time and produces a high risk source of mistakes. More reasons for solutions using analogue circuit automation methods appear in literature [1–3]. There is still no method nor a tool which allow to obtain a final ASIC circuit after providing parameters and specifications. The current work describes a proposition of a software tool for layout automation of the analogue circuit design using the switched-currents technique. The article briefly describes an idea of the created environment and its advantages for a designer. Examples of using the SI-Studio tool include: an analogue SI filter and the analogue Discrete Cosine Transform (DCT) processor.

2. Assumptions and concepts

A design process, which has not been yet automated, designs an analogue circuit layout. The proposed SI-Studio environment allows to obtain the final topography of an SI circuit chip in a case of a gyrator-capacitor prototype circuit (methods for obtaining automatically such a circuit were previously published in [4, 5]) or in a case of a switched-current prototype network without a given transistor level description. SI-Studio is in fact an environment of integrated applications realising subsequent design steps. It consists of: SIMaker and CurrentMirrorMaker programs described in [6] and the LayoutGenerator tool introduced in [7]. The whole concept of

such an integrated system is shown in Fig. 1. A design process is divided into few different steps realised by the mentioned tools. It starts with the generation of a VHDL-AMS standard language description of a switched-current circuit architecture generated using the SIMaker program. Such an architecture is built using the current mirror, the memory and the integrator cells [8].
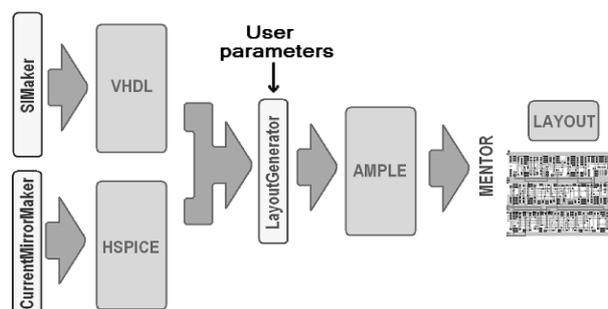
Fig. 1. Concept of an SI-Studio-integrated environment for the analogue switched-current circuits design automation

The CurrentMirrorMaker application offers a possibility of transforming such a structure to a transistor level description, calculating parameters of transistors which are located in current mirrors, which can be parameterised. Including libraries with cells, which cannot be parameterised (SI integrators, memories, comparators etc.), a full HSPICE program 'netlist' can be obtained and simulated offering the possibility of structure verification at a pre-layout step. The final step starts with the given technology specification parameters. Using this piece of information and the previously generated VHDL-AMS and HSPICE structures – an AMPLE script package may be obtained using the LayoutGenerator program. The AMPLE package can be executed under the ICStation environment (distributed by the Mentor Graphics company) which causes an automated drawing of the final circuit lay-

---

*e-mail: szymon.szczesny@put.poznan.pl

out [7]. User parameters allow to focus the process on power consumption, work speed or chip area occupancy.

Let us note that following all of the above steps, which result in generating an ASIC circuit project, has already taken an enormous amount of time and caused high risk of making mistakes by designers. The next section presents the SI-Studio environment from a user interface side, showing simultaneously that all above steps were done with single mouse-clicks, greatly simplifying the complex task of the analogue circuit design.

3. User interface

Figure 2 shows the main window of the SI-Studio environment after a gyrator-capacitor prototype ('FILTR.vhdla') loading. A description of the VHDL-AMS architecture is shown in the upper right corner. In this case a 5th-order filter pair with attenuation of 18dB is considered. Left upper window titled 'LIBRARY' shows the project tree – libraries created by a user while running subsequent steps. This tree becomes a navigation tree in the scope of the project. Not all branches of the tree are available for the user at every step. For example: a transistor description cannot be generated for a gyrator-capacitor prototype without generating the switched-currents architecture which is built using SI blocks and connections. The upper icon list contains buttons used for executing applications described in the previous section. Logs of the finished tasks and possible errors appear in the lower window.

To obtain a topography of a chip the user runs subsequent programs placed under icons in the upper menu. Those tools automatically load the circuit architecture from a previous step and generate the next architecture in just few seconds. Circuit architecture descriptions generated at each level are automatically included in the project. Figure 3 shows the effect of the first two steps: calculating node voltage equations of ('FILTR.equ') a gyrator-capacitor prototype circuit and building an SI prototype circuit ('FILTR.vhdl'), which in this case is an architecture of current mirrors and an integrator connections map. As it is seen in Fig. 3 those steps, now available for the user, led to the stage of choosing parameters for designing the chip. Now the user can define power consumption, speed of work and area occupancy. A factor which determines the design process considering the above parameters is the channel length of transistors used to build cells, which can be parameterised – current mirrors [7]. Chip area is directly dependent on transistors sizes. Power consumption, inversely proportional to transistors channel lengths, and settling time of the answer of a circuit are dependent on: linearly for short channels and square for long channels [9]. Users do not have to be aware of those relations and do not even have to know a channel length impact on chip parameters. The process of

defining parameters has been simplified to operating a single dial (Fig. 3) and estimations of power, speed and area properties have been illustrated with relevant slides. Exactness of illustrations is proved by designed prototype network simulations [6]. Channel lengths are calculated on the basis of a grid file, determined by the technology used in the process. An example of solutions generated for the mentioned filter pair is shown in Fig. 4a. *Lin* and *win* parameters describe the length and the width of transistors in an input stage of a 'CMXXp' current mirror with a balanced structure. *Louti* and *wouti* parameters describe the length and the width of transistors in output stages, which realise the chosen scaling factor S. Complementary transistors in a chosen input or output stage have a common length. All NMOS transistors in a chosen current mirror have a common width, and all PMOS transistors have similar widths, calculated using the grid file [6].

The last step before generating an AMPLE package is a parameter definition with respect to the used technology, i.e. transistors widths used in a grid file, the standard cell height, layer names, transistors models, etc. (Fig. 4b). Parameters from Figs. 4a and 4b are written during generating scripts, which allows to make the design process independent on the technology.

The last step of the design process is AMPLE package generation, which then is used in Mentor Graphics environment to draw the final layout of the circuit. Figure 5 shows a window with the summary of a current design step. The WIZARD position, which corresponds to the generated package, appears in the project tree. It consists of scripts with included algorithms of generating 5 integrators and 16 current mirrors cells, taking into consideration the technological specification ('TECH') and AMPLE libraries ('CM.lib', 'INT.lib'), which are used to generate cells of an SI circuit. The main program window shows a summary of the design process: input and output packages with the circuit architecture description, the number of generated cells, design parameters (e.g. the standard cell height, estimated parameters of power consumption, speed of work and chip area occupancy) and finally the location of files which took part in the design process.

An example of running the generated scripts for a TSMC 0.18 μm technology is shown in Fig. 6. The generated 5th-order filter pair, consisting of 5 integrators and 16 current mirrors, is built using 500 transistors. Using the Calibre tool distributed by the Mentor Graphics company – a post-layout simulation including a long 'netlist' of many parasitic elements – can be run. Results of a simulation in the frequency domain are shown in Fig. 7b with comparison to the ideal characteristics obtained from the filter pair transfer function. Figure 7a shows and compares the same results but for an early step – the transistor schematic stage, just before generating the final layout.

SI-Studio – environment for SI circuits design automation
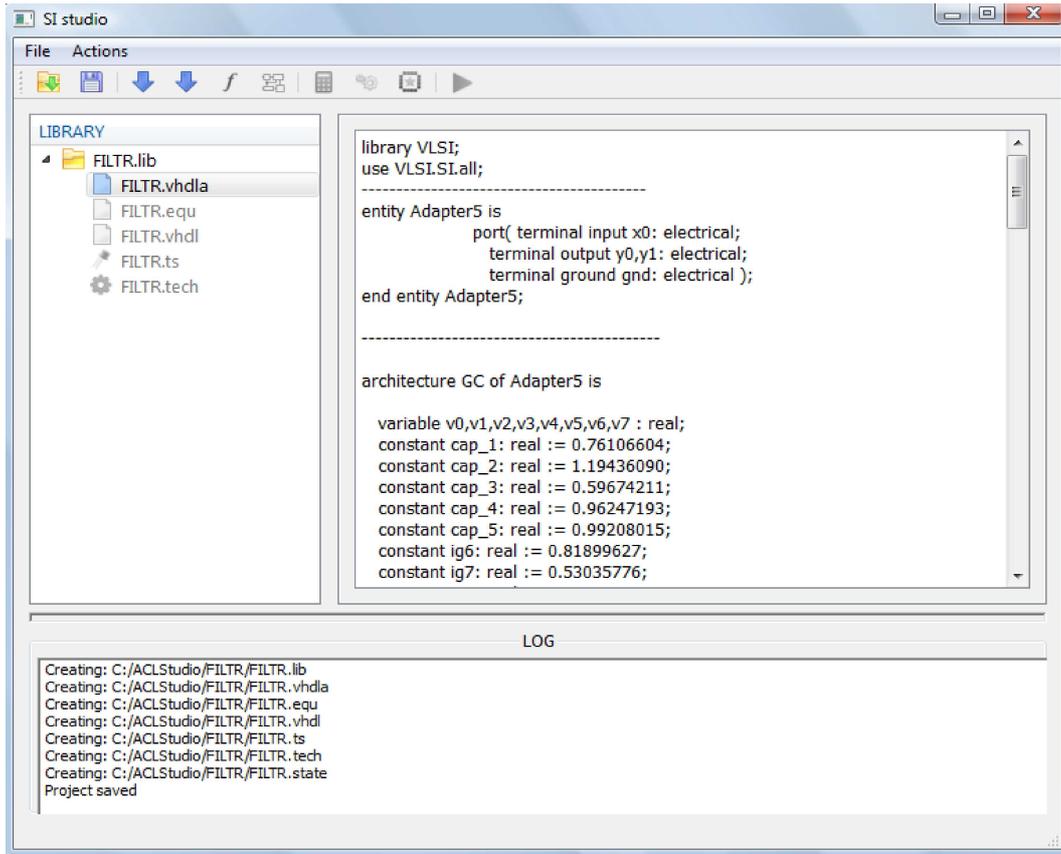
Fig. 2. Main window of the SI-Studio environment
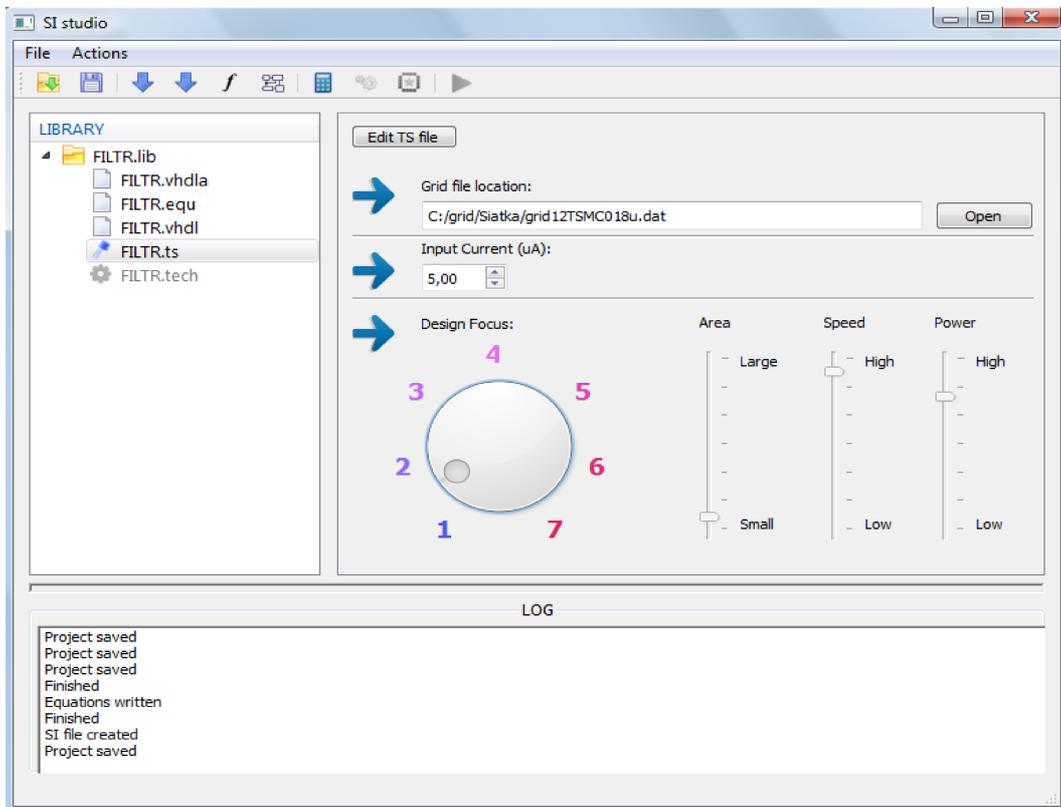
Fig. 3. Step of combined design parameters of the switched-current prototype circuit

S. Szczęsny, M. Naumowicz, and A. Handkiewicz

a)

b)
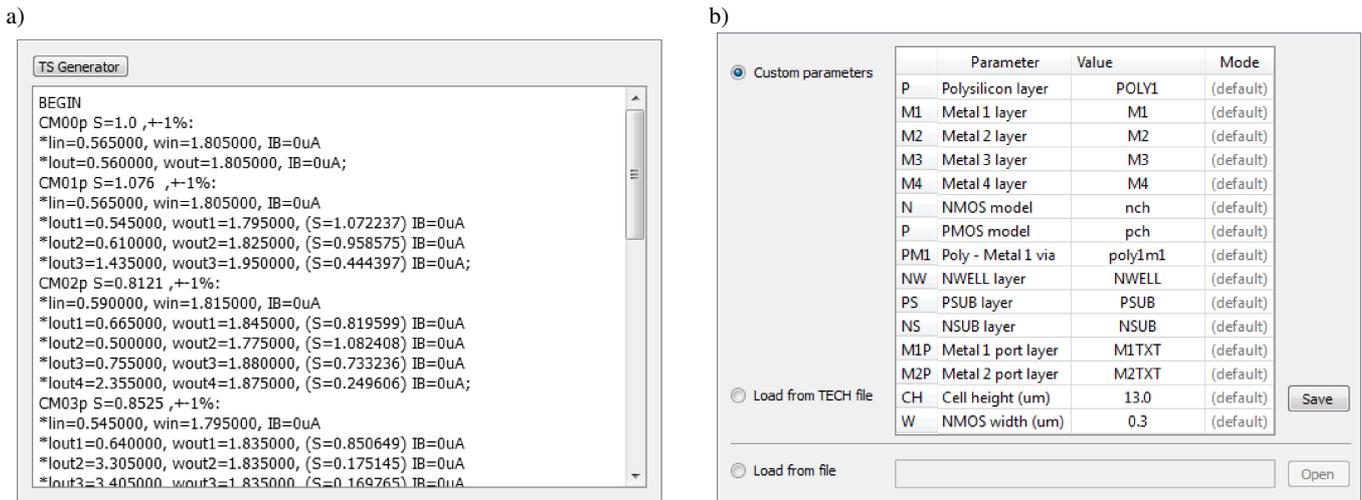
Fig. 4. a) Example of solutions generated for a filter pair, b) Table of technological parameters of the layout being designed
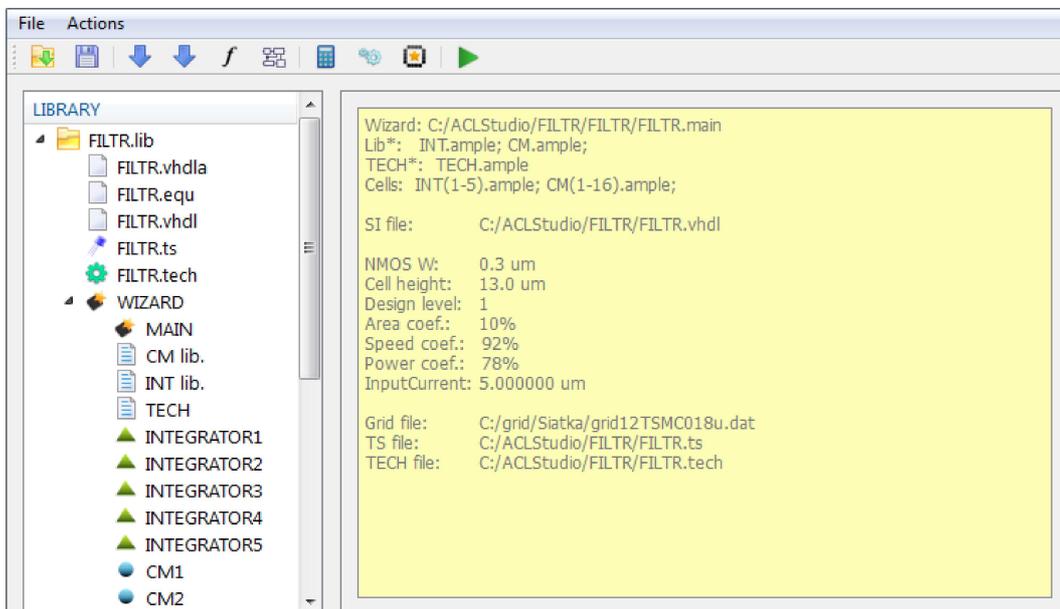
Fig. 5. Summary of a layout design process for a 5th-order filter pair
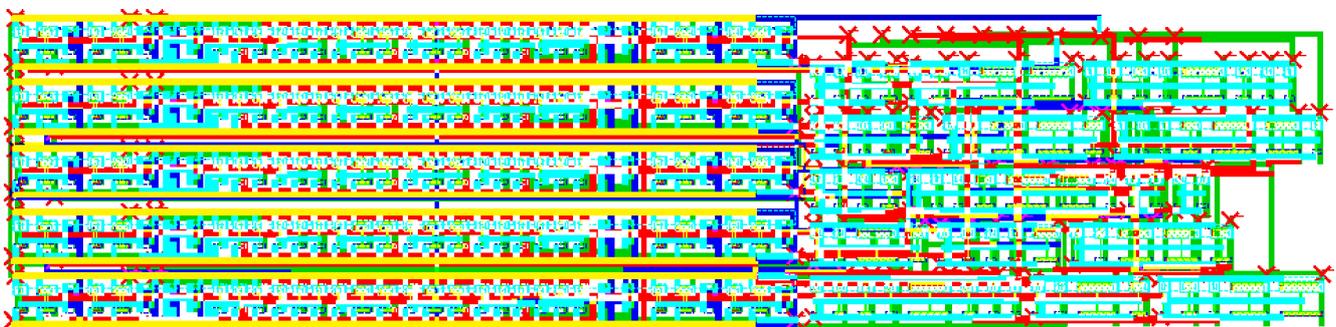
Fig. 6. Layout of a 5th-order filter pair (500 transistors)

a)

b)
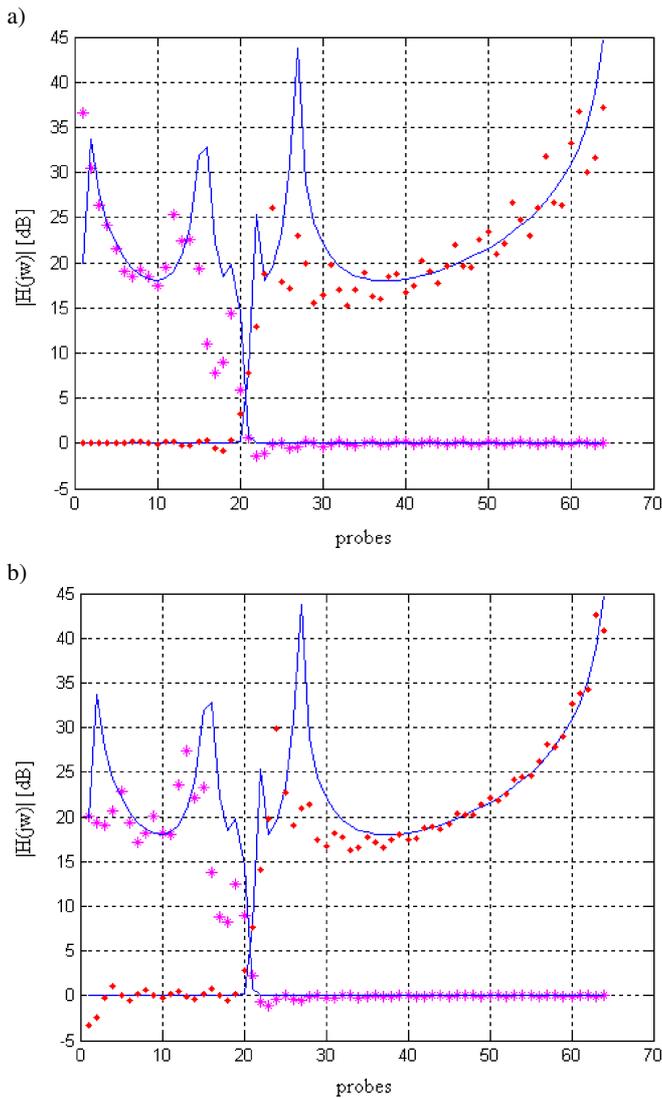
Fig. 7. Filter pair with attenuation of 18dB characteristics in the frequency domain: pre-layout (a) and post-layout (b) simulations. Ideal filter —, high pass output ∗, low pass output ♦

4. System versatility illustrated by a DCT circuit example

In the similar way it is possible to design any other circuit, which architecture consists of the current mirror, integrator, memory, comparator etc. cells – using the SI technique. For example, the presented SI-Studio tools have been adapted to the task of designing a two-dimensional DCT 4x4 analogue processor, which in fact multiplied of an input image and a constant coefficients matrices [10]. Architecture of such a processor is easy to implement in a switched-current technique [11] because mathematical operations are in fact multiplication operations realised using current mirror cells and the addition operations are implemented in nodes according to the 'Current Kirchhoff's Law'. Because of the need of repeating same operations twice, when a two-dimensional transform is considered, a block of memories is necessary to store intermediate results. The input data is an SI architecture in the VHDL-AMS language, containing a connection scheme between current mirrors and memory cells. It is worth noting that for a transform of a chosen size – such a scheme is constant – independently on the used technology parameters defined by a user. Therefore, it can be loaded from a file predefined in the environment library. An example of a generated DCT 4×4 circuit in the TSMC 0.18 μm technology, with parameters for the shortest channels lengths is shown in Fig. 8.

Similarly to the method mentioned in Sec. 3, a DCT circuit from Fig. 8 has been tested using the Calibre tool and the parasitic elements extraction. The TSMC technology and the SI technique determine the maximum pixel value equal to 10 μA for an image which can be driven to the input of the DCT circuit. Equation (1) presents an example of a pixel frame which was taken to the test. Values included in the matrix are expressed in μA.

$$X_{4\times4,input} = \begin{bmatrix} 2.0 & 2.0 & 2.0 & 2.0 \\ 1.5 & 1.5 & 1.5 & 1.5 \\ 1.0 & 1.0 & 1.0 & 1.0 \\ 0.5 & 0.5 & 0.5 & 0.5 \end{bmatrix}. \qquad (1)$$
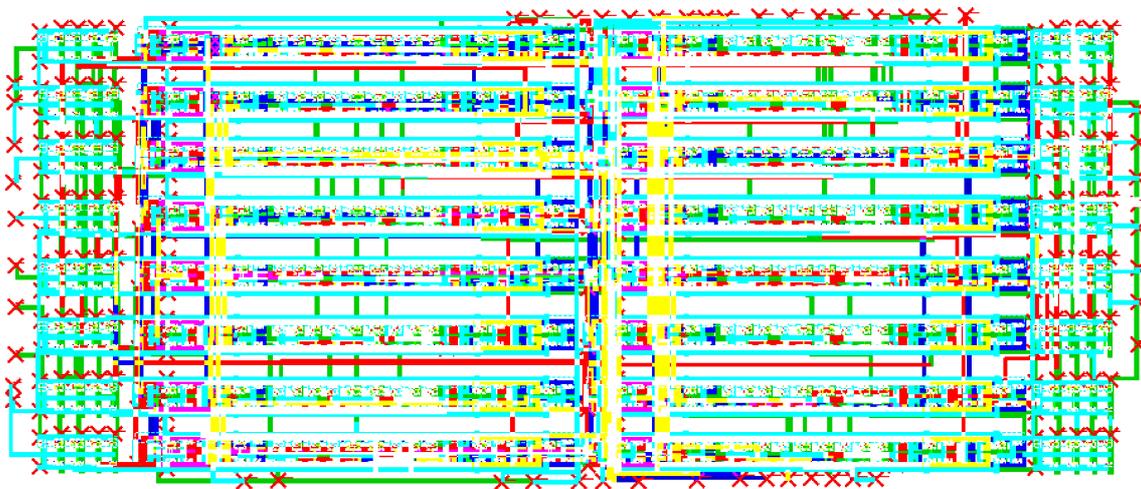
Fig. 8. Automatically generated two-dimensional DCT 4x4 circuit layout (900 transistors)

S. Szczęsny, M. Naumowicz, and A. Handkiewicz
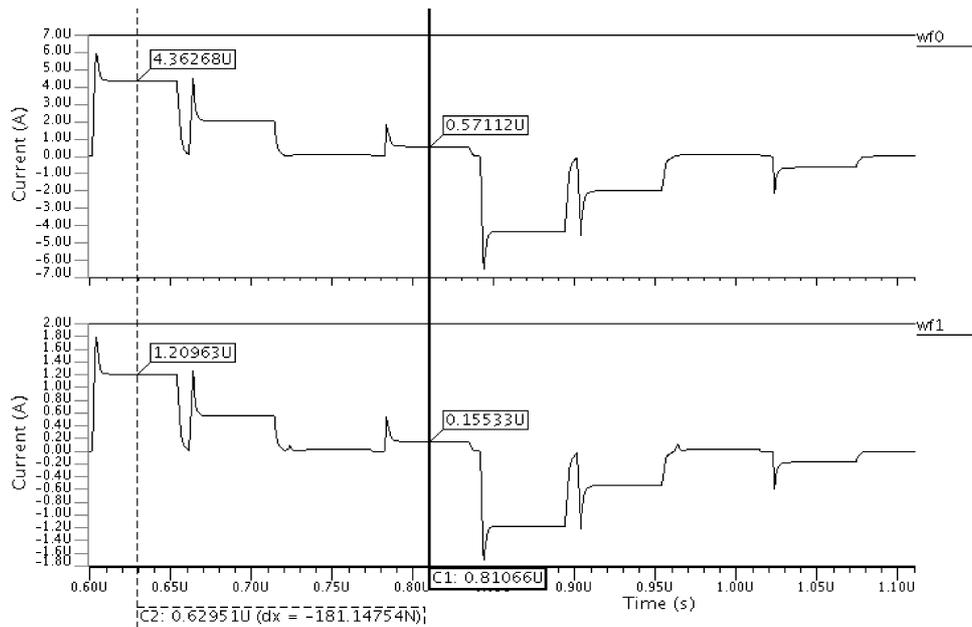
Fig. 9. DCT 4x4 post-layout simulation results

Figure 9 presents output signals from the DCT circuits obtained in simulations. Each waveform illustrates a single output frame column. Results are collected in Eq. (2).

$$X_{4\times4,output} = \begin{bmatrix} 4.3618 & 0.0 & 0.0 & 1.2094 \\ 2.0309 & 0.0 & 0.0 & 0.55 \\ 0.074 & 0.0 & 0.0 & 0.0223 \\ 0.5713 & 0.0 & 0.0 & 0.1554 \end{bmatrix}. \quad (2)$$

Using the method elaborated in [12] a Peak-Signal-to-Noise-Ratio (PSNR) coefficient and an accuracy factor can be obtained with an inverse transform calculation. A PSNR coefficient is equal to 35.45dB with the Mean Squared Error (MSE) equal to 0.02854 μA^2. An accuracy factor has the value of 43.3 dB.

5. Summary

The article presents the SI-Studio environment which is an answer to the problem of the SI analogue circuit layout generation. Difficult design steps, which have already taken a lot of time and caused a lot of mistakes, have been automated to the level of executing suitable programs and algorithms which realise those complex tasks. The current work contains brief descriptions of possibilities offered by the proposed tools. It includes examples of a layout generation for filters and analogue data processor circuits. Technology independence and versatility of the proposed method and tool are discussed and proved by post layout simulations. The elaborated method allows the user to optimize the designed circuit with respect to speed, power consumption or chip area.

REFERENCES

[1] E. Yilmaz and G. Dundar, "Analog layout generator for CMOS circuits", *IEEE Trans. Computer-aided Design of Integrated Circuits and Systems Archive* 28 (1), 32–45 (2009).

[2] H. Graeb, F. Balasa, R. Castro-Lopez, Y.-W. Chang, F.V. Fernandez, P.-H. Lin, and M. Strasser, "Analog – layout synthesis - recent advances in topological approaches", *Design, Automation & Test in Europe Conf. & Exhibition* 1, 274–279 (2009).

[3] R. Castro-Lopez, O. Guerra, E. Roca, and F.V. Fernandez, "An integrated layout-synthesis approach for analog ICs", *IEEE Trans. Computer-aided Design of Integrated Circuits and Systems* 27 (7), 1179–1189 (2008).

[4] A. Handkiewicz, P. Katarzyński, Sz. Szczęsny, J. Wencel, and P. Śniatała, "Analog filter pair design on the basis of a gyrator-capacitor prototype circuit", *Int. J. Circuit Theory and Applications* 40 (6), 539–550 (2012).

[5] A. Handkiewicz, P. Katarzyński, Sz. Szczęsny, "SI filter pair design with the use of a gyrator-capacitor prototype circuit", *IEEJ Int. Analog VLSI Workshop* 1, CD-ROM (2010).

[6] R. Rudnicki, "Choosen tools for automatic design of switched-current circuits", *PhD Dissertation*, Poznań University of Technology, Poznań, 2006, (in Polish).

[7] Handkiewicz, Sz. Szczęsny, M. Naumowicz, M. Melosik, and P. Katarzyński, "Generation of SI filters layout using the row strategy", *Electrical Review* 20, 80–83 (2011), (in Polish).

[8] R. Rudnicki, M. Kropidłowski, and A. Handkiewicz, "Low power switched-current circuits with low sensitivity to the rise/fall time of the clock", *Int. J. Circuit Theory and Applications* 38 (5), 471–486 (2010).

[9] R. Jacob Baker, *CMOS, Circuit Design, Layout and Simulation*, Wiley-Intercience, IEEE Press, London, 2007.

[10] A. Handkiewicz, *Mixed-Signal Systems: a Guide to CMOS Circuit Design*, John Wiley and Sons, London, 2002.

[11] A. Handkiewicz, P. Śniatała, G. Pałaszyński, Sz. Szczęsny, P. Katarzyński, M. Melosik, and M. Naumowicz, "Automated DCT layout generation using AMPLE language", *UTP Scientific Notebooks* 13, CD-ROM (2010), (in Polish).

[12] M. Pänkäälä, K. Virtanen, and A. Paasio, "An analog 2-D DCT processor", *IEEE Trans. Circuits and Systems for Video Technology* 16 (10), CD-ROM (2006).