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Current control with asymmetrical regular sampled pulse width modulator applied in parallel active filter

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Abstract. This paper presents an analysis of the properties of pulse width modulator with a single (symmetrical regular sampled PWM) and double (asymmetrical regular sampled PWM) control sampling of the input signal (low-frequency control input wave) in presence of a triangular auxiliary signal. In this paper, a comparison of the characteristics of these modulators used in the control system with a linear proportional controller is presented. The article provides the relations derived for the maximum amplification of regulators for which the control system operates stably. Analysis results have been confirmed by simulation and experimental studies of a commercial active filter installed in an industrial plant.

Key words: Active Power Filter, asymmetrical regular sampled PWM, current control.

1. Introduction

The use of P-type current regulators in the Active Power Filter (*APF*) not requiring intensive calculations, is particularly attractive in systems containing non-stationary loads. Other solutions, such as predictive current regulators [1], require much more time for calculation, which may be an obstacle to achieving good dynamic properties. The repetitive control [2–4] is useful if the reference signal is of repetitive nature.

In *APF* systems for fast Current Control, different forms of hysteresis controllers are applied. The most popular solution is a modulator with constant hysteresis value. This solution is characterized by a variable frequency of the current ripple in the inductance at the inverter output of *APF*. Solutions with variable hysteresis width [5] allow for achieving a constant frequency, however, they are still not synchronous systems. This makes it difficult to optimize parameters of the *LCL* ripple filter.

The use of proportional controllers allows for obtaining possibly low-order characteristic equations describing the current control system, which is particularly useful from the viewpoint of preserving the stable operation of the power system with *APF* reactive power compensating capacitive load.

In addition to the constant operating frequency of the transistors, a PWM modulator [6] should ensure good dynamic and static parameters of the closed loop *APF* output current control system. Paper [7] discusses the control system with a proportional controller with a sampling frequency, which is double and quadruple of the switching frequency. Since the *APF* requires 6 modulators, the proposed modulator is too complex to apply.

The article includes a simulation study of the control system with symmetrical regular sampled (SRS) pulse width modulator (PWM) with single sampling frequency and with asymmetrical regular sampled (ARS) PWM with double sampling frequency.

Simulation studies show an increase of the critical proportional controller gain with symmetrical regular sampled PWM with a doubled number of samples in the period of the triangular auxiliary signal for which the control system is stable. Also, the analysis included in this article demonstrates the possibility of increasing the value of the gain of the proportional controller in a closed system with asymmetrical regular sampled PWM.

Publications [8–14] devoted to applications in power electronics systems with the asymmetrical regular sampled PWM are not related to control systems with a proportional controller. From the point of view of the topics covered in this article, the most interesting paper is publication [15]. This paper addresses the digital control system with asymmetrical regular sampled PWM with different types of controllers, but the issues critical to the gain of the proportional controller addressed in the present article are not discussed.

One of the objectives of the work presented is to compare the dynamic and static properties of the control system with a proportional controller and symmetrical regular sampled or asymmetrical regular sampled PWM.

Carried out in this article is an analysis taking into account the time between the instant of measurement of the controlled value and the actual determination of the magnitude of the sampled reference (PWM computation delay [15]).

Control system with proportional controller has non-zero value of disturbance error. From the point of view of minimizing the disturbance errors and the reducing the time of decay of transient component of this error advantages of asymmetrical regular sampled PWM compared to the symmetrical regular sampled PWM manifest themselves only under the condition of an appropriately small value of the PWM computation delay.

The article also describes a mechanism allowing for elimination of the impact of this error on the output current of the *APF*.

This is a feature of *APF* with supervisory system of DC link voltage which allows the use of output current proportional controller.

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2. Description of the input circuit of active power filter

Fig. 1 shows a schematic diagram of the analyzed medium-voltage power supply system [16]. Controlled twelve-pulse converter is powered via a transformer *Tr2* with a vector group of Dd0y5 connections. *APF* containing two voltage inverters and medium voltage transformer *Tr1* with a vector group of Dy5 compensates harmonic current drawn by the non-linear load in the form of *Th12* converter. The chokes at the output of the inverter with the *C* capacitors and the leakage inductance of the transformer *Tr1* form *LCL* filter type [17, 18] in each phase. The *APF* has two two-level inverters (*T1_1–T6_2*) [19, 20] with FF600R12IS4F hybrid modules.

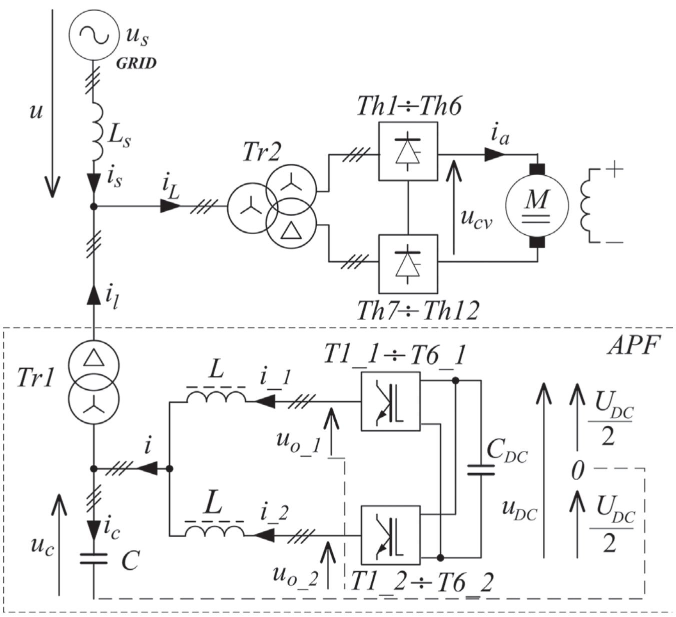

Fig. 1. The diagram of the analyzed circuit with active filter

The vectorial variables: $\boldsymbol{u}_s$, $\boldsymbol{u}$, $\boldsymbol{i}_s$, $\boldsymbol{i}_L$, $\boldsymbol{i}_l$, $\boldsymbol{i}_c$, $\boldsymbol{u}_c$, $\boldsymbol{i}_{\_1}$, $\boldsymbol{i}_{\_2}$, $\boldsymbol{i}$, $\boldsymbol{u}_{\_o1}$, $\boldsymbol{u}_{\_o2}$ are defined as follows:

- $\boldsymbol{u}_s = [u_{s1}, u_{s2}, u_{s3}]^T$ – vector of the mains source voltages
- $\boldsymbol{u} = [u_1, u_2, u_3]^T$ – vector of the phase voltages
- $\boldsymbol{i}_s = [i_{s1}, i_{s2}, i_{s3}]^T$ – vector of the line currents
- $\boldsymbol{i}_L = [i_{L1}, i_{L2}, i_{L3}]^T$ – vector of the *ac* load currents
- $\boldsymbol{i}_l = [i_{l1}, i_{l2}, i_{l3}]^T$ – vector of the *APF* output current
- $\boldsymbol{i}_c = [i_{c1}, i_{c2}, i_{c3}]^T$ – vector of the *C* capacitor currents
- $\boldsymbol{u}_c = [u_{c1}, u_{c2}, u_{c3}]^T$ – vector of the *C* capacitors voltages
- $\boldsymbol{i}_{\_1} = [i_{1\_1}, i_{2\_1}, i_{3\_1}]^T$ – vector of the *INV1* output currents
- $\boldsymbol{i}_{\_2} = [i_{1\_2}, i_{2\_2}, i_{3\_2}]^T$ – vector of the *INV2* output currents
- $\boldsymbol{i} = [i_1, i_2, i_3]^T$ – vector of the sum inverters currents
- $\boldsymbol{u}_{o\_1} = [u_{o1\_1}, u_{o2\_1}, u_{o3\_1}]^T$ – vector of the *INV1* output voltages
- $\boldsymbol{u}_{o\_2} = [u_{o1\_2}, u_{o2\_2}, u_{o3\_2}]^T$ – vector of the *INV2* output voltages.

3. Description of control system

The control system of one phase *APF* with a voltage regulator in the *DC* circuit shown in Fig. 2 implements the algorithm described in the literature [13, 21, 22]. Supervisory u_{DC} voltage regulator stabilizes the set value, proportional to u^*_{DC}. Signals u_1^*, u_2^*, u_3^* are in phase with the phase voltages u_{c1}, u_{c2}, u_{c3}, which cause the controller output signal u_n to determine the amplitude and phase (0 or π rad) of the active component of the inverter output currents. Such a control system provides discharging or charging of C_{DC} capacitor in transient states that are related to the change of active power drawn by the load. The control system of the filter uses the measurement signals of the load currents to determine the waveforms (i_1^*, i_2^*, i_3^*) that provide the set-point values of the inverter output currents. Set-point signal of current i_1 contains three components: the $i^*_{1,p(DC)}$ is a component of the set-point signal of current in phase with the voltage u_{c1}, controlling the voltage u_{DC}. The $i^*_{1,h}$ component contains the sum of selected harmonics of load currents, the current $i^*_{1,f}$ comprises the fundamental frequency component. Since the *APF* inverters are connected to the grid through *Tr1* transformer with Dy5 connection group, set-point signals (i_1^*, i_2^*, i_3^*) should depend on the difference of currents $i_{L1} - i_{L2}$, $i_{L2} - i_{L3}$, $i_{L3} - i_{L1}$ respectively, which indirectly results from the formulas that relate the currents on both sides of the transformer:

$$i_1 = -\tilde{o}_z \left(i_{l1} - i_{l2}\right)/3 \tag{1}$$

$$i_2 = -\tilde{o}_z \left(i_{l2} - i_{l3}\right)/3 \tag{2}$$

$$i_3 = -\tilde{o}_z \left(i_{l3} - i_{l1}\right)/3\ , \tag{3}$$

wherein υ_z means transformer turns ratio.

Above dependencies have been determined without taking into account the magnetizing current of the transformer and *C* capacitors currents. Values of k_{iL} and k_i coefficients are the constants of current transducers.

The purpose of band-pass filters and phase shifters, used in the load current measurement circuit, is to compensate for phase shifts of individual harmonic introduced both by the load current measuring transducers and *Tr1* transformer [21], [23–25].

The principle of compensation of individual $\boldsymbol{i}_{L,n}$ harmonics in load current involves forcing such *APF* output current, so the vector of its instantaneous values $\boldsymbol{i}_{l,n}$ satisfies the relationship:

$$\boldsymbol{i}_{l,n} = \boldsymbol{i}_{L,n}\ , \tag{4}$$

where n is the harmonic order ($n > 1$). This equality is satisfied also for the individual components of the vectors and thus also for their amplitudes, which will be marked as $I_{Lm,n}$ and $I_{lm,n}$ omitting indices *1, 2, 3*:

$$I_{Lm,n} = I_{lm,n}\ . \tag{5}$$

Since the load is three-phase balanced without neutral, the amplitude difference of the currents $i_{L1,n} - i_{L2,n}$ is √ 3 times the amplitude of the harmonic in any phase. For the summing nodes

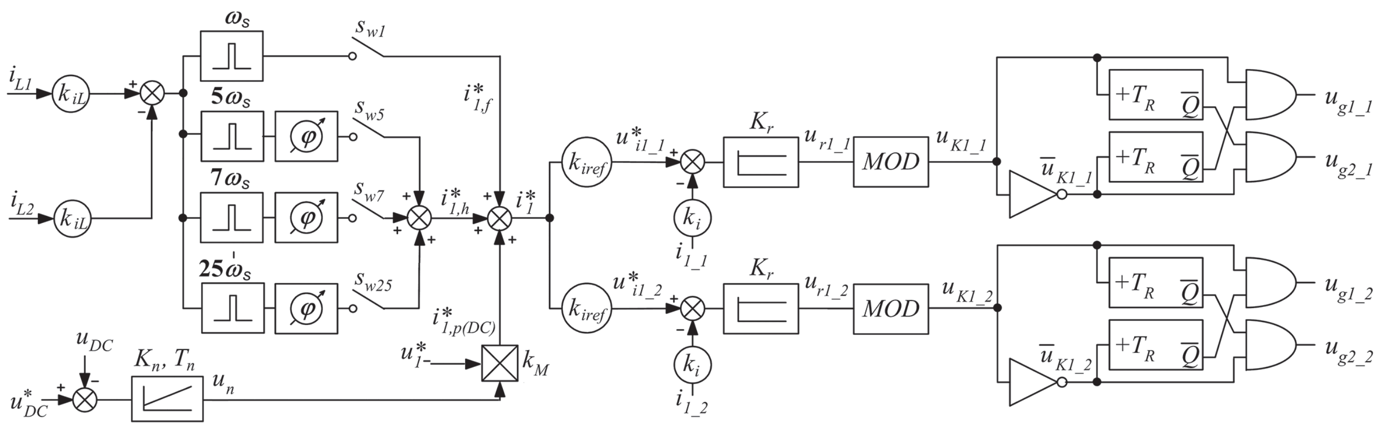

Fig. 2. Equivalent diagram for active filter control system for one phase *APF*

at the inputs of proportional controllers we can write equality, whose fulfillment ensures compensation of the n order harmonic of the load current:

$$\sqrt{3} I_{Lm,n} k_{iL} k_{uf} k_{iref} = 0.5 k_i I_{m,n}, \tag{6}$$

wherein k_{uf} denotes the gain of the band-pass filter, $I_{m,n}$ is the amplitude of the n order harmonic of i current and k_{iref} is the scale factor. The selection of the k_{iref} coefficient allows for such conditioning of measurement signal level of the load current that leads to the right compensation of selected harmonics.

From equations (1) and (3) the following relationship prevails:

$$I_{lm,n} = \frac{\sqrt{3} I_{m,n}}{\tilde{o}_z}. \tag{7}$$

After substituting (5) and (7) in (6), we obtain the relationship based on which one can determine the value of k_{iref} assuring compensation of individual harmonics:

$$k_{iref} = \frac{k_i \tilde{o}_z}{6 k_{iL} k_{uf}}. \tag{8}$$

To implement the chosen filter control we have used a popular TMS320F28335 DSP applied in power electronics [26].

4. Output current control system of voltage inverter with inductive load

Comparative analysis of the three types of modulators was performed based on the systems shown in Figs. 3 and 4. Modulators shown in Figs. 4b and 4c contain two systems of *S & H*. Pulses *trig1* (error sampling) are ahead of pulses *trig2* (PWM updating) by τ_w time. The minimum time τ_w is associated with the processing time of the *A/D* and the time required for the error calculation and its multiplication by the K_r constant.

To examine the properties of the modulators shown in Fig. 4 from the point of view of maximum gain $K_{r,cr}$ of the proportional controller which ensures stable operation of the system,

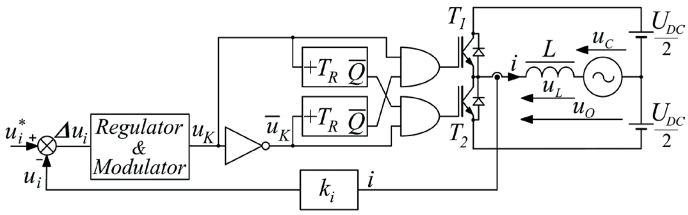

Fig. 3. Diagram of the output current control system of voltage inverter with inductive load

simulation tests were performed. Research was carried out for L = 80 μH, the frequency of the triangular carrier f_c = 15 kHz ($f_c = 1/T_c$), k_i = 1, U_{DC} = 720 V, and for the maximum value of the triangular carrier U_T = 5.5 V.

The variables expressed in the p.u. system shown in Figs. 5, 6, 8–11 are defined by the following formulas: $\bar{u}_c = u_c/U_{DC}$, $\bar{u}_L = u_L/U_{DC}$, $\bar{u}_T = u_T/U_T$, $\bar{u}_r = u_r/U_T$, $\bar{\imath} = i/I_b$, $\bar{u}_i^* = u_i^*/I_b$. Base current I_b defined by relation

$$I_b = U_{DC}/(4Lf_c) \tag{9}$$

is equal to the maximum value of the inverter *(T1,T2)* output current shown in Fig. 3 for $u_i^* = 0$, $u_c = 0$.

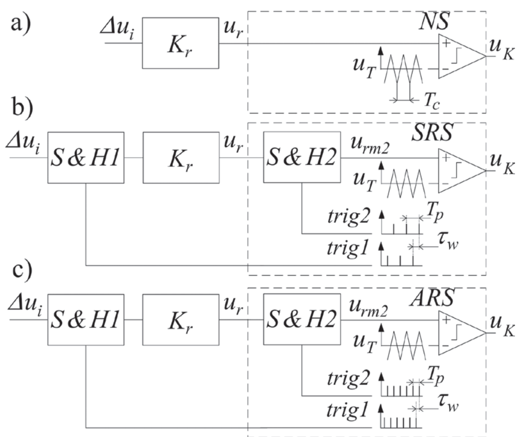

Fig. 4. Diagrams of tested systems of PWM modulators: a) double-edge naturally sampled PWM, b) symmetrical regular sampled PWM, c) asymmetrical regular sampled PWM

The analysis presented in this article has been based on the assumption of a very large value of L/R (R is the parasitic resistance of the L inductor) characteristic for high power devices.

5. Current control system with double-edge naturally sampled PWM

For the control system shown in Fig. 3 with pulse width modulation, involving the direct comparison of u_T auxiliary signal with the output of the current controller u_r (double-edge naturally sampled PWM [27], Fig.4a), the critical gain $K_{r,cr}$ can be determined by comparing the slew rate of the two signals:

$$\left|du_r / dt\right| \le \left|du_T / dt\right| . \tag{10}$$

If this condition is not satisfied, a repeated change in the output of the comparator in the period of T_c leads to unstable operation of the control system. Fig. 5 shows the border state for which the control system is stable.
The output signal of the controller is:

$$u_r = (u_i^* - k_i i)K_r . \tag{11}$$

If for analysis we assume constant value of the set-point signal u_i^*, then we obtain

$$du_r / dt = -k_i K_r \left(di / dt\right). \tag{12}$$

The du_T/dt derivative depends on the maximum value and the period of the auxiliary triangle wave:

$$\frac{du_T}{dt} = \frac{4U_T}{T_c}. \tag{13}$$

From (10–13) we obtain

$$k_i K_r \frac{di}{dt} \le \frac{4U_T}{T_c}. \tag{14}$$

Boundary conditions for which the current can be formed, occur for two cases: $u_c = -U_{DC}/2$ or $u_c = U_{DC}/2$. Maximum slew rate of the current i occurs when U_{DC} voltage is present across the inductance of the choke L. For this state the following equality is valid:

$$K_{r,cr} = \frac{4U_T}{U_{DC}} \frac{Lf_c}{k_i}. \tag{15}$$

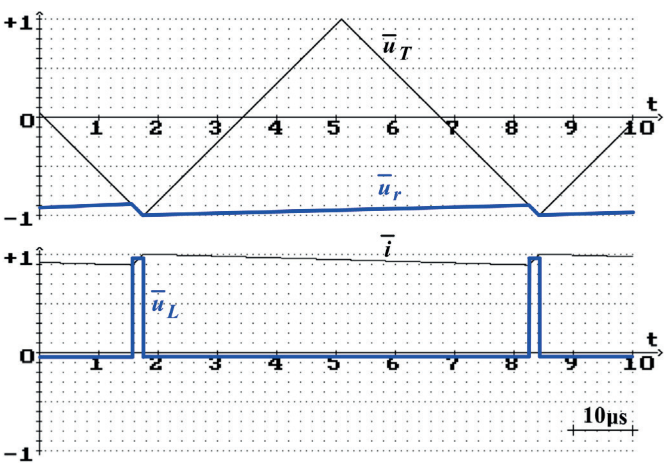

Fig. 5. Waveforms of voltage $\bar{u}_r$, $\bar{u}_T$, $\bar{u}_L$ and of current $\bar{i}$ for the modulator in Fig. 4a for $u_i^* = 0$, for $\bar{u}_c = -0.47$ and for $K_r = 0.0365$.

6. Current control system with symmetric and asymmetric sampled PWM

Figs. 6a and 6b show the waveforms made for both types of modulators for K_r gains with values close to the critical values and time τ_w=0. Figs. 6a and 6b show that twofold increase of the value of K_r reduces the steady state disturbance error twice. Simulations were performed for $u_i^* = 0$, therefore the value of i_{AV} means disturbance steady state error.

Below, the discrete signal of the control error is determined and formulas are derived describing the critical value of gain for the modulators shown in Figs. 4b and 4c.

The block diagram shown in Fig. 3 can be represented in the form of a pulse automatic control system (Figs. 7a and 7b). The Modulator *MOD* comprises a Zero Order Holder (ZOH) as shown in Fig. 4b or Fig. 4c. The Zero Order Holder (ZOH) consists of a pulsar of the sampling period T_p and the block $G_p(s)$ with the transfer function:

$$G_p(s) = \frac{1 - e^{-sT_p}}{s}. \tag{16}$$

Replacement of two S & H systems by one of the modulators of Figs. 4b and 4c results from the assumption of zero lead time τ_w.

Inverter ($T1$, $T2$) is represented by block K_{INV} [15, 28– 30]:

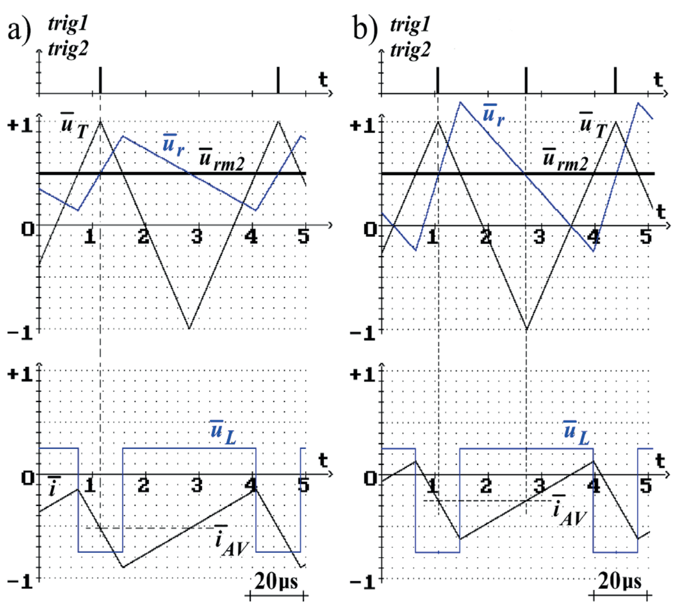

Fig. 6. Waveforms of voltage $\bar{u}_r$, $\bar{u}_T$, $\bar{u}_L$ and of current $\bar{i}$ for the symmetrical (a) and for asymmetrical regular sampled PWM (b) for $u_i^* = 0$, for $u_c/U_{DC} = 0.25$, for $K_r = 0.95\ K_{r,cr}$ and for $\tau_w = 0$

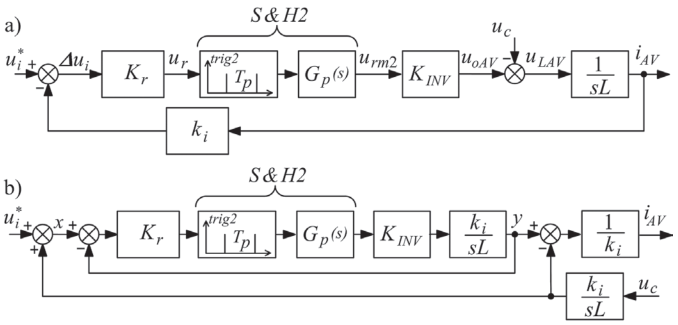

Fig. 7. Average value model block diagram representation of active filter control system (a) and its transformed form (b)

$$K_{INV} = \frac{U_{DC}}{2U_T}. \tag{17}$$

The following magnitudes u_{oAV}, u_{LAV} and i_{AV} represent mean values of the inverter output voltage, the voltage across the inductor L and the output current of the inverter, respectively. The mean values are calculated for one period of the T_p. Fig. 6 shows that for $\tau_w = 0$, the sample values are equal to the average current values for both types of modulation:

$$i_{AV} = i(mT_p), \tag{18}$$

where m is the number of the next sample of the S &$H2$ system. Therefore the adoption of the model shown in Fig. 7 is justified. Fig. 7b shows the system in the form convenient for determining the total error ε_u of controlled variable i_{AV}. The transfer function $G_{yx}(z)$ of a closed loop, with the input signal being variable x and the output being variable y, is defined by the dependence

$$G_{yx}(z) = \frac{Y(z)}{X(z)}. \tag{19}$$

Transfer function $G_{yxo}(s)$ of continuous portion of the open loop is

$$G_{yxo}(s) = \frac{k_i K_r U_{DC}}{2U_T L} \frac{1 - e^{-sT_p}}{s^2}. \tag{20}$$

Transfer function $G_{yxo}(s)$ corresponds to the pulse transfer function $G_{yxo}(z)$:

$$G_{yxo}(z) = \frac{k_i K_r U_{DC}}{2U_T L} \frac{T_p}{z - 1}. \tag{21}$$

The transfer function of closed system $G_{yx}(z)$ has the form:

$$G_{yx}(z) = \frac{1 - b}{z - b}, \tag{22}$$

where:

$$b = 1 - \frac{k_i K_r U_{DC} T_p}{2U_T L}. \tag{23}$$

Based on the diagram shown in Fig. 7b, we can write:

$$I_{AV}(z) = \frac{1}{k_i} G_{yx}(z) U_i^*(z) + \\ + Z\left\{ L^{-1}\left[\frac{U_c(s)}{sL}\right]_{t=mT_p} \right\}\left[G_{yx}(z) - 1\right], \tag{24}$$

where Z is the operator of the discrete transform, L^{-1} is the operator inverse Laplace transform.

The overall deviation of the system shown in Fig. 7 is defined by the following relationship:

$$\varepsilon_u(m) = u_i^* - i_{AV}. \tag{25}$$

According to the definition of control deviation given in [31], it results that Δu_i signal is equal to this deviation for k_i=1 only.

The Z transform of error ε_u defined by (25) can be determined on the basis of (22, 24):

$$E_u(z) = \left[\frac{z - 1}{z - b} + \frac{a}{z - b}\right] U_i^*(z) + \\ + Z\left\{ L^{-1}\left[\frac{U_c(s)}{sL}\right]_{t=mT_p} \right\} \frac{z - 1}{z - b}, \tag{26}$$

where:

$$a = \frac{(k_i - 1) K_r U_{DC} T_p}{2U_T L}. \tag{27}$$

The $\varepsilon_u(m)$ control error contains two components: the error associated with the reference signal u_i^*(tracking error) and the error associated with the u_c disturbance signal (disturbance error):

$$\varepsilon_u(m) = \varepsilon_{ui}(m) + \varepsilon_{uc}(m). \tag{28}$$

The first component of equation (26) is a transform of tracking error $E_{ui}(z)$, the second is a transform of disturbance error $E_{uc}(z)$.

The Z transform $E_{ui}(z)$ has the form:

$$E_{ui}(z) = \left[\frac{z - 1}{z - b} + \frac{a}{z - b}\right] U_i^*(z). \tag{29}$$

By forcing $u_i^*(t) = U_i^* \, 1(t)$ we obtain:

$$E_{ui}(z) = \frac{z}{z - b} U_i^* + a \frac{z}{(z - 1)(z - b)} U_i^*. \tag{30}$$

The original of tracking error is described by the following relationship:

$$\varepsilon_{ui}(m) = U_i^* b^m 1(m) + a U_i^* \frac{1 - b^m}{1 - b} 1(m). \tag{31}$$

When we insert a, b given by (27, 23) into equation (31), we obtain:

$$\varepsilon_{ui}(m) = \frac{U_i^*}{k_i}\left(1 - \frac{k_i K_r U_{DC} T_p}{2U_T L}\right)^m 1(m) + U_i^* \frac{k_i - 1}{k_i} 1(m). \quad (32)$$

The first component of equation (32) describes the transient tracking error $\varepsilon_{ui,t}$, while the second is the steady-state tracking error $\varepsilon_{ui,ss}$. Due to simplification, the control errors can be described without marking that they are discrete functions. The transient tracking error $\varepsilon_{ui,t}$ will decrease asymptotically to zero if the absolute of the base of power in the first factor of equation (32) is lower than unity.

The condition for asymptotic stability of the system is the fulfilment of inequality:

$$0 < \frac{k_i K_r U_{DC} T_p}{2U_T L} < 2. \quad (33)$$

The maximum value of K_r, for which the condition (33) is true is the critical value of gain $K_{r,cr}$.

The asymmetrical sampling method is not equivalent to doubling the sampling frequency; however, when substituting $\tau_w = 0$, the model shown in Fig. 7 (correct for the average current) distinguishes between symmetrical regular sampled and asymmetrical regular sampled based on the amount of samples.

For control system with symmetrical regular sampled PWM ($T_p = T_c$) we obtain relations describing $K_{r,cr}$:

$$K_{r\,cr} = \frac{4U_T L f_c}{k_i U_{DC}}. \quad (34)$$

$K_{r,cr}$ for control systems with symmetrical and with double-edge naturally sampled PWM are described by the same expressions (15, 34). For control system with asymmetrical regular sampled PWM ($T_p = T_c/2$) we obtain:

$$K_{r\,cr} = \frac{8U_T L f_c}{k_i U_{DC}}. \quad (35)$$

The minimum time settings of the control system can be determined from the condition:

$$\frac{k_i K_r U_{DC} T_p}{2U_T L} = 1. \quad (36)$$

Equation (36) is a result of adopting zero value of the power base of the first part (32).

Such minimum-time setting of K_r ensures aperiodic stability. One can assume the minimum time setting of K_r as an approximate criterion for the selection of gain.

In the control system of such settings, there is a theoretical possibility of obtaining a steady state after T_p time. Asymmetrical regular sampled PWM offers the possibility of a faster decay of the $\varepsilon_{ui,t}$ component.

Simulation studies demonstrate the advantages of asymmetrical regular sampled PWM in terms of decay time t_d of the transient error component.

Fig. 8a shows a simulation of the relative value of $\bar{\imath}$ current at step change in setpoint value of $\bar{u}_i^*$ for a regularly sampled symmetric PWM while Fig. 8b – for a regularly sampled asymmetric PWM system for minimum-time settings ($K_r = K_{r,cr}/2$). Simulation studies were performed for $\tau_w = 1.5$ μs.

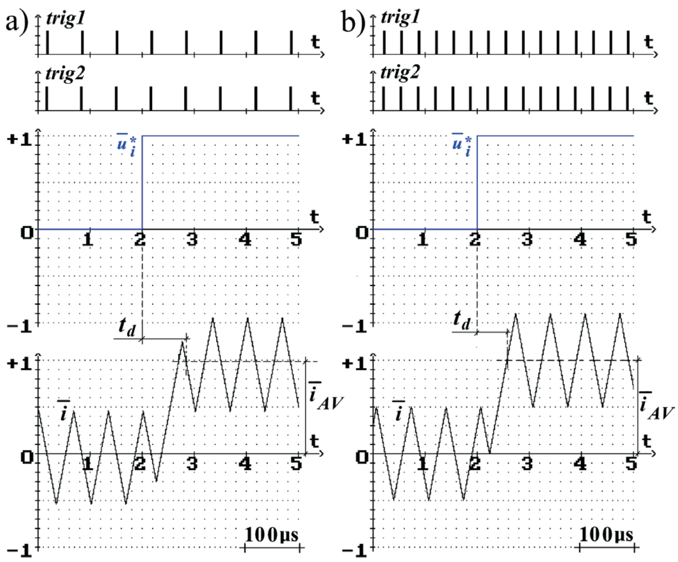

Fig. 8. Waveforms of the reference signal $\bar{u}_i^*$ and of $\bar{\imath}$ current for the symmetrical (a) and asymmetrical regular sampled PWM (b) for minimum-time setting of K_r, for $u_c = 0$ and for $\tau_w = 1.5$ μs

Steady-state tracking error $\varepsilon_{ui,ss}$ described by the second part of equation (32) for both types of modulation can be determined from the relationship:

$$\varepsilon_{ui,s} = U_i^* \frac{k_i - 1}{k_i}. \quad (37)$$

For $k_i = 1$ is error $\varepsilon_{ui,ss} = 0$, which means that the control system shown in Figs. 7a and 7b, representing the block diagram shown in Fig. 3 with the ideal inductance L, is for $u_c = 0$ an astatic system.

From the above analysis one can conclude that for $\tau_w = 0$, both types of modulation are equivalent in terms of steady state tracking error of the control system with zero disturbance signal ($u_c = 0$).

7. Disturbance error in control systems with symmetric and asymmetric sampled PWM

According to equation (25), disturbance error ε_{uc} for $u_i = 0$ is:

$$\varepsilon_{uc} = -i_{AV}. \quad (38)$$

The second component of equation (26) is a discrete transform $E_{uc}(z)$ of the disturbance error ε_{uc}:

$$E_{uc}(z) = Z\left\{L^{-1}\left[\frac{U_c(s)}{sL}\right]_{t=mT_p}\right\}\frac{z-1}{z-b}. \quad (39)$$

By forcing $u_c(t) = U_c 1(t)$, we obtain the pulse transfer function $E_{uc}(z)$:

$$E_{uc}(z) = \frac{U_c T_p}{L}\frac{z}{(z-1)(z-b)}. \quad (40)$$

Original of disturbance error is described by the following relationship:

$$\varepsilon_{uc}(m) = -\frac{2U_T U_c}{k_i K_r U_{DC}}\left(1 - \frac{k_i K_r U_{DC} T_p}{2U_T L}\right)^m 1(m) + \frac{2U_T U_c}{k_i K_r U_{DC}} 1(m). \quad (41)$$

The first component of equation (41) describes the transient disturbance error $\varepsilon_{uc,t}$, while the second is the steady-state disturbance error $\varepsilon_{uc,ss.}$ Equation (41) shows that for $K_r \approx K_{r,cr}/2$, transient disturbance error $\varepsilon_{uc,t}$ decays faster for asymmetrical regular sampled PWM.

The steady-state disturbance error $\varepsilon_{uc,ss}$ for both types of modulation can be determined from the relationship:

$$\varepsilon_{uc,s}(m) = \frac{2U_T U_c}{k_i K_r U_D} 1(m). \quad (42)$$

From equations (32, 41) it follows that disturbance errors more strongly depend on the value K_r.
Fig. 9a shows a simulation of the relative value of $\bar{i}$ current at step change in setpoint value of $\bar{u}_c$ for a regularly sampled symmetric PWM, while Fig. 9b – for a regularly sampled asymmetric PWM system for minimum-time settings (K_r=$K_{r,cr}/2$). Simulation studies were performed for τ_w = 1.5 µs. System with asymmetric sampled PWM offers the possibility of a significantly faster decay of the $\varepsilon_{uc,t}$ component.

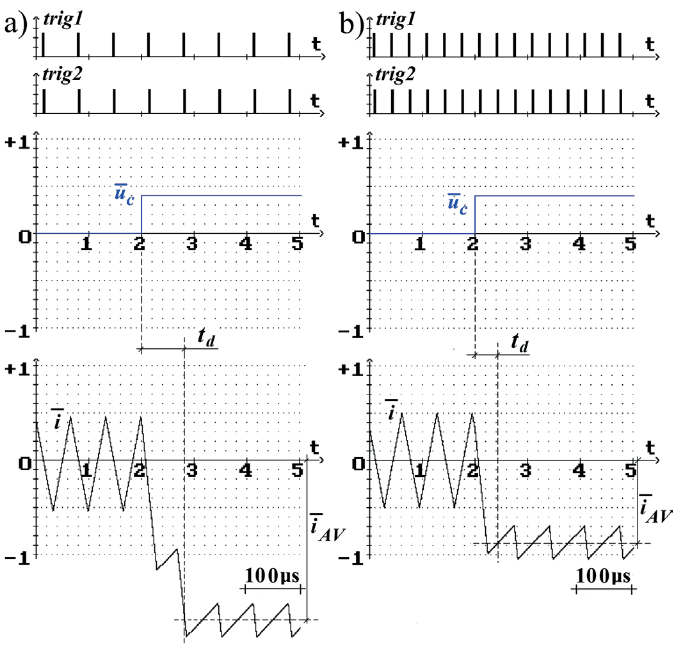

Fig. 9. Waveforms of the disturbance signal $\bar{u}_c$ and of $\bar{i}$ current for the symmetrical (a) and for the asymmetrical regular sampled PWM (b) for minimum-time setting of K_r, for u_i^* = 0 and for τ_w = 1.5 µs

8. Steady-state disturbance error for non-zero PWM computation delay

Below, equations are derived describing the steady-state disturbance error taking into account the time τ_w for both types of modulation.

From the viewpoint of the control time, the sinusoidal course of u_c voltage may be taken as constant. The analysis will be limited to the determination of steady-state disturbance error $\varepsilon_{uc,ss}$. Below we will determine the offset current in the control system with symmetrical regular sampled PWM. At steady state (Fig. 10), the average voltage value across the inductance L for period T_c is zero. Hence the equality

$$u_{Lmax}\tau + u_{Lmin}(T_c - \tau) = 0 \quad (43)$$

(where $u_{Lmax} = 0.5U_{DC} - u_c$, $u_{Lmin} = -0.5U_{DC} - u_c$) is valid, from which τ time can be determined:

$$\tau = \frac{0.5U_{DC} + u_c}{U_{DC}} T_c. \quad (44)$$

The average error for the period T_c resulting from the non-zero voltage u_c and finite gain value of K_r (for τ_w = 0) can be determined from the similarity of triangles (*ABC* and *ADE)*:

$$\frac{U_T + i_{\tau w} k_i K_r}{T_c - \tau} = \frac{2U_T}{T_c}. \quad (45)$$

Substituting (44) to (45) we obtain:

$$i_{\tau w} = -\frac{2u_c U_T}{k_i K_r U_{DC}}. \quad (46)$$

The average value of the output current i_{AV} in steady state operation of the inverter for the period T_c is:

$$i_{AV,ss} = i_{\tau w} + \Delta i_{\tau w}, \quad (47)$$

where $i_{AV,ss}$ is a mean value of the current in a steady state, $\Delta i_{\tau w}$ means an additional error due to the non-zero lead time τ_w . The error is defined by the relationship:

$$\Delta i_{\tau w} = -\frac{0.5U_{DC} + u_c}{L}\tau_w. \quad (48)$$

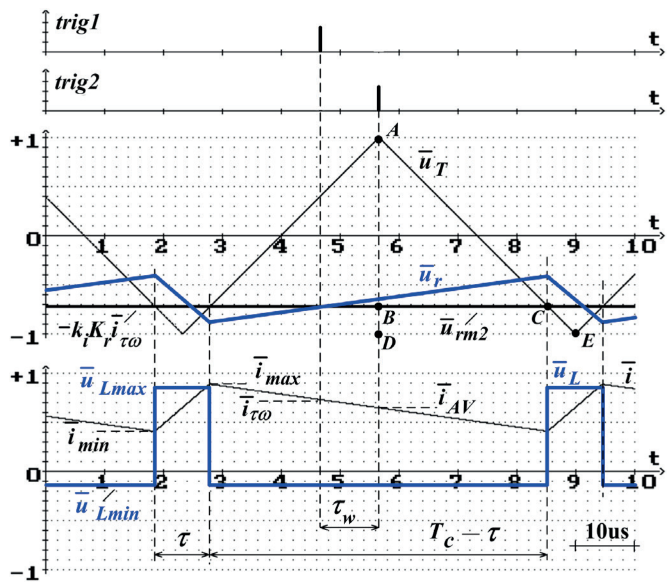

Fig. 10. Waveforms of voltage $\bar{u}_r$ $\bar{u}_T$,$\bar{u}_L$ and of current $\bar{i}$ for the symmetrical regular sampled PWM for u_i^* = 0, for u_c < 0 and for $K_r \le K_{r,cr}$

Steady-state disturbance error $\varepsilon_{uc,ss}$ is described, according to (38), by the new relationship:

$$\varepsilon_{uc,ss} = -i_{AV,ss} \tag{49}$$

Thus, the steady-state disturbance error value is equal to the negative average $i_{AV,ss}$:

$$\varepsilon_{uc,ss} = \frac{2u_c U_T}{k_i K_r U_{DC}} + \frac{U_{DC}+2u_c}{2L}\tau_w . \tag{50}$$

For $u_c<0$, in the range of small values of τ_w, steady-state disturbance error decreases with the increase of τ_w, while for $u_c > 0$, the absolute value of the error decreases (Fig. 12).

Below, a formula is derived defining the critical gain $K_{r,cr}$ in the control system with asymmetrical regular sampling for small values of τ_w / T_c.

The formulas (43, 44) are valid for systems irrespective of the type of PWM modulation.

On the basis of simulation studies for $u_c \leq 0$, it was observed that for small values of $\tau_w / T_c > 0$, the value of the sample taken before the negative apex of the triangular auxiliary voltage corresponds exactly to the minimum value of the output current of the inverter. Similarly, for $u_c \geq 0$ it has been observed that for small values of $\tau_w / T_c > 0$, the value of the sample taken prior to the positive apex of auxiliary triangular voltage corresponds exactly to the maximum output current of the inverter.

The first case is illustrated by the waveforms shown in Fig. 11. Using the similarity of triangles (*FGH* and *ADE* or *ABC* an *ADE,* respectively) we derive the following two relationships:

$$\frac{U_T - k_i K_{rc} i_{min}}{\tau - \tau_w} = \frac{4U_T}{T_c} \tag{51}$$

$$\frac{U_T + k_i K_{rc} i_{\tau w}}{0.5T_c - \tau_w} = \frac{4U_T}{T_c}. \tag{52}$$

After time ($T_c/2$ τ) the value of the current decreases from i_{max} to $i_{\tau w}$, which is shown by equation

$$i_{max} = i_{\tau w} + \frac{0.5U_{DC}+u_c}{L}\left(\frac{T_c}{2} - \tau\right). \tag{53}$$

The increase of the current in time τ is described by the following relation:

$$i_{max} - i_{min} = \frac{0.5U_{DC}-u_c}{L}\tau . \tag{54}$$

From equations (44, 51–54), we obtain a relation that describes the critical gain for small values of τ_w/T_c for the control system with the sampled regular asymmetrical PWM:

$$K_{r\,cr} = \frac{8U_T L f_c}{k_i\left(0.5U_{DC}+u_c\right)}\left(\frac{1}{2} + \frac{u_c}{U_{DC}} - 2\frac{\tau_w}{T_c}\right). \tag{55}$$

Running a similar analysis for $u_c \geq 0$ allows for generalization of the above relation for positive and negative values of u_c:

$$K_{r\,cr} = \frac{8U_T L f_c}{k_i\left(0.5U_{DC}-|u_c|\right)}\left(\frac{1}{2} - \frac{|u_c|}{U_{DC}} - 2\frac{\tau_w}{T_c}\right). \tag{56}$$

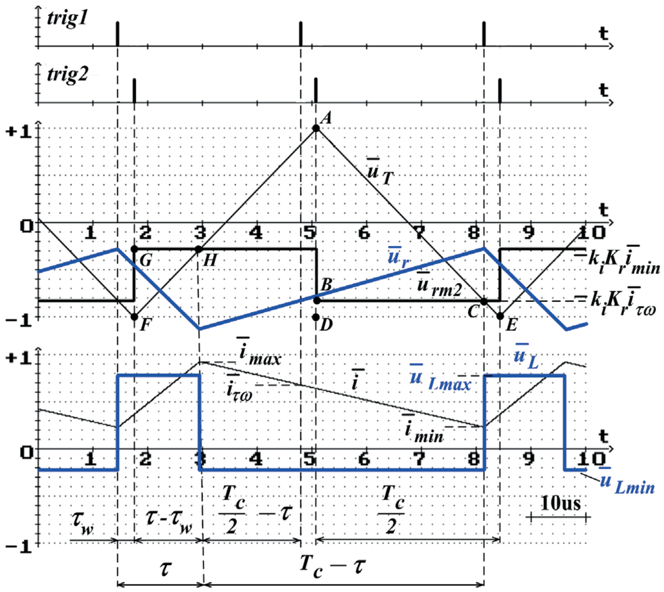

Fig. 11. Waveforms of voltage $\bar{u}_r$, $\bar{u}_T$, $\bar{u}_L$ and of current $\bar{i}$ for the asymmetrical regular sampled PWM for $u_i^*=0$, for $u_c<0$ and for $K_r=K_{r,cr}$

Fig. 13a shows that the increase of τ_w causes a decrease of $K_{r,cr}$ to values described by equation (34). Comparing the right sides of (34) and (56), we obtain the equation which can be used for determining the limit value of τ_w for which (56) is met.

The limit of τ_w, for which (56) is true is described by the following relation:

$$0 < \frac{\tau_w}{T_c} < \frac{1}{8} - \frac{|u_c|}{4U_{DC}}. \tag{57}$$

Formula (56) for $\tau_w \to 0$ takes the form:

$$K_{r,cr} = \frac{8U_T L f_c}{k_i U_{DC}}. \tag{58}$$

Equation (58) is identical to equation (35), obtained on the assumption that the inverter may be replaced by a linear circuit with an output voltage equal to the average value for the T_c period, set at the time of sampling the output current. It is clear from the above relations that the control system of asymmetrical regular sampled PWM allows for setting higher values of the K_r gain controller as compared to the value of the symmetrical regular sampled PWM, especially for small values of $\tau_w/T_c > 0$, so further considerations will apply to this case.

The value of the $i_{AV,ss}$ average current is equal to:

$$i_{AV,ss} = \frac{i_{max}+i_{min}}{2}. \tag{59}$$

Using formulas (44, 51–53), for $u_c \leq 0$, we obtain:

$$i_{AV,ss} = -\frac{2U_T u_c}{k_i K_{rc} U_{DC}} - \frac{u_c}{U_{DC}}\frac{U_{DC}+2u_c}{4L}T_c. \tag{60}$$

Having run an identical analysis for $u_c \geq 0$ and considering a linear nature of the control circuit ($\varepsilon_{uc,ss} = -i_{AV,ss}$ for $u_i^* = 0$), the following formula for steady-state disturbance error is obtained:

$$\varepsilon_{uc,ss} = \frac{2U_T u_c}{k_i K_{rc} U_{DC}} + \frac{u_c}{U_{DC}} \frac{U_{DC} - 2|u_c|}{4L} T_c. \tag{61}$$

Simulation studies (Fig. 6b) for the case when $\tau_w = 0$ and $K_r \leq K_{r,cr}$, showed that the sampled reference u_{rm2} is constant in time and waveforms of u_r , u_L and i are similar to the waveforms for the circuit with symmetrical regular sampled PWM for $\tau_w = 0$. Thus, the error for the system of asymmetrical regular sampled PWM for $\tau_w = 0$ is specified by the first component of the formula (61):

$$\varepsilon_{uc,ss} = \frac{2U_T u_c}{k_i K_r U_{DC}}. \tag{62}$$

For zero value of time τ_w, the steady-state disturbance error in the system with asymmetrical regular sampled PWM can be half of the steady-state disturbance error in the system of symmetrical regular sampled PWM.

Figs. 12 and 13 show the critical gains and steady-state errors $\delta_{uc,ss}$ expressed in the p.u. system as function of τ_w/T_c, determined on the basis of simulations. It is assumed that the fixed state is at the time when the current at the beginning and end of the period T_c does not differ by more than 1% of the base value I_b, as described by formula (9).

Critical gain is referenced to the value given by formula (34), while the error is referenced to the base value of I_b current.

$$\delta_{uc,ss} = \frac{\varepsilon_{uc,ss}}{I_b} \tag{63}$$

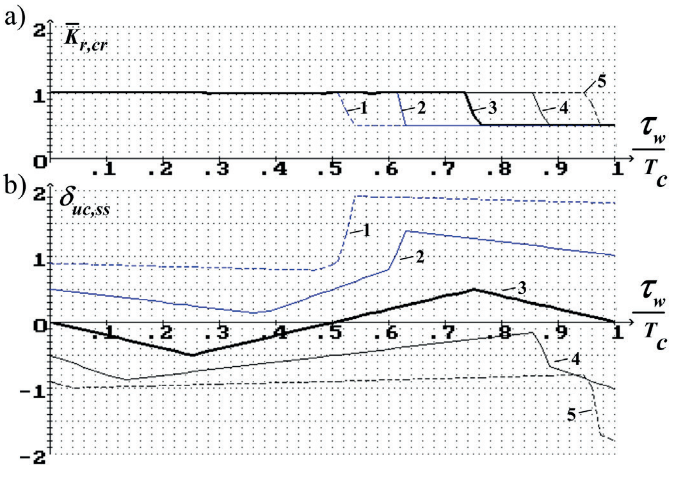

Fig. 12. Relative value of critical gain (a) and relative value of error (b) in a system with symmetrical regular sampled PWM for $u_i^* = \text{const}$

Individual characteristics were obtained for the following data: waveform 1 for $\bar{u}_c = -0.44$, waveform 2 for $\bar{u}_c = -0.25$, waveform 3 for $u_c = 0$, waveform 4 for $\bar{u}_c = 0.25$, waveform 5 for $\bar{u}_c = 0.44$.

The $\delta_{uc,ss}$ variables for waveform 3 show the relative values of steady-state error for the case $u_c = 0$. Therefore, the $\delta_{uc,ss}$ variables for this case can be treated as relative values of steady-static error associated with the set point u_i^*. For symmetrical regular sampled PWM, steady-state error $\varepsilon_{ui,ss}$ strongly depends on the time τ_w. For asymmetrical regular sampled PWM, this dependence does not occur.

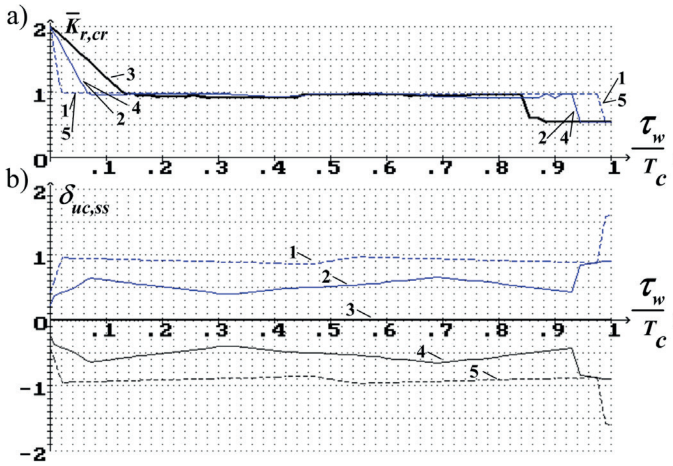

Fig. 13. Relative value of critical gain (a) and relative value of error (b) in a system with asymmetrical regular sampled PWM for $u_i^* = \text{const}$

In real systems, the average value of the output voltage of the inverter depends on the simultaneous minimum off-time of the two transistors of each branch of the inverter (t_{dead}). For continuous output current of the inverter u_{oAV} value is described by the relationship:

$$u_{oAV} = K_r \frac{U_{DC}}{2U_T} \Delta u_i - U_{DC} t_{dead} f_c sign(i). \tag{64}$$

The magnitudes used in the above formula are indicated in Figs. 3 and 4. The second component changes replacement gain of the open loop system, for which Δu_i is input and u_{oAV} is output signal, respectively. This fact causes a certain impact of t_{dead} on the value of the critical gain $K_{r,cr}$. In this article, this effect is not evaluated, whereas simulation tests, the results of which are shown below were made for the inverter models that take into account the non-zero value of t_{dead}.

In the control circuit of the output current of the inverter shown in Fig. 3, disturbance error $\varepsilon_{uc,ss}$ was described in equation (50) for symmetrical regular sampled PWM and in equation (61) for asymmetrical regular sampled PWM. If the voltage u_c is a sinusoidal function, the disturbance error $\varepsilon_{uc,ss}$, assuming $\tau_w = 0$ for both modulators, also varies sinusoidally. This means that even for a reference value of $u_i^* = 0$, at the output of the inverter shown in Fig. 3 the current component will appear in phase with the voltage u_c.

9. APF output current error

The control system with a voltage regulator in the DC circuit in the *APF* enforces an additional component of the reference signal of its output current, compensating the disturbance error of the proportional current controller, ensuring also the reactive nature of the output current of the parallel active filter in a steady state operation.

By neglecting the *Tr1* magnetizing currents and *C* capacitors currents, considerations for error in *APF* output current can be reduced to evaluation of the overall error in total output current (i) of two inverters. For clarity of the following considerations, the vector magnitudes were replaced by their components without indices *1, 2, 3*:

As shown in Fig. 1, i output current of each phase has two components:

$$i = i_{\underline{1}} + i_{\underline{2}}. \tag{65}$$

Fig. 2 shows a control diagram for the first phase of the *APF*. For the remaining phases the scheme is the same. In order to generalize the below analysis for errors in any *APF* symbols of phase voltage, current, setpoint signal and erorr index 1 is omitted.

Setpoint signal of i current contains three components:

$$i^* = i^*_{p(DC)} + i^*_f + i^*_h. \tag{66}$$

The $i^*_{p(DC)}$ is a component of the setpoint signal of current in phase with the u_c voltage, controlling the voltage u_{DC}. The i_h^* component contains the sum of selected harmonics of load currents according to the respective phases as shown in Fig. 2. The i_f^* current comprises two components:

$$i^*_f = i^*_{fsin} + i^*_{fcos}, \tag{67}$$

where the fundamental frequency component of i^*_{fsin} is in phase with the voltage u_c, and the fundamental frequency component of i^*_{fcos} is orthogonal to u_c voltage. In the *APF* system, i^* is the setpoint for total output current of the inverters and, therefore, the total error ε is described by the following relationship:

$$\varepsilon = i^* - i \tag{68}$$

The error ε is discrete in digital regulation, but for the following analysis it will be presented as a continuous quantity.

For the control system of the total output current of two active filter inverters, the setpoint signal is the sum of $u^*_{i\_1} + u^*_{i\_2}$ Thus, error ε_u is described by the new relationship:

$$\varepsilon_u = k_{iref} i^* - i \tag{69}$$

In the *APF* system in the states of unsettled average voltage u_{DC}, we can distinguish five components of the inverters output current i: the fundamental frequency components of $i_{p(DC)sin}$ and i_{fsin} that are in phase with the u_c voltage, the fundamental frequency component of i_{fcos} orthogonal to u_c voltage, the component containing higher harmonics i_h and the i_{car} component including sideband harmonics of f_c:

$$i = i_{p(DC)} + i_{fsin} + i_{fcos} + i_h + i_{car}. \tag{70}$$

The i_{car} component of i current does not depend on the coefficient of K_r, while the error for the remaining components can be written as the sum of the errors of the fundamental components $\varepsilon_{p(DC)}$, ε_{fsin}, ε_{fcos} and component containing higher harmonics ε_h:

$$\varepsilon = \varepsilon_{p(DC)} + \varepsilon_{fsin} + \varepsilon_{fcos} + \varepsilon_h, \tag{71}$$

wherein ε, $\varepsilon_{p(DC)}$, ε_{fsin}, ε_{fcos} and ε_h are errors corresponding to setpoint signals i^*, $i^*_{p(DC)}$, i^*_{fsin}, i^*_{fcos} and i_h^*, respectively:

$$\varepsilon_{p(DC)} = i^*_{p(DC)} - i_{p(DC)} \tag{72}$$

$$\varepsilon_{fsin} = i^*_{fsin} - i_{fsin} \tag{73}$$

$$\varepsilon_{fcos} = i^*_{fcos} - i_{fcos} \tag{74}$$

$$\varepsilon_h = i^*_h - i_h. \tag{75}$$

The u_c value in the active filters is the phase voltage u_{c1}, u_{c2} or u_{c3}. Since in the steady state operation of the filter, the mean (for the period of the mains voltage) value of $U_{DC,AV}$ is constant, i current does not contain the active component ($i_{p(DC)} + i_{fsin} = 0$). This condition is achieved by forcing an appropriate value u_i* that contains a component $i^*_{p(DC)}$ proportional to u* which is a value dependent on the output signal of the u_n voltage regulator. Reducing the impact of steady state disturbance error of proportional regulator on output current of the *APF* by $i_{p(DC)}{}^*$ and $i_{fsin}{}^*$ reference signal components means for $\tau_w = 0$ satisfying the equality:

$$k_{iref}\left(i^*_{p(DC)} + i^*_{fsin}\right) = \frac{2U_T u_c}{k_i K_r U_{DC}}. \tag{76}$$

The right side of equation (76) is a disturbance error $\varepsilon_{uc,ss}$ described by (62) and the left side of the equation is associated with the component of the reference signal of inverter current ensuring no active component in the output current in a steady operating condition of the *APF*.

Another conclusion drawn from the foregoing discussion is that the current i described by formula (70) contains a non-zero sum of the components $i_{p(DC)}$ and i_{fsin} only in the states of non-zero error of the average voltage $u_{DC,AV}$, associated with the change of active power load. In the states of a steady state operation (without taking into consideration heat losses in the *APF* system), the sum of the $i_{p(DC)} + i_{fsin}$ components takes a value of zero, which means that the active filter can compensate only the reactive and deformation power, and the accuracy of the compensation depends on the value of ε_{fcos} and ε_h errors.

The influence on output current of the steady state disturbance error forced by mains voltage higher harmonics is not compensated.

10. Simulation tests of the power supply system APF

Simulation tests of the power supply system shown in Fig. 1 were performed with the following parameters: *Tr1* (400 V / 400 V), *Tr2* (400 V / 400 V / 400 V), $L_l = 20$ μH, $L_p' = 80$ μH (*Th1-Th2* and *Th7-Th12* rectifier side dispersion inductance of *Tr2*), $L_s' = 3$ μH, armature inductance $L_a = 1$ mH, armature resistance $R_a = 10$ mΩ , $k_i = 1$, $k_{uf} = 1$, parameters of voltage controller u_{DC}: $T_n = 1.25$ s, $K_n = 0.0044$, constant of multiplier

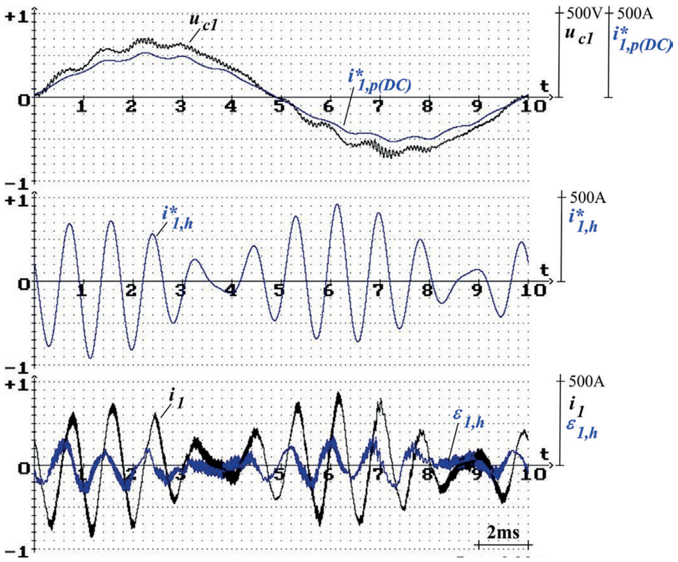

Fig. 14. Simulation of waveforms of reference currents $i^*_{1,p(DC)}$, $i^*_{1,h}$, current i_1(500 A/div), current error $\varepsilon_{1,h}$ (500 A/div) and voltage u_{c1} (500 V/div) in compensation system with symmetrical regular sampled PWM

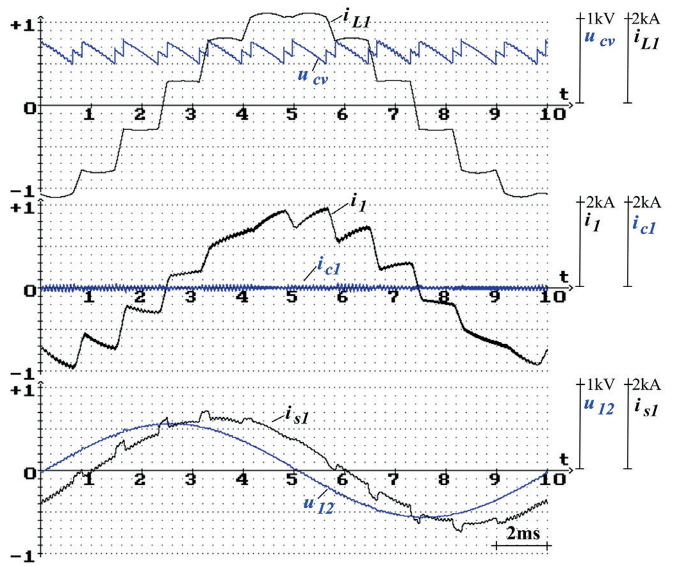

Fig. 16. Simulation of waveforms of currents: i_{L1}, i_1 i_{s1}, i_{c1} (2 kA/div) and voltages u_{CV}, u_{12} (1 kV/div) in compensation system with symmetrical regular sampled PWM

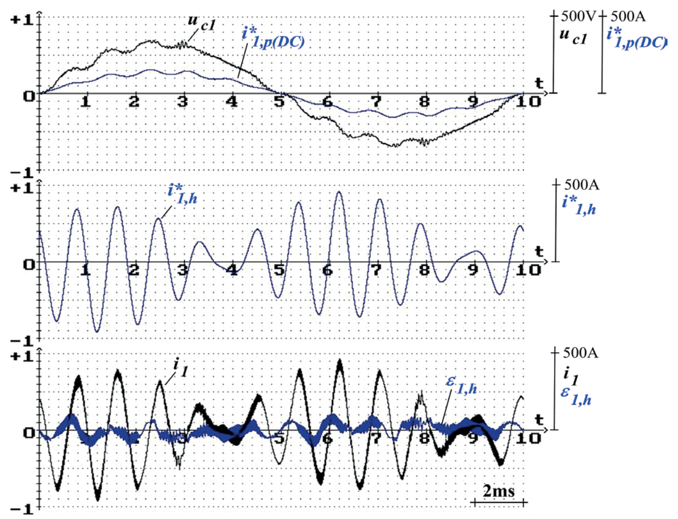

Fig. 15. Simulation of waveforms of reference currents $i^*_{1,p(DC)}$, $i^*_{1,h}$, current i_1 (500 A/div), current error $\varepsilon_{1,h}$ (500 A/div) and voltage u_{c1} (500 V/div) in compensation system with asymmetrical regular sampled PWM

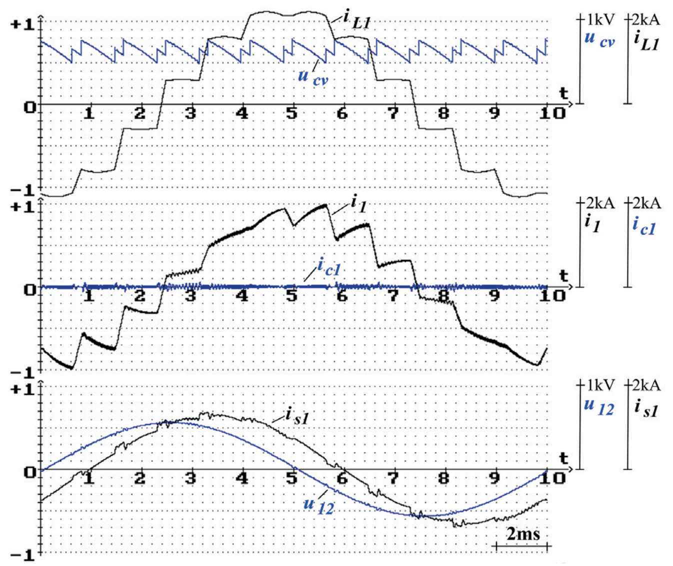

Fig. 17. Simulation of waveforms of currents: i_{L1}, i_1 i_{s1}, i_{c1} (2 kA/div) and voltages u_{CV}, u_{12} (1 kV/div) in compensation system with asymmetrical regular sampled PWM

system $k_M = 20$, armature current $I_a = 992$ A, armature voltage $U_a = 619$ V, firing angle of *SCR* converter $\alpha = 50°$, $k_{iref} = 0.5$, $k_{iL} = 1/\sqrt{3}$, $C_{DC} = 2.7$ mF, $C = 50$ μF, $L = 80$ μH, $U_{DC} = 720$ V, $f_c = 15$ kHz , $\tau_w = 1.5$ μs, $t_{dead} = 2$ μs and for the maximum value of the triangular carrier $U_T = 5.5$ V.

Figs. 14 and 15 show the results of simulation research on compensation for *11th* and *13th* harmonic for symmetrical and asymmetrical regular sampled PWM in stable operation of the filter for which the i_1 output current has no fundamental components ($i_1 = i_{1,h}$), respectively. Waveforms of errors $\varepsilon_{1,h}$ for both types of modulators indicate lower instantaneous values of error for asymmetrical regular sampled PWM.

Figs. 14 and 15 also show waveforms illustrating the compensation forced by the set-point component $i^*_{1,p(DC)}$ of the error of the inverter output current i_1 of *APF* inverters, resulting from the non-zero value of instantaneous u_{c1} voltage. For a system with symmetrical regular sampled PWM, for which the *APF* worked stably at a lower value of K_r, the maximum value $i^*_{1,p(DC)}$ required to compensate the $\varepsilon_{1,p(DC)}$ error must be larger than the value required in the system of asymmetrical regular sampled PWM.

The simulation (Figs. 16 and 17) was carried out for the case of a closed S_{w1} in Fig. 2, which means the compensation of reactive power and deformation reactive power shift.

Waveforms shown in Fig. 16 were obtained for a system with symmetrical regular sampled PWM. The system worked steadily for $k_i K_r$ = 0.021 and the obtained output coefficients were THD_i = 7.74% and THD_u = 1.33%, respectively. For a system with asymmetrical regular sampled PWM (Fig. 17), stable operation was ensured by the following product $k_i K_r$ = 0.045 V/A, and significantly better results were achieved: THD_i = 4.41%, THD_u = 1.1%.

11. Experimental studies

In order to verify the correctness of the analysis of the properties of the modulator with asymmetric sampled PWM, studies have been conducted with FAS-400k-400 active filter produced in MEDCOM company. Tests were conducted in industrial conditions in a coal mine. APF works as a compensator of high harmonic currents consumed by a lifting machine in the mine (for the case of open S_{w1} in Fig. 2).

Filter parameters U_{DC}, C_{DC}, C, L, f_c, t_{dead} correspond with those assumed for the simulation studies. The remaining parameters are: k_{iL} = 0.00625, k_{uf} = 2.72, υ_z = 26, k_i = 0.0025, k_{iref} = 0.65, *Tr1* (6 kV / 400 V / 1.6 MVA / short-circuit voltage 5.68%).

Due to the fact that the *APF* inverters are connected to the medium voltage network via *Tr1* transformer, a problem appears concerning phase shifts in the general case, which are different for the different harmonics. Phase error was also introduced by industrial current transducers used for measuring the load current. Therefore, the control system uses individual selection of phase correction-values for each harmonic.

Waveforms shown in Figs. 18a, 18b, and 18c were taken in the active filter in its normal operation state. In practice, waveforms shown in Fig. 18b with sufficient approximation satisfy the following equation, which shows the small control error of filter output current:

$$i_1 = 2 i^*_{1,h} k_{iref} / k_i. \tag{77}$$

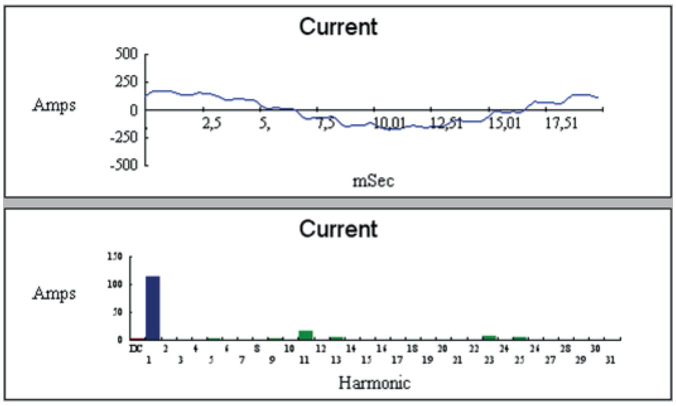

Fig. 19. Time waveforms of current i_{s1} and frequency spectrum of this current (values should be multiplied by 1.2) in power system with filter off

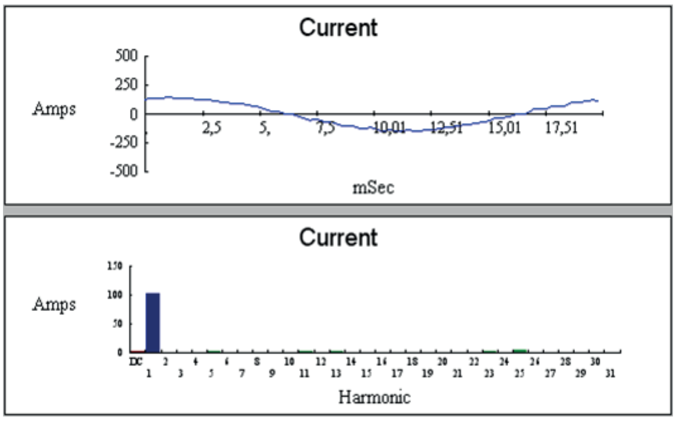

Fig. 20. Time waveforms of current i_{s1} and frequency spectrum of this current (values should be multiplied by 1.2) in power system with filter on (f_c = 15 kHz, $k_i K_r$ = 0.021) with symmetrical regular sampled PWM

Equation (77) was obtained on the basis of the current control loop (Fig. 2) assuming full compensation of the selected harmonics which means acceptance of $\varepsilon_{1,h}$ = 0.

(a) (b) (c)

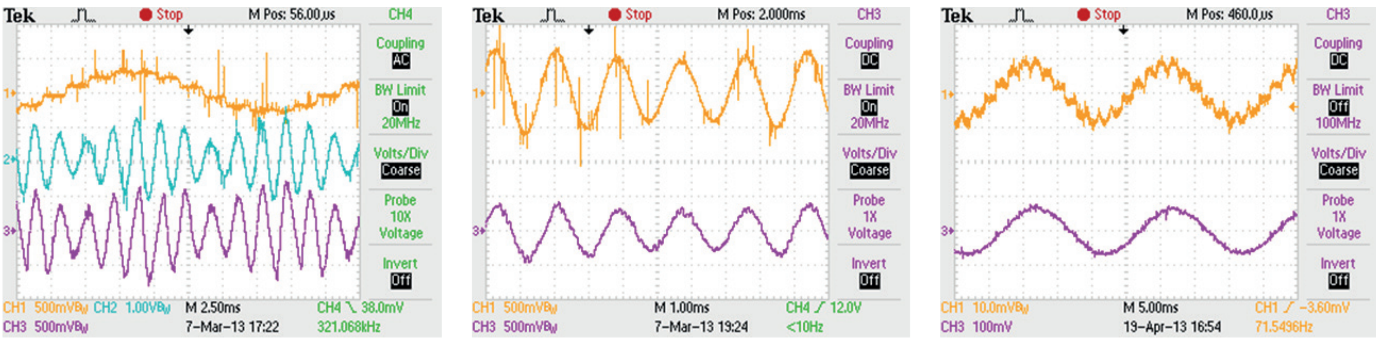

Fig. 18. Experimental results of a system with asymmetrical regular sampled PWM. (a) waveform of load current i_{L1} (CH1: 180 A/div) and current setpoint signal $i^*_{1,h}$ (CH2: 1 A/div) and current i_1 (CH3: 500 A/div) for compensation of *11th* and *13th*; (b) waveform of setpoint signal $i^*_{1,h}$ (CH1: 0.5 A/div), of output filter current i_1 (CH3: 500 A/div); (c) waveform of load current i_{L1} (CH1:90A/div) and input main current i_{s1} (CH2: 120 A/div)

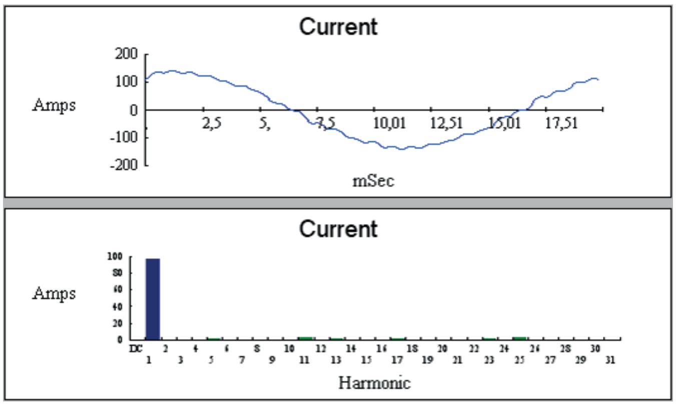

Fig. 21. Time waveforms of current i_{s1} and frequency spectrum of this current (values should be multiplied by 1.2) in power system with filter on (f_c = 15 kHz, k_iK_r = 0.045) with asymmetrical regular sampled PWM

Lack of components with voltage ripple u_{c1} in waveforms of reference signal $i_{1,h}^*$ and current i_1 indicates that the disturbance error of proportional controller $\varepsilon_{uc,ss}$ forced by this voltage does not affect the output current of the *APF*.

The experimental results were obtained for the filter output current control system with symmetrical or asymmetrical regular sampled PWM.

Figs. 18–21 and Table 1 present the currents measured in the 6 kV main grid together with the input current harmonic distortion factor THD and the r.m.s. values of individual harmonics (the system with a disabled filter, and a system with enabled filter with a preset compensation of *11th*, *13th* and *23th* current harmonics). THD_i factor equal to 14.8 % was reduced to 5.45% when the filter was on for k_iK_r = 0.021 V/A and to 4.85% for k_iK_r = 0.045 V/A.

Table 1

f_c = 15kHz	I	I_{harm}	THD_i	I_{11h}	I_{13h}	I_{23h}
	A_{rms}	A_{rms}	%	A_{rms}	A_{rms}	A_{rms}
APF off	115.4	17	14.8	15	4.44	5.5
APF on/sym k_iK_r = 0.021	107.99	5.87	5.54	3.01	1.99	1.69
APF on/asym k_iK_r = 0.045	102.5	4.71	4.85	2.34	1.23	1.08

Table 1 also shows the impact of the gain of K_r on THD_i current drawn from the mains. Greater decrease in the value of *11th*, *13th* and *23th* current harmonics is visible for the control system of greater value of K_r.

12. Conclusions

The results of simulation and experimental tests show that the control system with asymmetrical regular sampled PWM allows for increasing the gain of the proportional controller in relation to the gain of the control system with symmetrical regular sampled PWM. This enables reduction of the steady-state disturbance error of the control system and reduction of the time decay of its transient component.

Critical gain of the proportional controller in a closed control system with asymmetrical regular sampled PWM strongly depends on the PWM computation delay time τ_w in the range of its small values (τ_w / T_c. < 0.15). From the point of view of minimizing the disturbance errors the advantages of asymmetrical regular sampled PWM compared to the symmetrical regular sampled PWM manifest themselves only under the condition of an appropriately small value of τ_w time.

The use of a proportional current controller in *APF* is justified by the particular property of an *APF* involving the elimination of the influence of sinusoidal steady-state disturbance error of the proportional controller on the output current of the active filter comprising a voltage regulation system in the DC circuit.

The use of a proportional controller provides very good dynamic parameters of the *APF*, which allows for achieving good compensating results in supply systems with nonlinear, non-stationary *SCR* type rectifier.

References

[1] Y. Zhang , Q. Zhang, Z. Li, Y. Zhangt, "Comparative Study of Model Predictive Current Control and Voltage Oriented Control for PWM Rectifiers", *2013 International Conference on Electrical Machines and Systems*, Busan, Korea, 2207–2212 (2013).

[2] S. Fukuda and H. Kamiya, "Adaptive learning algorithm assisted current control for active filters", in *Proc. IEEE Ind. Appl. Conf.,* 1, 179–185 (2001).

[3] R. Costa Castello, R. Grino, R. Cardoner -Parpal, and E. Fossas, "High performance control of a single-phase shunt active filter", *IEEE Transactions on Control Systems Technology,* 17, 1318–1329 (2009).

[4] A. Garcia-Cerrada, O. Pinzon-Ardila, V. Feliu-Batlle, P. Roncero-Sanchez, and P. Garcia-Gonzalez, "Application of a Repetitive Controller for a Three-Phase Active Power Filter", *Power Electronics, IEEE Transactions on,* 22, 237–246 (2007).

[5] Y. Li, X. Hao, X. Yang, R. Xie, T. Liu, "A variable-band hysteresis modulated multi-resonant sliding-mode controller for three-phase grid-connected VSI with an LCL-filter", *ECCE Asia Downunder (ECCE Asia), 2013 IEEE,* 670–674 (2013).

[6] D.G. Holmes, T.A. Lipo, *Pulse Width Modulation For Power Converters*, IEEE PRESS, Willey-Interscience, 2003.

[7] H. Fujita, "A Single-Phase Active Filter Using an H-Bridge PWM Converter With a Sampling Frequency Quadruple of the Switching Frequency", *IEEE Transactions on Power Electronics,* 24(4), 934–941 (2009).

[8] D.G. Holmes and B. McGrath, "Opportunities for harmonic cancellation with carrier-based PWM for a two-level and multilevel cascaded inverters", *IEEE Trans. Ind. Appl*., 37(2), 574–582 (2001).

[9] Z. Yi-Feng, Z. Zheng, Y. Hai-zhu, T. Kai, "A new control method for neutral-point-clamped three-level PWM rectifiers", *Consumer Electronics, Communications and Networks (CECNET),* 983–986 (2011).

[10] S.W Lu, F. Lin, X.J You, T.Q. Zheng, "Research of Multi-module PWM Rectifier for Feeding System of High-speed Maglev Vehicles", *IEEE Trans on Industrial Electronics*, 1998–2002, (2006).

[11] X. Jiang, X. Xiao, H. Liu, Y. Ma, "The Output Spectrum Analysis of High-Power Multilevel Voltage Source Converters using Double Fourier Series", *Transmission and Distribution Conference and Exhibition: Asia and Pacific*, 2005 IEEE/PES, 1–5 (2005).
[12] K. Tan, Q. Ge, Z. Yin, etc., "The optimized strategy for input current harmonic of low switching frequency PWM rectifier", *The 5th IEEE Conference on Industrial Electronics and Applications (ICIEA)*, 1057–1061 (2010).
[13] J. Liu, X. Yin, Z. Zhang, Q. Xiong, "Study on Theory and Key Technologies of Full Digital SPWM Implementation for Three-Level Neutral Point Clamped Inverter", *Communications, Circuits and Systems, 2007. ICCCAS,* 1287–1291 (2007).
[14] H. Akagi., E H. Watanabe, M. Aredes, "*Instantaneous Power Theory and Applications to Power Conditioning*", IEEE PRESS, Willey-Interscience (2007).
[15] D. G. Holmes, T. A. Lipo, B. P. McGrath, W. Y. Kong, "Optimized design of stationary frame three phase AC current regulators", *IEEE Trans. Power Electron.*, 24(11), 2417–2426 (2009).
[16] M. Maciążek, D. Grabowski, M. Pasko: "Active power filters – optimization of sizing and placement", *Bull. Pol. Ac.: Tech.* 61(4), 847–853 (2013).
[17] M. Malinowski, S. Bernet., "A Simple Voltage Sensorless Active Damping Scheme for Three Phase PWM Converters With an LCL Filter", *IEEE Trans. Ind. Electron.*, 55(4), 1876 – 1880, (2008).
[18] Y. Tang, P. C. Loh, P. Wang, F. H. Choo, F. Gao, F. Blaabjerg, "Generalized design of high performance shunt active power filter with output LCL filter", *IEEE Trans. Ind. Electron.*, 59(3), 1443–1452 (2012).
[19] L. Asiminoaei, E. Aeloiza, P. Enjeti and F. Blaabjerg,"Shunt Active-Power_Filter Topology Based on Parallel Interleaved Inverters", *IEEE Trans. Ind. Electron.,* 55(3), 1175–1189 (2008).
[20] H.G. Jeong, D.K. Yoon, and K.B. Lee,"Design of an LCL-Filter for Three-Parallel Operation of Power Converters in Wind Turbines", *Journal on Power Electronics,* 13(3), 437–445 (2013).
[21] C. Lascu, L. Asiminoaei, L. Boldea, and F. Blaabjerg, "Frequency response analysis of current controllers for selective harmonic compensation in active power filters", *IEEE Trans. Ind. Electron.*, 56(2), 337–347 (2009).
[22] C. Ben-Sheng and H. Yuan-Yih, "A minimal harmonic controller for a STATCOM", *IEEE Trans. Ind. Electron.*, 55(2), 655–664 (2008).
[23] P. Mattavelli and F. P. Marafao, "Repetitive-based control for selective harmonic compensation in active power filters", *IEEE Trans. Ind. Electron.*, 51(5), 1018–1024 (2004).
[24] O. Vodyakho, C. C. Mi, "Three-level inverter-based shunt active power filter in three-phase three-wire and four-wire systems", *IEEE Trans. Power Electron.*, 24(5), 1350–1363 (2009).
[25] F. Briz, P. García, M.W. Degner, D. Díaz-Reigosa, J.M. Guerrero, "Dynamic Behavior of Current Controllers for Selective Harmonic Compensation in Three-Phase Active Power Filters", *IEEE Transactions on Industry Applications*, 49(3), 1411–1420 (2013).
[26] M. Pasko, M. Maciążek, D. Buła, "Performance and Accuracy Comparison of Fixed and Floating – Point Realizations of the Active Power Filter Control Algorithm", *Przegląd Elektrotechniczny*, 1, 162–165 (2009).
[27] T.M. Rowan, R.J. Kerkman, T.A. Lipo,"Operation of Naturally Sampled Current Regulators in the Transition Mode", *IEEE Transactions on Industry Applications,* 1a-23(4), 586–596, (1987).
[28] D. Bula and M. Pasko,"Stability analysis of hybrid active power filter", *Bull. Pol. Ac.: Tech.* 62(2), 279–286 (2014).
[29] D. G. Holmes, B.P. Grath, and S.G Parker, "Current Regulation Strategies for Vector-Controlled Induction Motor Drives", *IEEE Transactions on Industrial Electronics,* 59(10), 3680–3689 (2012).
[30] H. Akagi, "Modern active filters and traditional passive filters", *Bull. Pol. Ac.: Tech.* 54 (3), 255–269 (2006).
[31] W. Pełczewski, "*Control Theory*", 305–319, WNT, Warszawa, 1980 (in Polish).