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A power electronics controlled current source based on a double-converter topology

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Abstract: The paper presents a conception of power electronics voltage controlled current source (VCCS) which is able much more precise mapping of its an output current in a reference signal, compared to a typical converter solution. It can be achieved by means of such interconnection of two separate converters that one of them corrects a total output current towards a reference signal. An output power of auxiliary converter is much smaller than an output power of main one. Thanks to continuous work of this converter also pulse modulation components in this current are minimized. These benefits are paid for by a relatively small increase in the complexity and the cost of the system. This conception of a converter has been called the double-converter topology (DCT). In the author opinion presented solution of the system can find application in many power electronics equipment and, therefore, will be developed. In the paper DCT basics, simulation experiments, and possible practical arrangement of the DCT are presented.

Key words: controlled source, converter control, converter topology, PWM, simulation model

1. Introduction

Non-linearity of receivers, limited frequency response of power electronics converters, and wide-band nature of signal sampling and pulse modulation processes are reasons of inaccurate mapping a converter's output current in a reference signal. To meet this requirement both, advanced solutions in hardware of converters and substantial modification of their control algorithms are necessary.

A subject of the article is a power electronics voltage controlled current source (VCCS) with a modified topology. This one is based on a two connected in parallel converters. The advantage of this idea is possibility of accurate mapping of the VCCS output current in the reference signal. The main expected application areas of the proposed VCCS solution are:

- power electronics active shunt filters,
- FACTS,
- current modulators,
- Automated Test Equipment (ATE),
- special purpose converters (e.g. equipment for medicine, especially for magnetotherapy).

The study presents the first stage of work on the layout of the current source, which includes, among other items, principles of work of the VCCS and, also, signal, and simulation models of this.

The following text is divided into four sections. The first one deals with a structure and principles of work of the VCCS. The second part presents simulation model researches for the VCCS. In the third part a possible practical implementation of the VCCS is proposed. In the last part conclusions are presented.

2. A double-converter topology basics

A conception of cooperation of a number interconnected converters is widely implemented in real systems, e.g. [2-6, 8]. In particular, this applies to using of two connected in parallel converters, where an output power output of one of them is a fraction of power of a second one. This idea is also presented in many studies e.g. [6, 9, 10]. The common feature of these solutions is that activation of an auxiliary converter (ACN) takes place only in transient states of a main converter (MCN) output current. Usually, the role of an auxiliary converter depends on maximization of a system's dynamics, i.e. extension of its a frequency response. In consequence, a total system output current is better mapped in a reference signal. Unfortunately, a system control algorithms, especially in relation to an ACN, are often defined informally. Because of this potential possibilities of a system are not utilized. The double-converter topology (DCT) conception is also related to a common work of two connected in parallel converters. However, an auxiliary converter operates continuously, not only in system output current transient states. Also, rules of a system work are defined in a formal way.

In the Figure 1 a block diagram of a typical VCCS based on a single converter is shown. The VCCS is an electrical system working in a closed feedback loop. Many factors, e.g. limited frequency response and work of a pulse modulator cause that a receiver current is often poorly mapped in a reference signal. Particularly it takes place when value of a PWM carrier frequency is low what is enforced by demanding of maximization of a converter energy efficiency.

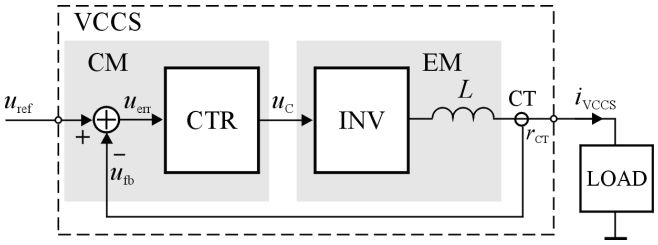

Fig. 1. Block diagram of a typical power electronics controlled current source

A VCCS consists of a control module (CM) and an execution module (EM). A CM includes a signal adder and a controller block (CTR), where a CTR is an output current regulator, while an EM contains: inverter (INV), passive filter (an L inductor), and current trans-

ducer (CT). The VCCS output current i_{VCCS} is related to the error signal $u_{\mathrm{err}} = u_{\mathrm{ref}} - r_{\mathrm{CT}} i_{\mathrm{VCCS}}$ at the input of the CM, where r_{CT} = const. In such a system a value of an error signal (u_{err}) is relatively large.

The general aim of a VCCS operating is fulfilling the following a theoretical formula:

$$i_{\mathrm{VCCS}} = \frac{1}{r_{\mathrm{CT}}}\left(u_{\mathrm{ref}} - u_{\mathrm{err}}\right) \xrightarrow[-\infty<t<\infty]{\forall\ |u_{\mathrm{err}}|\to 0} \frac{1}{r_{\mathrm{CT}}} u_{\mathrm{ref}}\,. \tag{1}$$

Fulfilling the Equation (1) obtains, only theoretically existing, the „ideal case" of a VCCS work. In a real system, even small minimization of an error signal can be a difficult task.

The simplified form of the VCCS, based on proposed the DCT concept, is presented in the Figure 2a. The main converter is supplemented with the auxiliary one. The main converter is high power one but its a frequency response is limited. The auxiliary converter is a low power one but its a frequency response is significantly extended, compared to the main one.

In the simplified of the system form the auxiliary converter is equipped with a transconductance amplifier. This amplifier is preceded by the limiter block (LIM) that clips the ACN control signal. This one imposes a maximal value of an ACN output current ($i_{\mathrm{out,A}}$), therefore a relationship of the ACN and MCN an output power.

In the small-signal model of system (Fig. 2b) the DELAY block is implemented. This one introduces a τ time delay and reflect delays occurring in a real system, mainly being results of: limited value of a signal sampling period, time needed for signal processing, and a non-zero period of a pulse modulation carrier frequency.

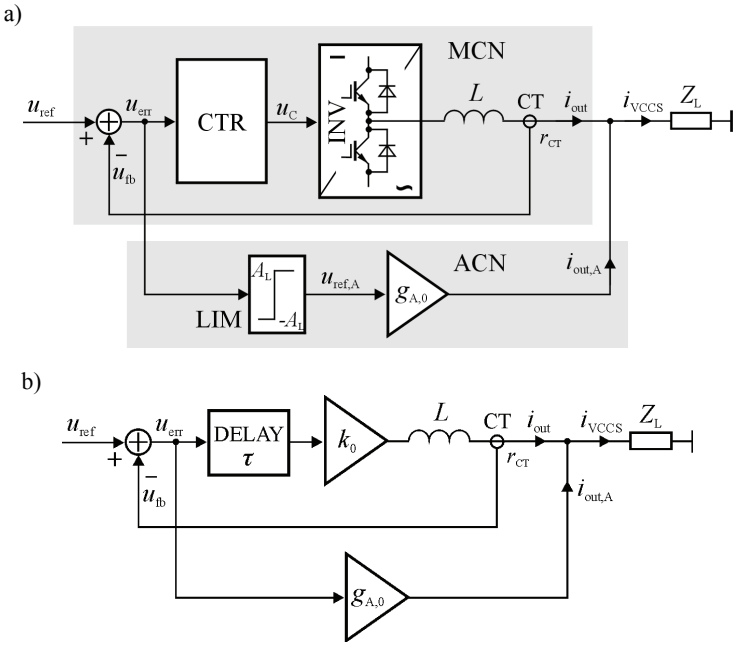

Fig. 2. Block diagram of the VCCS based on the simplified DCT (a) and its the small-signal model (b)

The general formula of the VCCS work is now modified towards the following one:

$$i_{\mathrm{VCCS}} = i_{\mathrm{out}} + i_{\mathrm{out,A}}\,, \tag{2}$$

and, in relationship to the linear model of the system:

$$\begin{gathered} i_{\mathrm{VCCS}} = i_{\mathrm{out}} + i_{\mathrm{out,A}} = i_{\mathrm{out}} + u_{\mathrm{err}} * g_{\mathrm{A}}(t) = i_{\mathrm{out}} + (u_{\mathrm{ref}} - r_{\mathrm{CT}} i_{\mathrm{out}}) * g_{\mathrm{A}}(t) : \\ : R_{\mathrm{L}} = 0, L_{\mathrm{L}} = 0\,, \end{gathered} \tag{3}$$

where $g_{\mathrm{A}}(t)$ is a pulse response of the transconductance amplifier.

Assuming the transfer function of the transconductance amplifier has the 0-order form, i.e. $g_{\mathrm{A}}(t) = g_{0,\mathrm{A}}\delta(t)$, the general equation describing the model work can be obtained:

$$\begin{gathered} i_{\mathrm{VCCS}} = i_{\mathrm{out}} + (u_{\mathrm{ref}} - r_{\mathrm{CT}} i_{\mathrm{out}}) * g_{\mathrm{A},0}\delta(t) = i_{\mathrm{out}} + g_{\mathrm{A},0} u_{\mathrm{ref}} * \delta(t) - g_{\mathrm{A},0} r_{\mathrm{CT}} i_{\mathrm{out}} * \delta(t) = \\ = g_{\mathrm{A},0} u_{\mathrm{ref}} + (1 - g_{\mathrm{A},0} r_{\mathrm{CT}}) i_{\mathrm{out}}\big|_{g_{\mathrm{A},0} r_{\mathrm{CT}} = 1} = g_{\mathrm{A},0} u_{\mathrm{ref}} : |u_{\mathrm{err}}| \subset \langle -A_{\mathrm{L}}, A_{\mathrm{L}} \rangle, \\ R_{\mathrm{L}} = 0, L_{\mathrm{L}} = 0, \end{gathered} \tag{4}$$

where $-A_{\mathrm{L}}$ and A_{L} are LIM block voltage clipping levels.

The Equation (4) indicates that a receiver current can match a reference signal regardless a degree of mapping in a reference signal a main converter output current (i_{out}) – under the condition that the amplitude of ACN control signal is not limited by the LIM block.

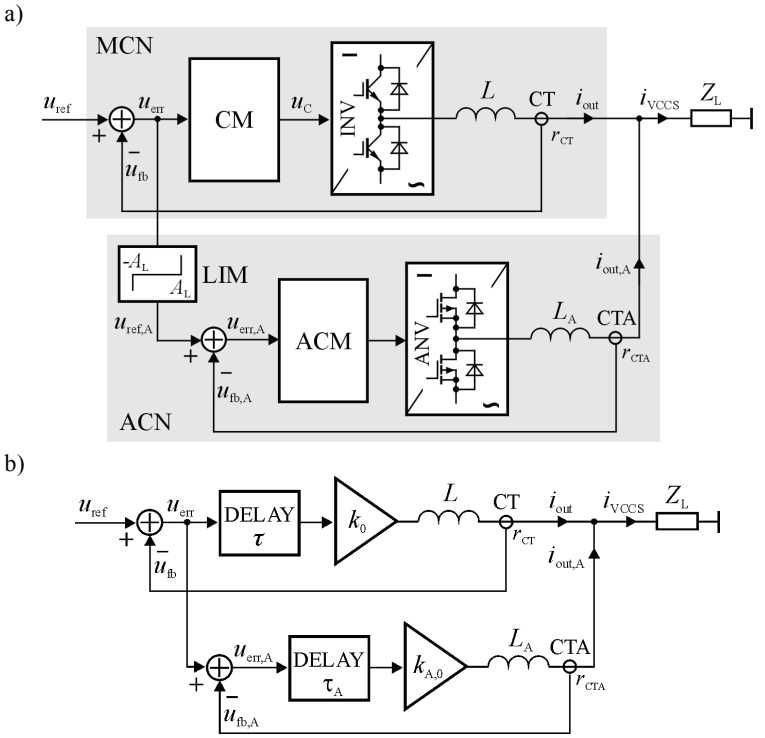

Fig. 3. Block diagram of the VCCS based on the DCT as the real system (a) and its the linear model (b)

In the Figure 3 the block diagram of the real possible arrangement of the VCCS based on the DCT and its the linear model are shown. The linear model has been used for system stability analysis based on the Nyquist criterion.

In a general, structures of both converters are very similar. However, values of parameters of both systems are different. For example, to obtain a sufficient frequency response, a PWM carrier frequency in the ACN needs to be much higher then in the MCN. So, the MCN uses in an execution module (INV) standard IGBT devices, while the ACN should use MOSFET ones. In a real system both converters would be powered from the same DC rails. Thus, nominal voltage of power electronics devices utilized there will be similar, while these devices will be differ in value of nominal output current (and also a cut-off frequencies). A phenomenon that usually occurs in multi-channel converters, in the case of the DCT based system should not occur. This phenomenon is an unbalanced current flow in particular converter channels, e.g. [7, 8]. Due to in the DCT current paths are controlled independently, it is expected that such an undesirable interaction between converters will be negligible.

The model of the VCCS is a Single Input Single Output (SISO) and Linear Time Invariant (LTI) type [5]. This one can be expressed in a frequency domain by the following equation:

$$I_{\mathrm{VCCS}} = U_{\mathrm{REF}} \frac{1}{r_{\mathrm{CT}}} \frac{e^{-j\omega\tau}}{j\omega \dfrac{L}{k_0 r_{\mathrm{CT}}} + e^{-j\omega\tau}} + U_{\mathrm{err}} \frac{1}{r_{\mathrm{CTA}}} \frac{e^{-j\omega\tau_{\mathrm{A}}}}{j\omega \dfrac{L_{\mathrm{A}}}{k_{\mathrm{A},0} r_{\mathrm{CTA}}} + e^{-j\omega\tau_{\mathrm{A}}}}: \quad |u_{\mathrm{err}}| \subset \langle -A_{\mathrm{L}}, A_{\mathrm{L}} \rangle, Z_{\mathrm{L}} = 0, \tag{5}$$

where τ_{A} is the time delay introduced in the linear model of ACN.

Maximal gain values in the controller blocks (k_0 and $k_{\mathrm{A},0}$), due to a system stability behavior, are limited. These are given by following formulas [1]:

$$k_{0,\max} < \frac{\pi}{2} \frac{L}{r_{\mathrm{CT}} \tau}, \tag{6}$$

$$k_{\mathrm{A},0,\max} < \frac{\pi}{2} \frac{L_{\mathrm{A}}}{r_{\mathrm{CTA}} \tau_{\mathrm{A}}}. \tag{7}$$

Respecting Equations (6) and (7), the Equation (5) takes now the following form:

$$I_{\mathrm{VCCS}} = U_{\mathrm{REF}} \frac{1}{r_{\mathrm{CT}}} \frac{1}{j\omega \dfrac{2}{\pi} \tau e^{j\omega\tau} + 1} + U_{\mathrm{err}} \frac{1}{r_{\mathrm{CTA}}} \frac{1}{j\omega \dfrac{2}{\pi} \dfrac{\tau}{p} e^{j\omega \frac{\tau}{p}} + 1}: \quad |u_{\mathrm{err}}| \subset \langle -A_{\mathrm{L}}, A_{\mathrm{L}} \rangle, Z_{\mathrm{L}} = 0, \tag{8}$$

where

$$p = \frac{\tau}{\tau_{\mathrm{A}}}.$$

The Equation (8) expresses the best, for mapping of the VCCS output current in the reference signal, conditions of the system work. Respecting Equations (6) and (7) also occurs:

$$\frac{L_{\mathrm{A}}}{L}=\frac{k_{\mathrm{A},0,\max}}{k_{0,\max}}\frac{r_{\mathrm{CTA}}}{r_{\mathrm{CT}}}\frac{1}{p}. \tag{9}$$

Thus, for the effective of system work following dependencies should take place: $p>>1$ (in other words: $f_{\mathrm{c,A}}>>f_{\mathrm{c}}$, where f_{c} and $f_{\mathrm{c,A}}$ are PWM carrier frequencies in the MCN and the ACN respectively) and $L_{\mathrm{A}}<<L$. In the result, the following relationship can be satisfied:

$$\forall_{-\infty<t<\infty}\ |u_{\mathrm{err,A}}|<<|u_{\mathrm{err}}|. \tag{10}$$

Quality of the VCCS output current can be evaluated on the base of a control error value. This one is defined by the formula:

$$\varepsilon=\sqrt{\frac{\overline{|\Delta u|^2}}{\overline{|u_{\mathrm{ref}}|^2}}}100\%, \tag{11}$$

where, in respect to the MCN: $\varepsilon=\varepsilon_{\mathrm{M}}$ and $\Delta u=u_{\mathrm{err}}$, while, in respect to the VCCS: $\varepsilon=\varepsilon_{\mathrm{VCCS}}$ and $\Delta u=u_{\mathrm{ref}}-\left(r_{\mathrm{CT}}i_{\mathrm{out}}+r_{\mathrm{CTA}}i_{\mathrm{out,A}}\right)$. The signal integration period for calculating its a RMS value is equal to the reference one (T_{ref}).

By fulfilling Equations (6) and (7) the ACN frequency response is p-times extended, compared to the MCN one. Hence, a dominant effect on the quality of the VCCS output current is set in both, the $f_{\mathrm{c,A}}$ value and u_{err} signal clipping levels ($\pm A_{\mathrm{L}}$).

3. Simulation experiments

For checking theoretical assumptions a simulation model of the DCT based the VCCS with use of the OrCAD/PSpice tool has been investigated. The model have consisted of the following elements: reference signal generator, main and auxiliary converters, power supply, and load (Fig. 4). Ready to use models of power electronics devices that are implemented in OrCAD/PSpice have been modified towards real devices. These ones are mentioned in the section 4. Basic electrical parameters of the VCCS simulation model have been as follows:

- converters DC link voltage: 560 V,
- PWM carrier frequency: f_{c} = 10 kHz, and $f_{\mathrm{c,A}}$ = 200 kHz,
- gain factor: k_0 = 190 V/V, and $k_{\mathrm{A},0}$ = 1150 V/V,
- converter output inductance: L = 5 mH, and L_{A} = 1.5 mH,
- nominal amplitude of the VCCS output current: $A_{\mathrm{VCCS,n}}$ = 20 A,
- maximal amplitude of the ACN output current: $A_{\mathrm{ACN,max}}$ = 4 A,
- load: $R_{\mathrm{L}}=0\div1\ \Omega$, $L_{\mathrm{L}}=0\div100\ \mu$H.

Values of gain factors have been very close to maximal ones. Due to imposed values of voltage clipping levels in the limiter block, the nominal output power of the ACN has been equal to 20% of the VCCS one.

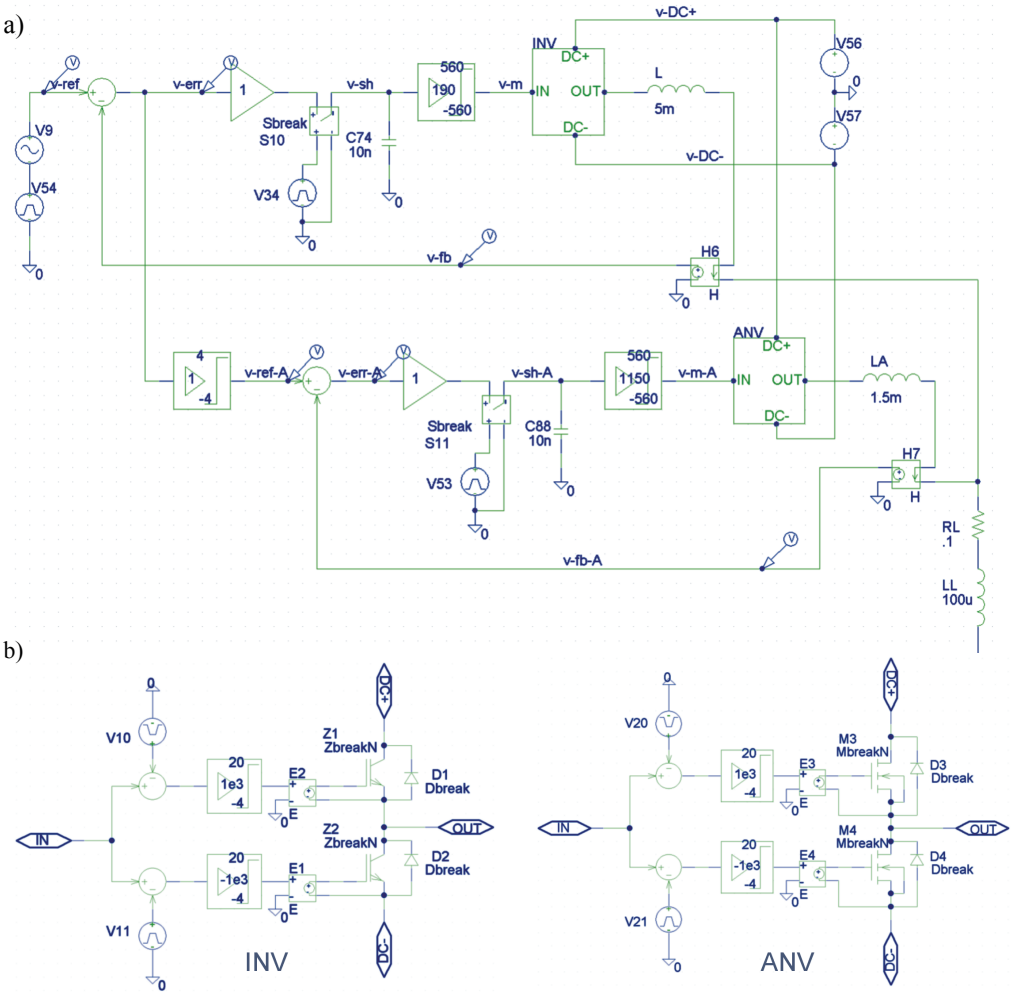

Fig. 4. DCT simulation model: a) general view, b) INV and ANV blocks

For evaluation of the simulation model properties different reference signals has been used. Selected waveforms of these are shown in the Figures 5 and 6.

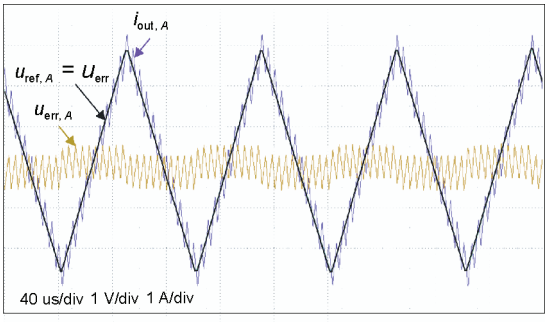

Fig. 5. Signal waveforms in the ACN: reference signal (MCN error signal), output current, and error signal

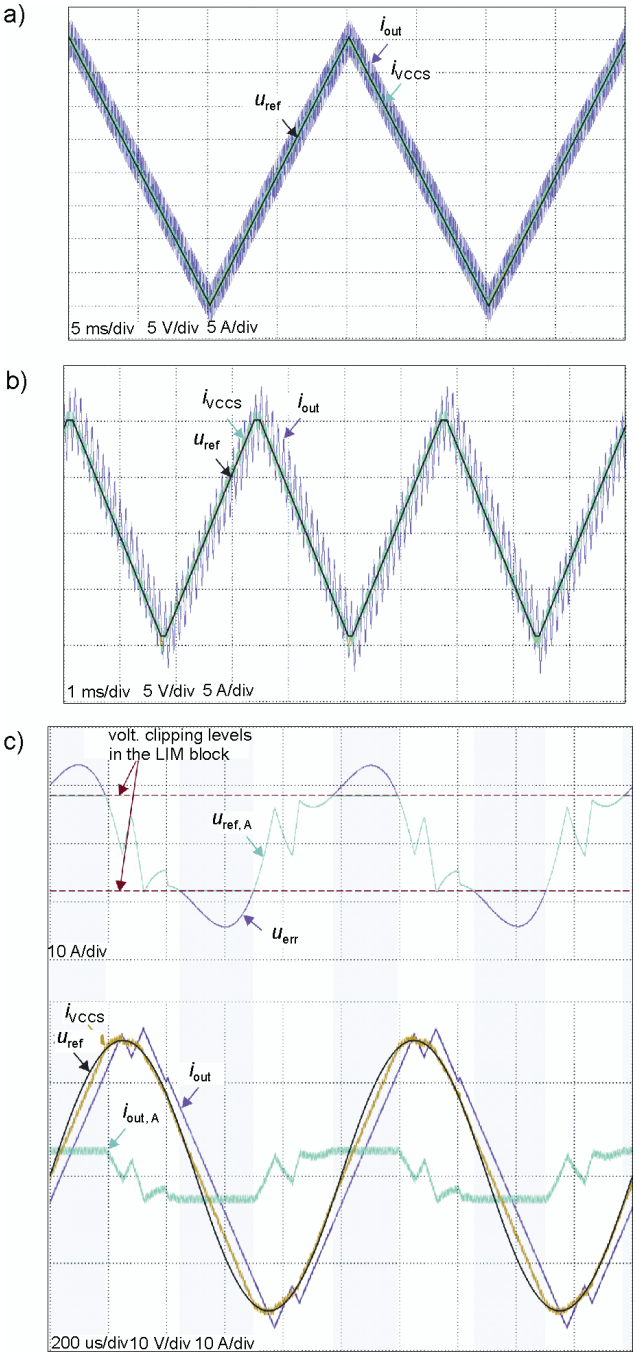

Fig. 6. Waveforms in the simulation model of the VCCS for different parameters of the reference signal: a) reference signal is the triangular one, f_{ref} = 50 Hz, and A_{ref} = $A_{ref,\,n}$ = 20 V, b) reference is the triangular one, f_{ref} = 300 Hz, and A_{ref} = 0.5 $A_{ref,\,n}$ =10 V, and c) reference is the sinusoidal one, f_{ref} = 1000 Hz, and $A_{ref,}$ = $A_{ref,\,n}$ =15 V

Shown in the Figure 5 the error voltage (u_{err}) is just a result of PWM caused ripples in the MCN output current. As can be observed, the limited gain factor ($k_{\mathrm{A},0,\max}$) in the ACN control circuit not allows for exact mapping (omitting ACN own PWM ripples) of the ACN output current in the reference signal. So, the error signal ($u_{\mathrm{err,A}}$) is relatively large.

Analysis of control error values points at the significant operating efficiency of auxiliary converter, regardless of reference voltage parameters. E.g. for the case of reference shown in the Figure 6a these values have been as follows: ε_{M} = 13.9%, and $\varepsilon_{\mathrm{VCCS}}$ = 2.9%. In any analyzed case of reference, a value of $\varepsilon_{\mathrm{VCCS}}$ has been $4 \div 5$ times lower than ε_{M}. Also, undesired, from the point of view of the output current quality, interactions between both of converters have been negligible.

In the Figure 6c an affect of clipping of u_{err} signal on inaccurate mapping of VCCS output current in the reference is presented. This process is marked with the gray background.

4. Practical implementation of the VCCS

The control module of proposed VCCS needs high computation power. It results from high a signal sampling rate (as high as hundreds of kHz), due to demanded the ACN parameters. In the case of a DSP based control module the Analog Devices 4th-generation of 32-bit floating point processors SHARC® family ADSP-214XX could be the good choice. This family is especially dedicated applications in advanced power electronics converters. These processors are characterized by precision mathematic (ALUs and MACs) units on-chip, substantial computation power (up to 2700 MFLOPS), and useful hardware, e.g. the high performance 16-channel PWM unit. This unit, when configured in a typical for power electronics application the paired channel mode, is able to control up to 8 of inverter legs. Another possibility is utilization in a control circuitry e.g. of TEXAS INSTRUMENT Tiva™ C Series MCUs.

In the execution part of the main converter IGBT/IPMs could be used. Good choice seems the L1 series 1200 V [11] family of IPMs, manufactured by MITSUBISHI ELECTRIC. In the auxiliary converter the 800 V CoolMOS™ power MOSFETS [12] from INFINEON could be utilized. Models of these just devices have been used in simulation experiments.

An interesting alternative for silicon based devices is utilization in the ACN Silicon-Carbide (SiC) MOSFETs, e.g. Z-FET® series from CREE [13]. In the result the PWM carrier frequency could be further increased.

5. Conclusions

The power electronics controlled current source based on the proposed double-converter topology is characterized by a much better mapping of its an output current in a reference signal, compared to a typical converter solution. Thanks to the operation of the auxiliary converter in a continuous manner, even components of pulse modulation in this current can be minimized. Therefore, energy transmission losses can be lowered and a converter can easier

meet EMC requirements. These benefits are paid for by a relatively small increase in the system complexity (and the system cost).

In the author opinion presented solution of the power electronics system can find application in many power electronics equipment. Thus, it will be developed towards e.g. controlled voltage sources and equipment based on multi-channel (interleaved) converters topology.

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