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jet INTL JOURNAL OF ELECTRONICS AND TELECOMMUNICATIONS, 2014, VOL. 60, NO. 1, PP. 109–115
Manuscript received November 12, 2013; revised February, 2014. DOI: 10.2478/eletel-2014-0013

Design of an Ultra-Low Power CT ΣΔ A/D Modulator in 65 nm CMOS for Cardiac Pacemakers: From System Synthesis to Circuit Implementation

Yelin Wang and Hao Cai

***Abstract*—A high performance, ultra-low power, fully differential 2^{nd}-order continuous-time ΣΔ analogue-to-digital modulator for cardiac pacemakers is presented in this paper. The entire design procedure is described in detail from the high-level system synthesis in both discrete and continuous-time domain, to the low-level circuit implementation of key functional blocks of the modulator. The power consumption of the designed modulator is rated at 182 nA from a 1.2 V power supply, meeting the ultra-low power requirement of the cardiac pacemaker applications. A 65 nm CMOS technology is employed to implement the ΣΔ modulator. The modulator achieves a simulated SNR of 53.8 dB over a 400 Hz signal bandwidth, with 32 KHz sampling frequency and an oversampling ratio of 40. The active area of the modulator is $0.45 \times 0.50\, mm^2$.**

***Keywords*—cardiac pacemaker, CMOS, ultra-low power, analogue-to-digital, Sigma-Delta modulation, continuous-time**

I. Introduction

As the industry of the medical implantable devices develops, lowering power consumption as much as possible is essential in improving the service time of battery, which cannot be replaced frequently. Implantable cardiac pacemaker using transistors were introduced in the 1950s, which is used to treat bradyarrhythmia [1]. The pacemaker detects the natural heart beat of the patient. If the detected heart beat gets lower than the default pace, the pacemaker then produces electrical stimulus and recovers the default pace. The service time of a common pacemaker is about five to ten years nowadays [2]. To make a pacemaker stay active as long as possible, low-power high-performance designs of the internal ICs are highly required.

A sensing unit is essential in a cardiac pacemaker. It monitors the natural activities of the heart and converts the detected electrical (analog) signals to digital quantities, which are then further processed by a digital-signal-processing (DSP) unit followed. Converting the analog signals to digital quantities helps precise signal processing and is accomplished with a low-power analog-to-digital converter (ADC). The continuous-time (CT) Sigma-Delta (ΣΔ) modulator is a good candidate for low-power ADCs design [3]–[8]. Figure 1 shows a basic CT ΣΔ modulator. In CT ΣΔ modulation, the spectrum of the noise is shaped by noise shaping capability achieved through the feedback path. As a result, the in-band noise is significantly decreased as most of it is shifted towards high frequencies. In this way, a relatively high in-band signal-to-noise ratio (SNR) can be achieved. Another advantage of the CT ΣΔ modulation lies in the fact that CT structure possesses good quality of inherent anti-aliasing, which simplifies the system design by eliminating the need for the anti-aliasing filter. In turn, power consumption introduced by the anti-aliasing filter is avoided [4]. In addition, for CT structure sampling of the analogue signal happens at the output of the loop filter so that the error introduced by imperfections of the sampling process can be largely suppressed by noise shaping.

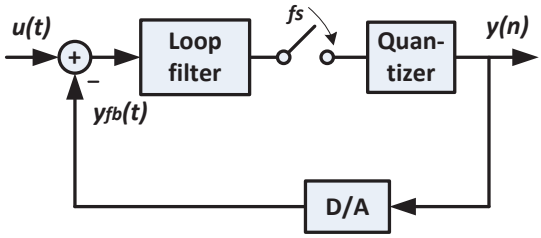

Fig. 1. Block diagram of continuous-time delta-sigma modulator system.

In this work, a fully differential 2^{nd}-order CT ΣΔ modulator is designed. From simulation, 53.8 dB SNR is achieved over 400 Hz bandwidth under a low oversampling ratio (OSR) of 40. The power consumption is only 182 nA with 1.2 V supply voltage. The modulator is designed using the classic Boser-Wooley structure, which is rather simple and straightforward, and belongs to the Cascade of Integrators with Distributed Feedback and Coupling (CIFB) architecture [3], [9]. Active RC integrators are employed to make the 2^{nd}-order loop filter because of their simplicity and good linearity. Return-to-Zero (RZ) feedback waveform is realized by a switch-based digital-to-analogue converter (DAC) in order to reduce the effect of excess loop delay. A discrete-time (DT) ΣΔ modulator is first synthesized in MATLAB and then converted to the CT equivalent using Verilog-A models. Optimal design parameters are obtained through simulations on the Verilog-A CT system. Finally, the CT ΣΔ modulator is implemented using a 65 nm CMOS process in Cadence design tools. The paper is organized as follows. Section II describes the high-level design including system synthesis and DT to CT modulator conversion and other issues. In Section III, low-level circuit design of each blocks in the CT ΣΔ modulator is illustrated and discussed. Post-layout simulation result is shown in Section IV, followed by conclusions in Section V.

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II. High-Level System Synthesis

The basic concepts and methodologies for system synthesis of DT and CT ΣΔ modulators are elaborated in this section. Optimal design parameters, such as gain and bandwidth of the integrator operational amplifiers, are acquired by system simulations, providing essential guidance for circuit implementation.

A. DT ΣΔ Modulator Synthesis

A ΣΔ A/D modulator shown in Fig. 1 can be modelled by a composition of signal transfer function (STF) and noise transfer function (NTF). Assume that the transfer function of the loop filter is represented as $G(z)$, the STF and NTF can be written as:

$$STF(z) = \frac{G(z)}{1+G(z)} \tag{1}$$

$$NTF(z) = \frac{1}{1+G(z)} \tag{2}$$

and the modulator can be represented by:

$$Y(z) = STF(z)U(z) + NTF(z)E(z) \tag{3}$$

where $Y(z)$, $U(z)$ and $E(z)$ are the modulator output, input and the quantisation noise, respectively.

As the first step in the design of a ΣΔ modulator, the NTF needs to be determined. Since the Boser-Wooley structure is used in the design, the NTF of the system in DT domain is described as [9]:

$$NTF = (1-z^{-1})^2 \tag{4}$$

The NTF can be easily synthesized using the Delta-Sigma Toolbox, and the feed-forward and feedback coefficients are determined by the toolbox as well [3]. Figure 2a shows the synthesised DT ΣΔ modulator. The loop filter is composed of two cascaded integrators, followed by a single bit quantizer. The feedback DAC generates the required feedback waveform. The purpose of synthesizing the DT ΣΔ modulator is to figure out values of the coefficients in the system. With these coefficients the conversion from DT to CT system can be performed. The coefficients are illustrated in Fig. 2a and their values are as follows: $a_{1,DT} = -1$, $a_{2,DT} = -2$, $b_{DT} = 1$, $c_{DT} = 1$. Figure 3 plots the simulated SQNR as a function of the amplitude of input sinusoidal signal in dB_{FS}. The frequency of the input signal is at 401 Hz, and the OSR is equal to 40 (sampling frequency is 32 kHz). From the curve it can be observed that the peak SQNR of 61.6 dB is obtained when the amplitude of the input signal is around -6 dB_{FS}.

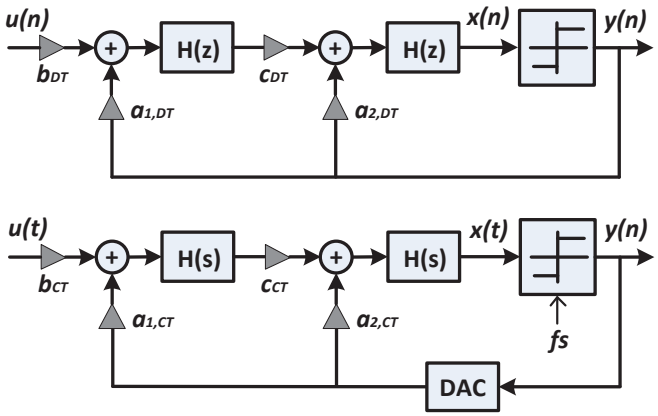

Fig. 2. (a) Block diagram of the synthesized 2^{nd}-order DT ΣΔ modulator, $H(z) = \frac{z^{-1}}{1-z^{-1}}$; (b) the CT equivelant, $H(s) = \frac{f_S}{s}$.

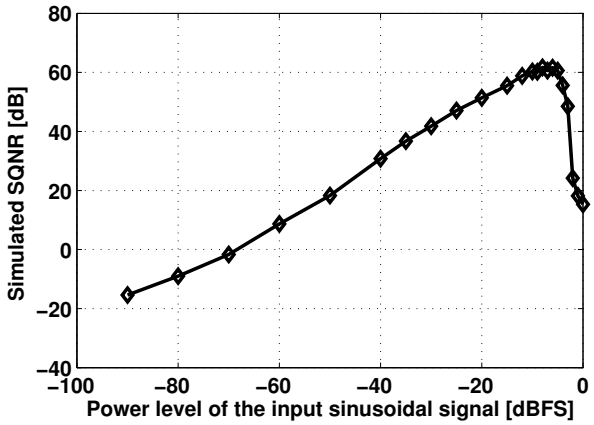

Fig. 3. Simulated SQNR versus the amplitude of the input sinusoidal signal of the synthesised DT ΣΔ modulator system.

B. Return-to-Zero Feedback Waveform

Before converting the DT system to its CT equivalent, the shape of the feedback waveform (the output of the feedback DAC) needs to be determined first, since the scheme of the conversion depends on it. Two types of feedback waveforms are commonly used in ΣΔ modulation: non-return-to-zero (NRZ) and return-to-zero (RZ), as described in Fig. 4. The main difference between the two types lies in whether the same status (i.e., digital "0" or "1") lasts an entire clock period or not. Take the first clock period in Fig. 4 for an example. In NRZ type, status "1" holds on for the whole clock period [0, T_S]; but in RZ type, status "1" holds on only for part of the clock period [$\alpha \cdot T_S, \beta \cdot T_S$], where $\alpha, \beta \in (0, 1)$, and returns to the "reset" or "common-mode" status in the period [0, $\alpha \cdot T_S$] and [$\beta \cdot T_S$, T_S].

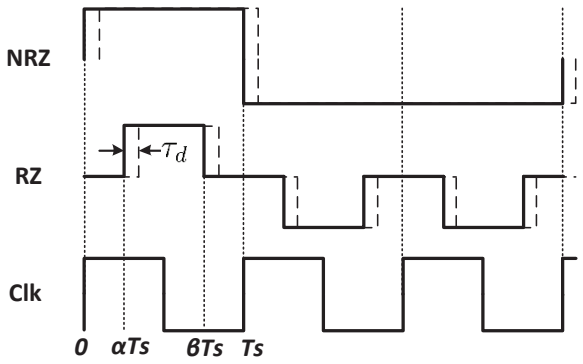

Fig. 4. NRZ and RZ feedback waveforms used in ΣΔ modulator system.

One main concern when choosing the type of feedback waveform is the effect of excess loop delay, which arises from the propagation time and status settling time in quantizer, latches, flip-flops and DAC included in the system. As illustrated by the dashed waveforms in Fig. 4, with an excess loop delay time of τ_d, the desired waveforms are shifted by the delay to be within $[\tau_d, T_S + \tau_d]$ for NRZ case and $[\alpha \cdot T_S + \tau_d, \beta \cdot T_S + \tau_d]$ for RZ case. The start and stop time instants of the feedback waveform are key parameters to figure out the new system coefficients during the DT-to-CT conversion. Shift in the time instants means mismatch occurs between the system coefficients and the real behaviour, which causes degradation in the dynamic performance. Figure 5 shows the simulation results of SNR versus excess loop delay τ_d for both NRZ and RZ ΣΔ modulators (for RZ case, $\alpha = 0.25$, $\beta = 0.75$). It can be observed that the RZ system has much better tolerance to excess loop delay than the NRZ system in terms of dynamic performance: For RZ system less than 1 dB degradation on SNR is observed when τ_d equals to $0.25{\cdot}T_S$; while for NRZ case the dynamic performance is deteriorated by more than 8 dB at the same τ_d. For the system to be more robust against excess loop delay, RZ feedback scheme is chosen in this work.

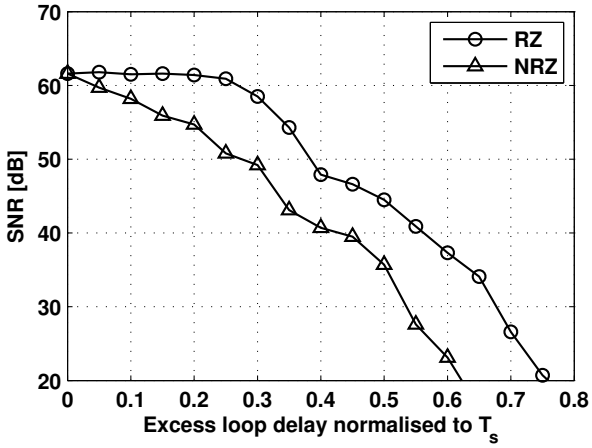

Fig. 5. Effect of excess loop delay on the dynamic performance of the ΣΔ modulator system.

C. DT-to-CT System Conversion

Among many methods to perform DT-to-CT system conversion, the *impulse-invariant transformation* is chosen [4]. To ensure the DT ΣΔ modulator and its CT counterpart functioning in the same way, at every sampling instant the input signals to the quantizers in DT and CT systems should be equal to each other. This can be represented by:

$$x(n) = x(t)|_{t=n\cdot T_S} \tag{5}$$

where $x(n)$ and $x(t)$ represent the inputs to the quantizers in the DT and CT ΣΔ modulators, respectively (as seen in Fig. 2). To make this condition always fulfilled, the transfer functions (TF) from the modulator output $y(n)$ to the quantizer input ($x(n)$ and $x(t)$) must be the same for DT and CT systems, which is illustrated by:

$$TF(z) = a_{1,DT} \cdot H^2(z) + a_{2,DT} \cdot H(z) \tag{6a}$$

$$TF(s) = a_{1,CT} \cdot H^2(s) + a_{2,CT} \cdot H(s) \tag{6b}$$

$$TF(z)|_{Z\Rightarrow S} \equiv TF(s) \tag{6c}$$

By following the Z-to-S domain transformation and mathematical deduction described in [4], the relationship between the system coefficients of DT and CT ΣΔ modulators can be obtained:

$$a_{1,CT} = \frac{1}{\beta - \alpha} \cdot a_{1,DT} \tag{7}$$

$$a_{2,CT} = \frac{1}{2} \cdot \frac{\alpha + \beta - 2}{\beta - \alpha} \cdot a_{1,DT} + \frac{1}{\beta - \alpha} \cdot a_{2,DT} \tag{8}$$

$$b_{CT} = b_{DT} \tag{9}$$

$$c_{CT} = c_{DT} \tag{10}$$

where $\alpha = 0.25$ and $\beta = 0.75$ represent the start and stop time instants of the RZ feedback waveform as described previously. From the DT system synthesis, values of the coefficients are obtained: $a_{1,DT} = -1$, $a_{2,DT} = -2$, $b_{DT} = 1, c_{DT} = 1$, which results in the values of the coefficients in the CT equivalent: $a_{1,CT} = -2$, $a_{2,CT} = -3$, $b_{CT} = 1$, $c_{CT} = 1$. However, these coefficients cannot be directly used in the design since they are unscaled. Coefficient scaling is essential to properly limit the inner states of the modulator, i.e., outputs of the two integrators, which ensures that the integrators remain in their linear region all the time and the quantizer is never overloaded as well. For this work, the scaling factors are chosen as $k_1 = 8$ and $k_2 = 16$, resulting the scaled system coefficients for CT ΣΔ modulator, $a_{1,CT,S} = -0.25$, $a_{2,CT,S} = -0.1875$, $b_{CT,S} = 0.125$, $c_{CT,S} = 0.5$, where the concept and calculation are illustrated in Fig. 6. Take the first integrator (more close to the input) of the system as an example. $a_{1,CT}$ and b_{CT} are a pair of corresponding coefficients to the first integrator. To scale them down, both are divided by the scaling factor k_1 (= 8), resulting $a_{1,CT,S}$ and $b_{CT,S}$. At the output of the first integrator, the output coefficient c_{CT} (which is also the feedforward input coefficient to the second integrator) is multiplied by k_1 to compensate the decrease in the output due to the scaling at the input. The same concept is applied to scale the coefficients for the second integrator.

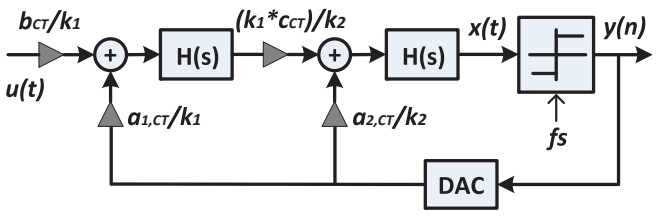

Fig. 6. Block diagram of the synthesized 2^{nd}-order CT ΣΔ modulator with scaled system coefficients.

D. CT ΣΔ Modulator Synthesis and Simulation

Figure 7 illustrates the schematic of the synthesized CT modulator. The loop filter contains two cascaded active RC-integrators. Values of the passive components can be figured out from the system coefficients obtained previously. The integrator op-amps are modelled as a function of the unity-gain bandwidth (GBW) and DC gain (A_{DC}), represented as a composition of a RC network and a voltage-controlled-voltage-source (VCVS). The comparator and DAC are modelled as ideal functional blocks using Verilog-A.

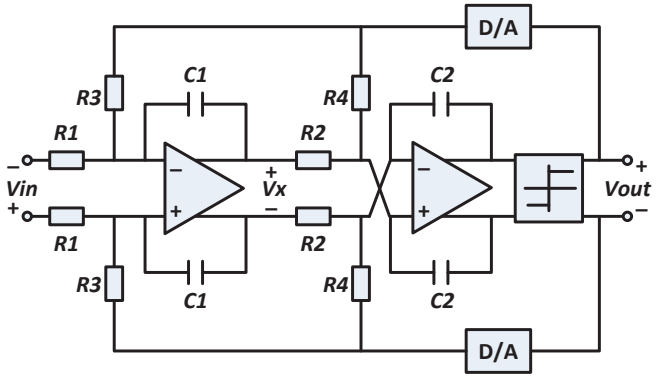

Fig. 7. Schematic of the synthesized CT ΣΔ modulator.

System simulations are performed to determine the values of A_{DC} and GBW which will be used as the design targets when implementing the op-amps in hardware afterwards. To determine A_{DC}, GBW is set closed to 'infinity' to isolate its effect on the dynamic performance of the system. Table I lists the simulated SNR of the synthesized CT system under different A_{DC} of the op-amps. It can be observed that the SNR does not degrade obviously until A_{DC} decreases under, i.e., 40 in our case. Figure 8 shows more simulation results on the issue. SNR versus OSR with different A_{DC} are plotted. It can be observed that for low to medium OSR (i.e.,OSR$\leq$50) the dynamic performance will not degrade significantly as long as A_{DC} is in the same order as/comparable to the OSR of the system. From this perspective, it is chosen that A_{DC} is targeted

TABLE I
SNR OF THE SYSTEM WITH DIFFERENT OP-AMP A_{DC}

A_{DC} (liner scale)	SNR (dB)
20	56.5
40	59.3
60	60.1
80	60.6
100	61.0

TABLE II
SNR OF THE SYSTEM WITH DIFFERENT OP-AMP GBW

GBW (Hz)	SNR (dB)
$2\times f_S$	55.3
$3\times f_S$	58.2
$4\times f_S$	59.1
$5\times f_S$	60.3

in the range of 40-60 for later circuit design, considering the trade-off between the power consumption and the performance of the op-amp.

Similar simulations are performed in order to determine the target GBW of the op-amp. Table II lists the simulated SNR under different GBW values, which are represented as multiples of the sampling frequency f_S ($f_S = 32\,kHz$). It can be seen that the dynamic performance of the system has little improvement with GBW increasing from 3 to 5 times of f_S (and higher multiples). Considering the requirement of low power consumption, GBW between 3 to 4 times of f_S is determined as the design target in later circuit implementation.

Finally, system simulation is performed with the selected values of A_{DC} and GBW, which provides an initial figure of how much SNR can be obtained. Figure 9 plots the simulated output spectrum of the synthesised CT ΣΔ modulator with op-amp A_{DC} and GBW of 40 and $3\times f_S$ (96 kHz), respectively. A SNR of 56.2 dB is achieved under a sinusoidal input signal with 401 Hz frequency and -6 dB_{FS} power level. Figure 9 plots also the simulated output spectrum of an ideal system, where the op-amp A_{DC} and GBW are set to be 'infinity'. Degradation in the dynamic performance can be observed and the SNR is deteriorated with approximately 5.4 dB.

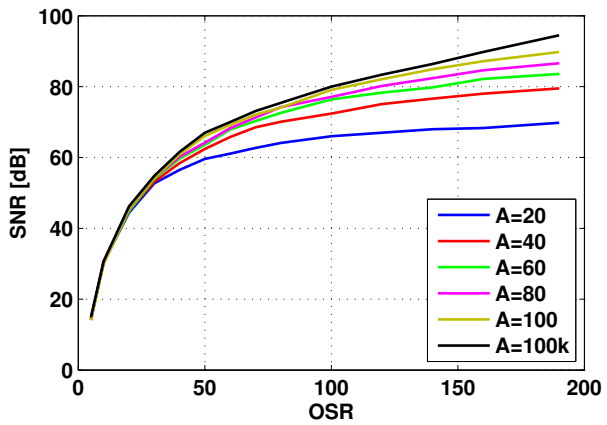

Fig. 8. Simulated SNR versus OSR with different A_{DC} of the CT ΣΔ modulator.

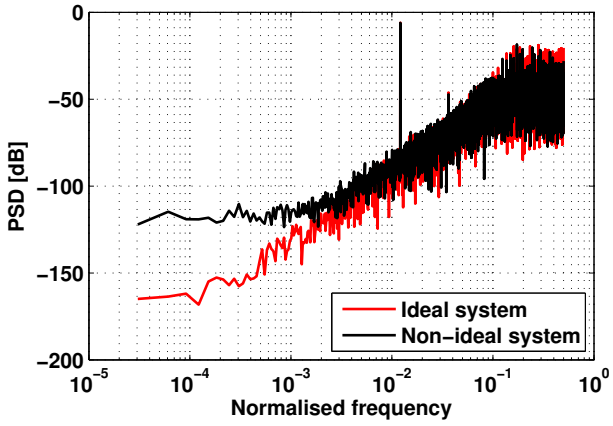

Fig. 9. Simulated output spectrum of the CT ΣΔ modulator system with non-ideal and ideal op-amps in the loop filter.

III. Low-Level Circuits Implementation

From system synthesis and simulation, a 2^{nd}-order 1-bit (quantizer) CT ΣΔ modulator is realised with 56.2 dB SNR with the integrator op-amps having 40 A_{DC} and $3\times f_S$ (96 kHz) GBW. In this section, transistor level implementation of some key functional blocks is described in detail.

A. Op-Amps in the Loop Filter

Low power consumption is the most important design target so that simple one-stage op-amps are preferable. For this work, the classic folded-cascode structure is chosen. Figure 10 shows the schematic of the designed fully differential folded-cascode op-amp. The negative and positive output nodes are connected back to the gates of transistors $M3b$ and $M4b$, providing the common-mode feedback (CMFB) path which defines the output CM level for the op-amp. This simple CMFB topology does not require any extra circuit branch that consumes current, which matches well the low power consumption requirement of the system.

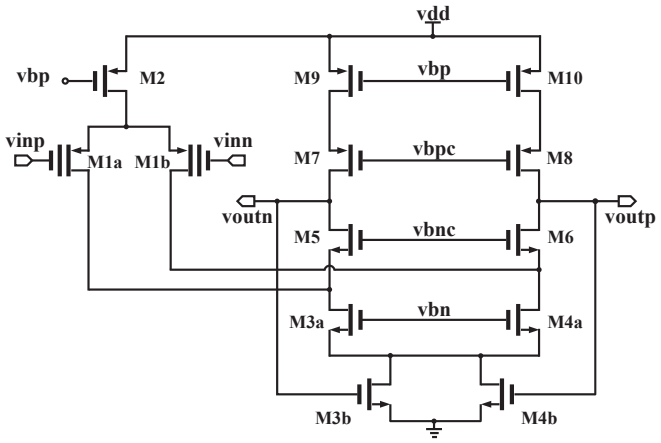

Fig. 10. Schematic of the designed folded-cascode op-amp.

Due to the ultra-low power consumption requirement, all the transistors are biased in the deep weak-inversion region, where the gate-source voltage is smaller than the threshold voltage [10]. For this work, the transistors work with ultra-low currents of magnitude of nA in the weak-inversion region. The CM input and output voltage are set to 600 mV, which is half of the supply voltage, to ensure that maximum voltage swing can be obtained at both input and output. Thick-gate transistors (which have higher threshold voltage) are used for the input differential pair $M1a$ and $M1b$, to improve the input voltage swing. The transconductance g_m of the input differential pair can be approximated based on the target GBW (3 to 4 times of f_S) decided from the system design in the previous section. In the final design, simulation shows that A_{DC} of 46 in linear scale and GBW of 100 kHz (a bit larger than $3 \times f_S$) are achieved with about 90 nA overall current consumption. Recalling the target A_{DC} of between 40 to 60 and GBW of between 3 to 4 times of f_S, the designed op-amp fulfils the targets quite well with a reasonably low power consumption.

B. Comparator as the Single-Bit Quantizer

A comparator is always employed as the internal single-bit quantizer in ΣΔ modulator design. Dynamic comparator is preferable because of its low power consumption attributed to its periodic operation. In this study, a modified Lewis-Gray dynamic comparator without pre-amplifier is designed using minimum size devices, as shown in Fig. 11 [11]. Operation principle of the comparator is described as follows. When Clk signal is low, the comparator operates in reset mode. $M3$ and $M4$ are cut off so that there is no current path existing between the supply voltage vdd and ground. $M9$ and $M10$ pull both outputs to vdd by charging the capacitance at the output node; meanwhile $M7$ and $M8$ are cut off and $M5$ and $M6$ start to conduct. When the comparator is latched by Clk signal, it works in regeneration mode. $M3$ and $M4$ immediately conduct at Clk low-to-high edge. Both output nodes $voutp$ and $voutn$ start to be discharged. If the current flowing in the left branch is larger than that in the right, $voutn$ is discharged to 0 V firstly and at the same time $M6$ is cut off and $M8$ starts to conduct, which pulls $voutp$ to vdd. In this way, the differential outputs are generated.

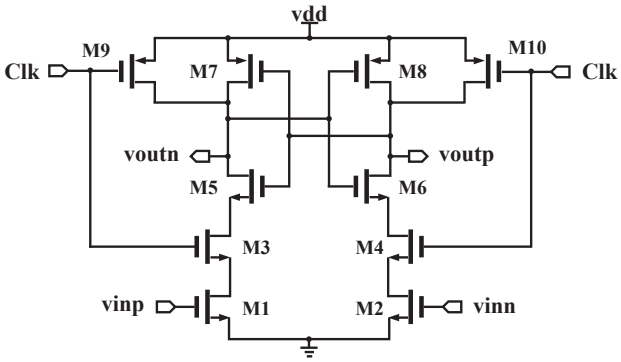

Fig. 11. Schematic of the designed dynamic comparator.

The decision time of the comparator needs to be considered, since it contributes to the excess loop delay which degrades SNR of the system as discussed previously. In Fig. 5 it has shown that for our system where the RZ waveform is used, less than 1 dB degradation on SNR occurs when τ_d equals to $0.25{\cdot}T_S$, namely, about 7.81 μS. The delay of the designed comparator is in the magnitude of tens of nS. Negligible effect will be made by the comparator on the overall dynamic performance of the system.

C. DAC in the Feedback Path

The feedback DAC is designed simply as a combination of several switches realised by transmission gates, as shown in Fig. 12. The outputs V_{outp} and V_{outn} are connected to the feedback resistors, which are not included in the figure for simplicity. Clk_p and Clk_n are generated by the preceding logic and control the state of the differential output, which is either V_{refp}-V_{refn} or inversely. Reset 'high' shorts two output nodes, making the outputs return to CM voltage of the system. In order to completely avoid the situation of short circuit, namely, all switches are closed during a certain period due to the overlap between clock signals, non-overlapping clocking

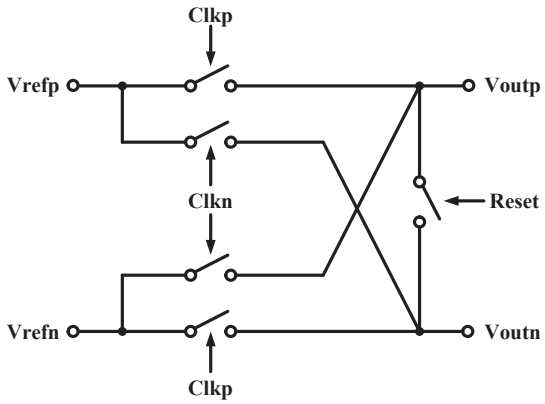

Fig. 12. Simplified symbol view of the designed DAC.

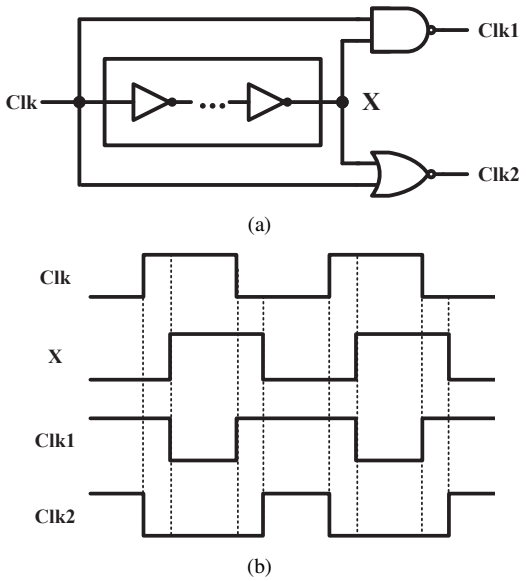

Fig. 13. Non-overlapping clocking scheme used in the DAC, (a) Symbol view of the logic employed; (b) An example of the generated non-overlapping signals, $Clk1$ and $Clk2$.

is employed. Figure 13 illustrates the scheme used in the work to generate the non-overlapping clock signals and an example of the generated signals.

IV. Post Layout Simulation Results

Figure 14 shows the layout of the designed CT ΣΔ A/D modulator with the clock generator included. It occupies an active area of $0.45 \times 0.50\, mm^2$, of which the majority area is used by resistance and capacitance in the modulator due to the low clock frequency (32 kHz) of the system. Common-centroid layout technique is used for transistors and passive elements as well to achieve good matching between critical elements. Post-layout simulation is performed and an SNR of 53.8 dB to the maximum has been achieved. There is slight degradation on the dynamic performance compared to the synthesised CT system, where a maximum SNR of 56.2 dB is achieved. This degradation is mainly due to the non-linearity of the large resistance used (in the magnitude of tens of MΩ) in the layout. Figure 15 plots the simulated SNR as

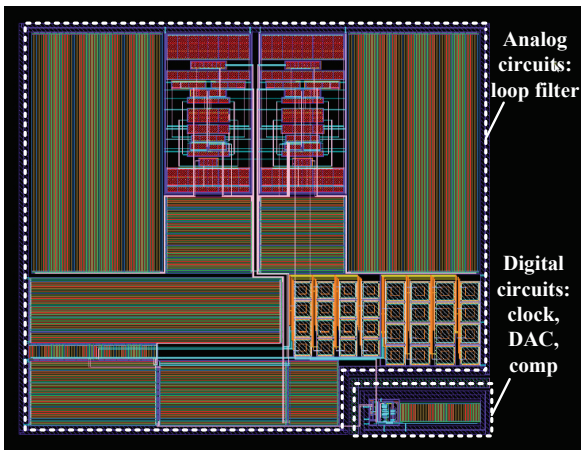

Fig. 14. Layout of the designed CT ΣΔ A/D modulator.

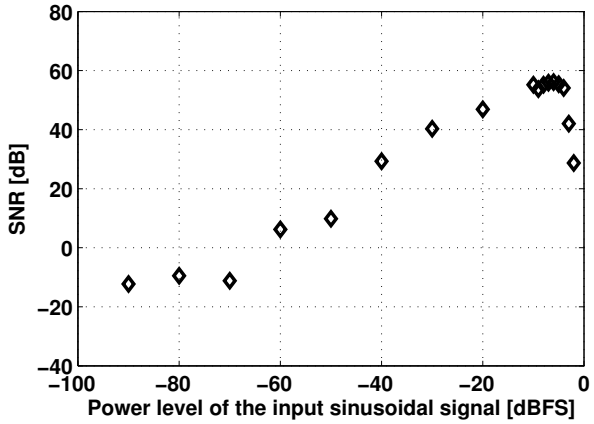

Fig. 15. Post-layout simulated SNR versus the power level of the input sinusoidal signal.

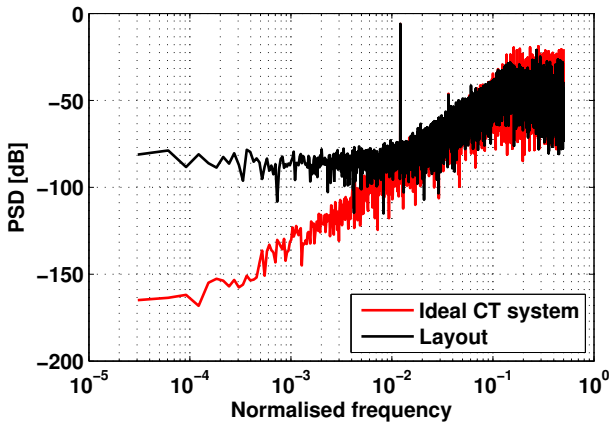

Fig. 16. Post-layout simulated output spectrum of the designed CT ΣΔ A/D modulator.

a function of the power level of the input sinusoidal signal with a frequency of 401 Hz. The maximum SNR is observed around -6dB_{FS} power level of the input signal. The simulated output spectrum that gives the best SNR is plotted in Fig. 16. The corresponding simulated output spectrum of the ideal CT ΣΔ A/D modulator (synthesised previously) is also plotted in

TABLE III
PERFORMANCE COMPARISON OF LOW POWER ADCS DESIGN

Refs.	Architecture	Process	BW [Hz]	Sampling rate [Hz]	V_{DD} [V]	ENOB [bits]	Power [nW]	FOM [pJ/conv.]	Area [mm^2]
[12]	SAR	0.14 μm	-	3.125 k	1.2	12	850	0.066	0.35
[13]	SAR	0.18 μm	20 k	80 k	1.0	8.0	400	0.0195	0.12
[14]	SAR	0.13 μm	-	1 k	1.0	9.1	53	0.0945	0.19
[15]	SAR	0.18 μm	-	17.8 k	1.2	5.2	162.5	2.2	-
[7]	CT ΣΔ	0.35 μm	25 k	3.2 M	3.0	9.04	4350	0.267	0.0138
[16]	SAR	0.18 μm	5 k	10k	1.1	7.4	127	0.0634	0.06
[17]	LC	0.18 μm	5-3.3 k	-	0.8	$\leq$7.9	313-582	0.219-0.565	0.045
[18]	SAR	65 nm	-	25 k	1.0	8.0	281	0.0433	0.0174
This work	**CT ΣΔ**	**65 nm**	400	**32 k**	**1.2**	**8.6**	**218.4**	**0.70**	**0.225**

Fig. 16 for comparison. The effective number of bits ($ENOB$) of the system is about 8.6 bits, which is calculated by:

$$ENOB = \frac{SNR - 1.76}{6.02} \tag{11}$$

The designed CT ΣΔ A/D modulator consumes about 182 nA current at 1.2 V supply voltage. Most of the power is consumed by the loop filter as indicated in previous section. The figure-of-merit (FOM) of the modulator is about 0.70 pJ/conversion step, calculated by:

$$FOM = \frac{P_{consumed}}{2 \times BW_{IN} \times 2^{ENOB}} \tag{12}$$

where $P_{consumed}$ is the power consumption of the designed CT ΣΔ A/D modulator and BW_{IN} is the bandwidth of input signal. Table III compares the performance of the design in our work and other low-power ADC designs in recent literature.

V. CONCLUSION

This paper presents the design of a low power fully differential 2^{nd}-order CT ΣΔ A/D modulator in a 65 nm CMOS process. The design achieves an ultra-low power consumption of 218.4 nW, making it suitable for pacemaker applications. It may also be used for other medical implantable devices, where low power consumption is a basic design concern. Loop filter of the designed modulator are realised by two cascaded active-RC integrators. The integrator op-amps are designed using folded-cascode topology. To meet the low power consumption requirement, the transistors are constrained to be operating in the weak-inversion region. The paper elaborates the complete top-down design procedure from system synthesis to circuit implementation. Important design issues are discussed for each stage in the design. It may be used as a quick design guidance for engineers and researchers in this area.

ACKNOWLEDGMENT

The authors thank Dejan Radjen and Martin Anderson, Lund University, Sweden, for their help and fruitful discussions throughout the whole work.

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