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Hardware software co-simulation of a digital EMI filter using Xilinx system generator

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Abstract: Mitigation of electromagnetic inference (EMI) is currently a challenge for scientists and designers in order to cope with electromagnetic compatibility (EMC) compliance in switching mode power supply (SMPS) and ensure the reliability of the whole system. Standard filtering techniques: passive and active ones present some insufficiency in terms of performance at high frequencies (HF) because analog components would no longer be controllable and this is mainly due to their parasitic elements. So developing EMI digital filters is very interesting, especially with the embedment of a machine control system on a field programmable gate array (FPGA) chip. In this paper, we present a design of an active digital EMI filter (ADF) to be integrated in a drive train system of an electric vehicle (EV). Hardware design as well as FPGA implementation issues have been presented to prove the efficiency of the developed digital filtering structure.

Key words: ADF, drive train system, conducted EMI noise, XSG, FPGA

1. Introduction

Currently, researchers are investigating alternatives to petroleum-fuelled internal-combustion-engine vehicles (ICEVs) in transportation. This is, mainly, due to the facts of climate change considerations (decreasing emissions of greenhouse gases and urban air pollutants) and minimizing petroleum consumption. The development of advanced electric vehicles (EVs) includes pure battery electric vehicles, hydrogen fuel-cell electric vehicles and plug-in hybrid electric vehicles. The EV stimulates a considerable interest but there are many constraints that developers and designers should take into account in order to ensure the reliability and the security of the EV. This paper deals with EMC compliance in the EV's powertrain system.

The powertrain of battery-power vehicles consists of a battery, a power converter that inverts the direct current (DC) output of the battery to alternating current (AC) and the electric motor. The output of the electric motor is the torque to the wheels that power the vehicle.

The power electronic part is a highly efficient switched-mode three-phase induction motor that produces an inherent common mode (CM) voltage; it drives unwanted currents into the whole system of the drive train. The produced CM currents are considered as a source of EMI, which can not only interfere with other electronic systems of the EV causing intolerable parasitic signals, but also damage the motor reliability and shorten its life.

In literature, reducing EMI was the aim of many works which discussed the effect of the topology of the inverter on EMI; in fact, in voltage source inverters, reducing the level of the switched voltage step, such as it is done in multilevel converters, can reduce the noise source in the system [1–3]. The authors of [4] have shown that a matrix converter can reduce the noise level by 20 dB due to the varying switched voltage, so that both the size of CM and differential mode (DM) filters can be reduced.

In other works, researchers have highlighted the impact of modulation techniques in attenuating EMI noise. Common mode reduction (CMR) techniques was widely used in power inverter to attenuate CM noise [5–7], some authors have exploited modulation techniques with three-level inverters [8–11] and five-level inverters [12–13].

Therefore, filtering technique is still the conventional technique in reducing EMI noise; many works were interested in passive filtering because of its simplicity of design and its performance [14–17], but the disadvantage of both size and cost of the filter were studied in [18–21] to improve its efficiency and deal with its drawbacks. Some authors have considered active filtering as an alternative to passive one [22]. But it proves efficiency ups to 1 MHz and this does not cover the range defined by the standard CISPER22 that consider a frequency range of 150 KHz to 30 MHz [23].

Thanks to the fast progress of digital processing techniques as well as high speed/precision processors, an integrated digital EMI filter has been emerged [24–25].

The developed ADF is realized to be embedded in the FPGA Virtex-5 chip that incorporates the control technique prototype of the induction motor (IM).

The advantages of the digital active filtering (DAF) are mainly size optimization, small parasitic parameters and the lower power consumption. Besides, it is no more frequency dependent.

FPGAs have many advantages like accuracy, reliability, programmability and high processing speed. They are considered as an effective platform for achieving digital control in switch mode converters [26]. Therefore, the execution of several algorithms simultaneously with high processing speed requires a performant processor in order to meet the real time performance requirement.

FPGAs are easily programmed and can also be tested in real time, but the knowledge of a high level language (VHDL or Verilog) is required. The proposed architecture of the ADF is realized using a Xilinx system generator (XSG) which makes the process of implementation on an FPGA simpler.

In this paper, we propose a design of an FPGA-based digital EMI filter in order to overcome conventional filters' disadvantages in terms of size, weight and cost, as well as to improve the efficiency of the whole system.

This paper is organized as follows: section 2 contains the principle of the inverter in order to locate the cause of EMI noise, section 3 is about presenting the design of DAF, section 4 is devoted to the simulations of the drive system train with and without integrating the digital filtering technique and discusses the obtained results, in section 5 we present the results of the hardware-software co-simulation of the EV's drivetrain integrating the ADF and the synthesis results, finally a conclusion about the paper's contribution is given.

2. The two-level inverter's principle

Voltage source pulse width modulation (PWM) inverters have been widely used in variable speed motor drive systems because of their various advantages such as low total harmonic distortion (THD) of output waveforms, high efficiency, a high power factor, etc.

The scheme of a two-level inverter is illustrated by Figure 1.

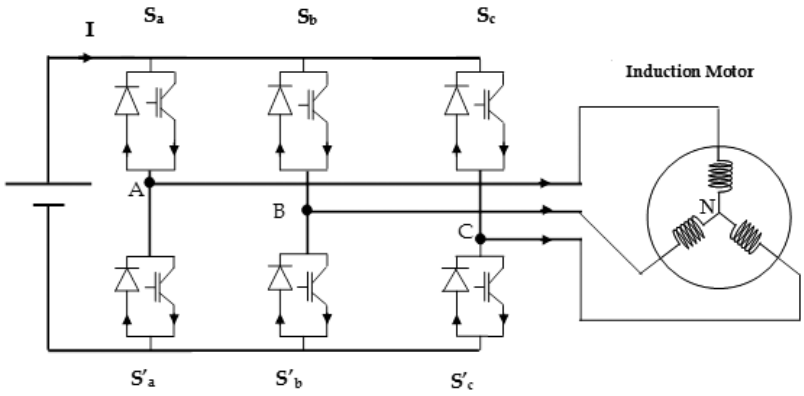

Fig. 1. The scheme of a two-level inverter

The common problem with power inverters is the generation of common mode voltage (CMV) that is due to the combination of switching states as shown in Equation (1):

$$V_{CM} + \frac{1}{3}(V_{AO} + V_{BO} + V_{CO}), \tag{1}$$

where O is the middle point of the DC link.

The CMV leads to leakage current which circulates through stray capacitors and the ground producing conducted and radiated EMI to electronic equipment through power lines [27]. This current may cause bearing failure of the induction motor [28] and even produce mechanical vibration [29]. These negative impacts are more significant with the increase of switching frequency and power of electronic elements.

The purpose of the presented work is to attenuate the undesirable EMI conducted noise caused by the power inverter of the EV's drive train.

3. The design of the ADF (active digital filter)

3.1. An overview of active analog EMI filters

An active noise cancellation technique is realized by using active devices that generate and inject the EMI noise, which is the opposite of the EMI system noise. But the switching speeds of these active components are unable to cover the whole frequency range (from 150 KHz to 30 MHz); in fact, their reliability is up to 3 MHz. So, in higher frequencies, passive components are needed to increase the filter's efficiency [30]. The disadvantages of the analog filter are mainly the parasitic components of analog devices which are more considerable in high frequencies, their volume and cost. Compared to analog filters discrete ones are characterized by their independency on frequency. Besides, there is no particular volume devoted to them since they are integrated with the system's control algorithm in the FPGA chip.

The next part is devoted to present the ADF; its principle of attenuating the EMI noise developed using XSG and the whole system of the drive train integrating the ADF.

3.2. The principle of the ADF

An ADF principle is developed in [24–25] and it is based on three steps:

- Sensing part: this stage is devoted to sense the noise signal. The used circuit is an RC high-pass filter with a cutoff frequency of 150 KHz.
- Control part: the role of this part is to generate a 180° degree shift signal.
- Injection part: this step is about injecting with high fidelity the produced opposed shift noise signal in the order of the nullification of the EMI noise signal. The used circuit at this stage is a RC low-pass filter with a cutoff frequency of 30 MHz.

The chosen cutoff frequencies aim to localize the frequency spectrum at the frequency range of interest (from 150 KHz to 30 MHz).

3.3. Transfer function of the ADF

The transfer function of the ADF is derived according to Figure 2 and the parameters of the DAF are tabulated in Table 1.

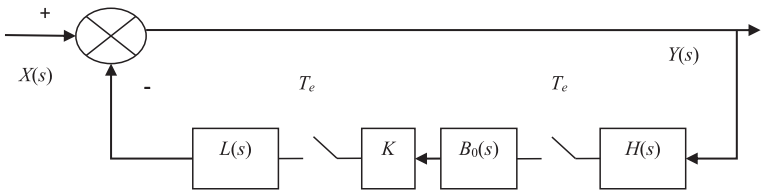

Fig. 2. The closed-loop block diagram of DAEF

where:

- $X(s)$ and $Y(s)$ are, respectively, the sensed noise and the injected noise,
- $H(s)$ is the transfer function of the sensor $H(s) = \dfrac{R_1 C_1 s}{1 + R_1 C_1 s}$,

– $L(s)$ is the transfer function of the injector $L(s) = \dfrac{1}{1 + R_2 C_2 s}$,
– the zero-order hold (ZOH) is the mathematical model of the practical signal reconstruction done by a conventional digital-to-analog converter (DAC), $B_0(s)$ is the transfer function of the DAC: $B(s) = \dfrac{1 - e^{-sT_e}}{sT_e}$, T_e is the sample period,
– K is the coefficient of the inversion process.

Table 1. Parameters of the developed ADF

Circuit	Parameters
ADC	100 MSPS
DAC	100 MSPS
Injecting circuit	R2 = 30 Ω, C2 = 1 nF
Sensing circuit	R1 = 1 KΩ, C2 = 0.1 μF

We design by $L(z)$ and $H(z)$ the Z-transform (ZT) of the continuous transfer functions $L(s)$ and $H(s)$ $H(z) = ZT(H(s))$; $L(z) = ZT(L(s))$. The discrete transfer function of the DAEF is given by Equation (2).

$$G(z) = \frac{1}{1 + L(z) \times H(z) \times ZT(K \,.\, B_0(s)} \,. \tag{2}$$

3.4. The design of the ADF using XSG

Compared to microcontrollers and digital signal processing (DSP), an FPGA shows the best performances that make it superior to other processors: its programmable hardware structure, the ability of parallel processing and the real time implementation are considered as the main features of the FPGA board layout. For the control of an IM, the FPGAs are widely used and this makes the digital filtering technique of conducted EMI noise interesting since it is embedded with the controller of the IM; therefore, the ADF allows the producer to reduce the size and save cost compared to conventional analog filtering techniques.

For prototyping the ADF in the FPGA, knowledge of the required hardware description language VHDL is required which complicates the intended task. An XSG is a toolbox developed for MATLAB/Simulink which enables a generation of a synthesizable VHDL code to be directly used for a Xilinx FPGA chip. The XSG makes the co-simulation of the hardware with the graphical environment of Simulink (Mathworks models based-Simulink) possible in order to validate the proposed designs. The FPGA implementation flow of the ADF is given in Figure 3.

The scheme of the ADF is developed using the XSG. The embedded design is created with the different blocks in the Xilinx block sets and it is based on the principle of an active filtering technique as detailed in the previous paragraph. It consists mainly of three stages:

– The analog-to-digital converter (ADC): AD9071 is used for a high-performance signal path. The frequency of the ADC must be higher than twice the upper limit of the frequency spectrum to fulfil a Nyquist criterion. The selected ADC operates at 100 MSPS and it is

characterized by a resolution of 10 bits. This ADC is designed to convert the analog signal (the sensed noise signal) to digital one.

– The inversion process: the sampled signal issued from the ADC is conducted to be processed into a phase reversal algorithm.
– The digital-to-analog conversion (DAC): the used device is THS6551. It is a 10 bit high speed converter with a sampling rate of 100 MSPS. Its role consists in the conversion of the digital inverted signal to an analog one in order to be injected into the circuit to nullify the sensed noise.

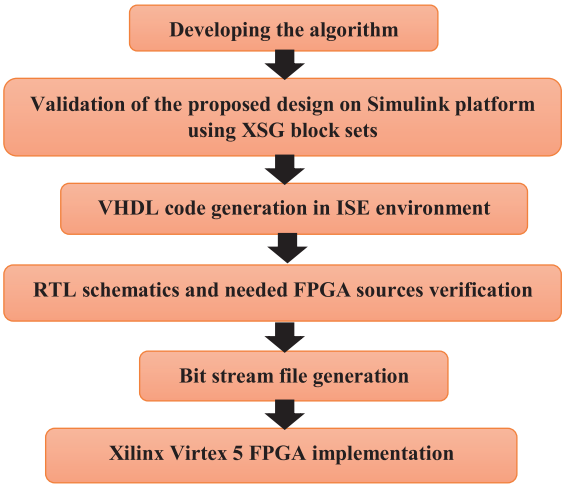

Fig. 3. FPGA Implementation flow using XSG

The design of the ADF based on the previous model of different described stages is realized by using black boxes and the predefined Xilinx block sets. Its scheme is illustrated in Figure 4.

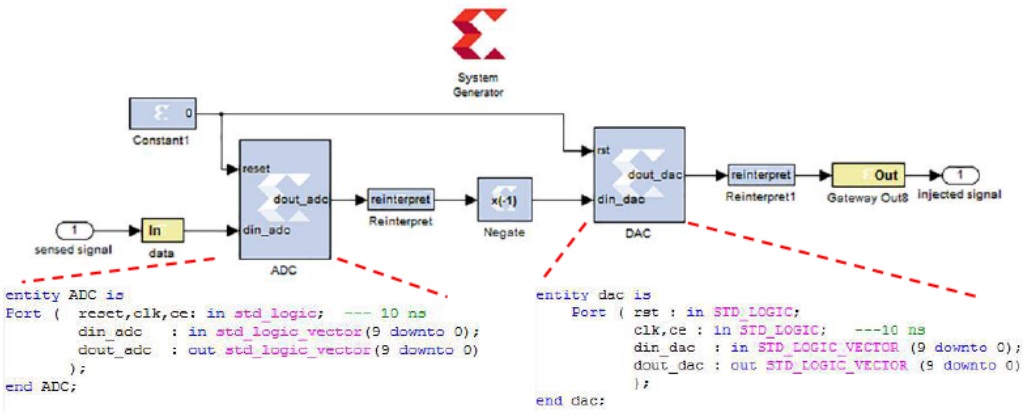

Fig. 4. The design of the ADF with Xilinx blocks

4. The model of the drive train integration of an ADF

The inverter is considered as the main cause of conducted noise in the drive system and it has been determined that the CM emissions dominate the conducted noise level [31].

The line impedance stability network (LISN) is used in an EMI measurement step at the frequency range of interest (from 150 KHz to 30 MHz). This configuration is used to evaluate the effects of the switching elements of the inverter on the motor.

The process of active noise attenuation is considered as an adaptive technique, it does not require a well-defined model of the system or a fixed level of EMI attenuation calculation. In fact, it is based on sensing, inverting and injecting a signal that is opposed to the sensed one. A decoupling inductor is inserted between the sensing circuit and the injecting one as a decoupling network.

The whole system of the EV's drive train including the battery, the LISN, the inverter, the induction motor and sensing and injecting ports is simulated using PSpice and the scheme is illustrated in Figure 5.

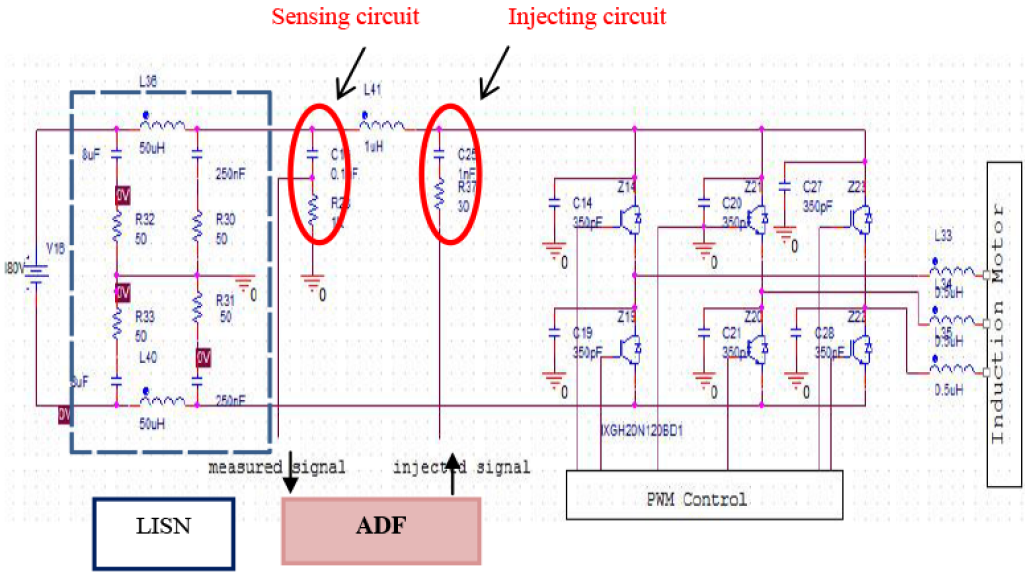

Fig. 5. PSpice schematic of the drive train system with the integration of an ADF

The input conducted EMI noise is received by a sensing circuit and digitized by an ADC unit. The acquired data is processed using a reverse data algorithm, then converted to the analog form using the DAC and injected into the system via an injecting circuit.

In order to validate the scheme of the proposed ADF, the drive train system of the EV is extracted to Simulink using an SLPS interface. The PSpice SLPS interface is a tool developed by Mathworks that enables the co-simulation between PSpice and MATLAB/Simulink. So the

drive train scheme is included in the Simulink system simulator allowing a single prototype to co-simulate both the established drive train system and the developed ADF, using the XSG.

The scheme of the EV's drive train system including the ADF is presented in Figure 6.

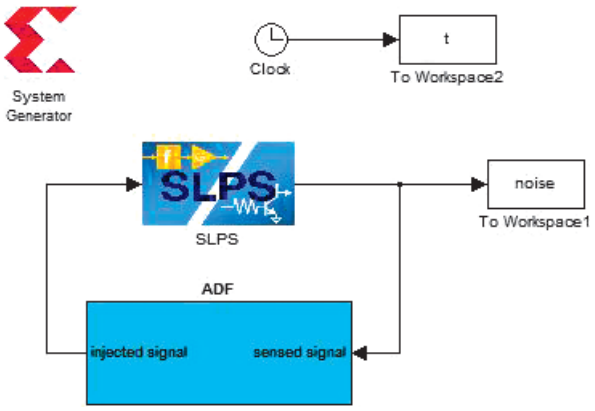

Fig. 6. The drive train system and the ADF design on MATLAB/Simulink

Figure 6 illustrates a co-simulation between PSpice/Simulink englobing the two schemes of Figure 5 and Figure 4.

Simulation results and interpretations are detailed in the following paragraph in order to investigate the contribution of the digital EMI filtering technique.

5. Simulation results and interpretation

The conducted noise is visualized in frequency spectrum by using the fast Fourier transform (FFT) to compare a performance of drive system with/without an ADF.

Figure 7 and Figure 8 illustrate, respectively, the frequency spectrum of EMI CM conducted noise without and with the integration of the ADF.

The first simulation is performed without integrating the EMI filter. As illustrated in Figure 7, we can note that the level of conducted CM EMI noise is attenuated from a value of 155.8 dBμV to an average value of 80 dBμV in a frequency range varying from 170 KHz to 30 MHz.

The second simulation is performed integrating the ADF filter. We can note that the frequency spectrum is attenuating in the frequency range of 150 KHz to 30 MHz, the higher values of CM conducted noise are depicted in the range of 150 KHz to 1 MHz with an average value of 92 dBμV. Generally, there is an attenuation of about 30 dBμV in the conducted EMI noise at the whole frequency range.

The performance of the ADF in terms of attenuating CM conducted noise is proved by simulation results.

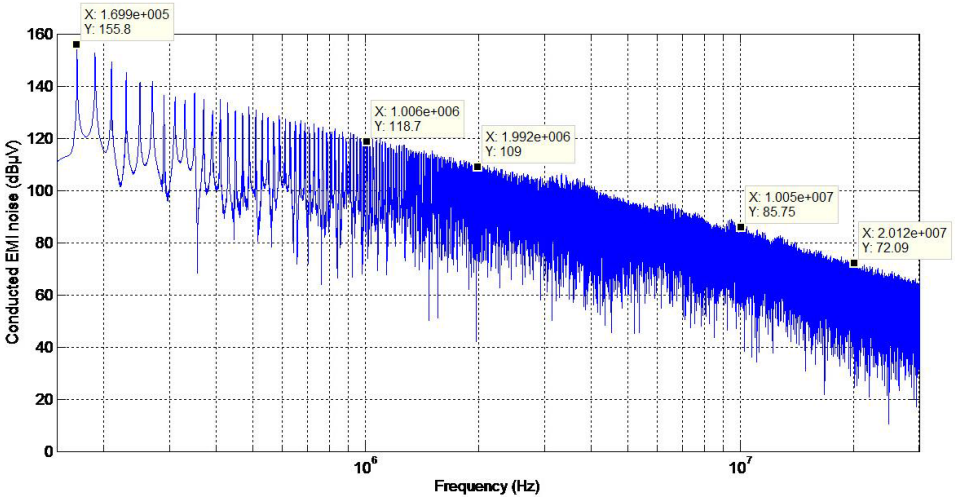

Fig. 7. CM EMI conducted noise without ADF filter

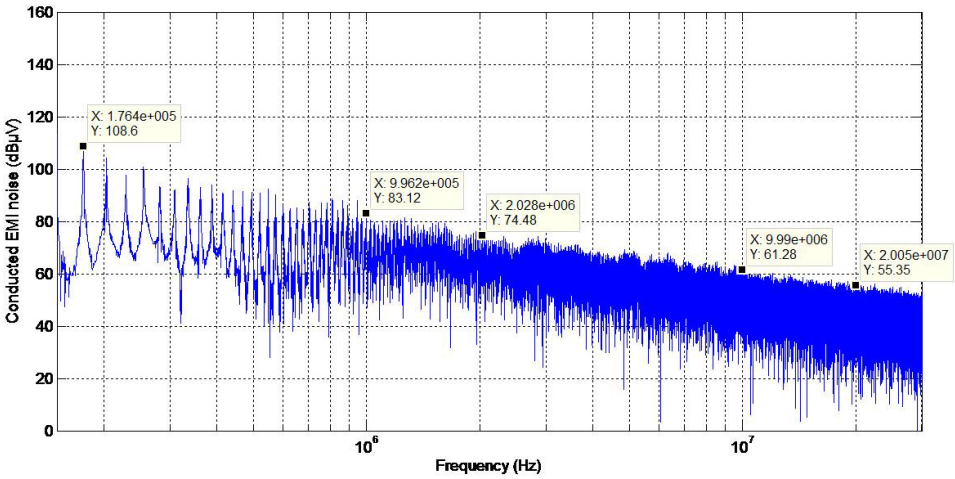

Fig. 8. CM EMI conducted noise with the integration of an ADF

6. Hardware software co-simulation and synthesis results

6.1. Hardware software co-simulation

The XSG, embedded in MATLAB/Simulink is used to design the filtering prototype. Then, it is possible to test it on the FPGA board using the properties of hardware co-simulation tools. The design was implemented targeting a Virtex-5 device.

Figure 9 shows the drive train system of an EV integrating a ADF simulation using hardware software co-simulation based on the FPGA Virtex-5 board.

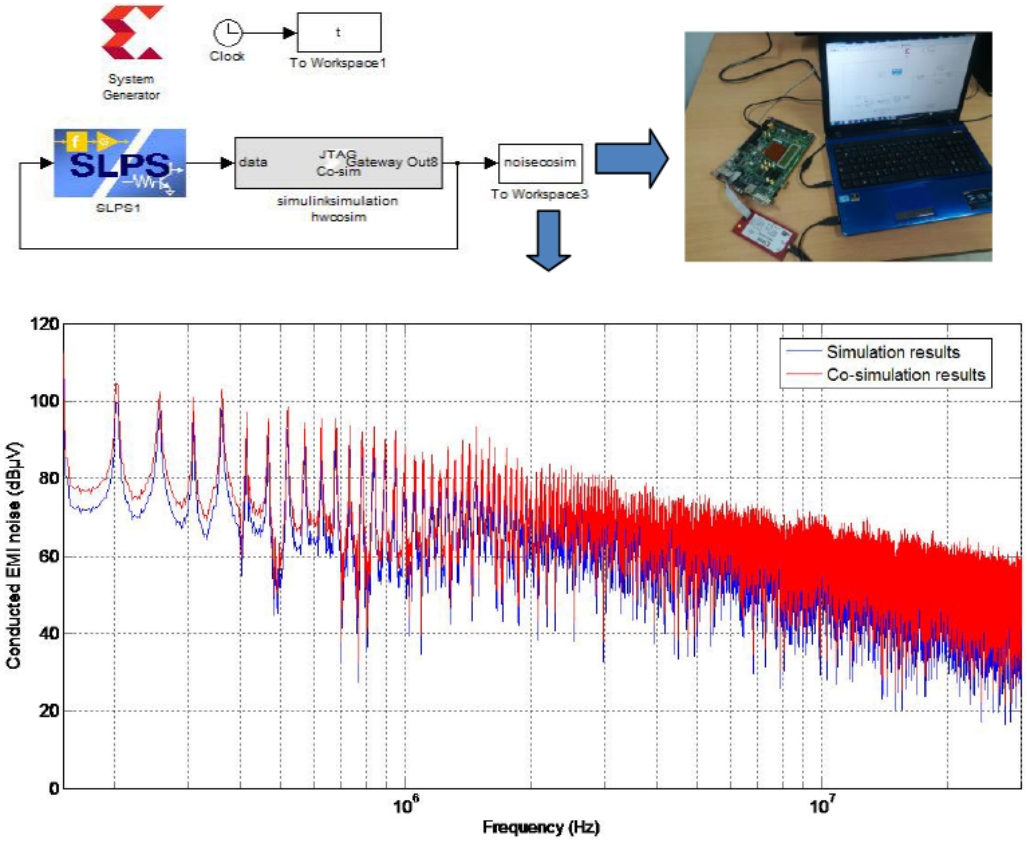

Fig. 9. Hardware software co-simulation using MATLAB/Simulink model on Virtex-5 platform

6.2. Synthesis results

The hardware block of the ADF established in an XSG can be synthesized and downloaded into the target FPGA chip. The complete design was verified for area utilization, timing and power consumption using Xilinx ISE. Figure 10 illustrates the RTL schematic implementation result made by Xilinx ISE and Table 2 shows the implementation results for ADF resources utilization of the implementation on Viretex-5.

Table 2. ADF resources utilization table

Resources	Available	Utilization
Number of slice registers	44 800	1%
Number of slice LUTs	44 800	1%
Number of bonded IOBs	640	3%
Number of BUFG/BUFGCTRLs	32	3%

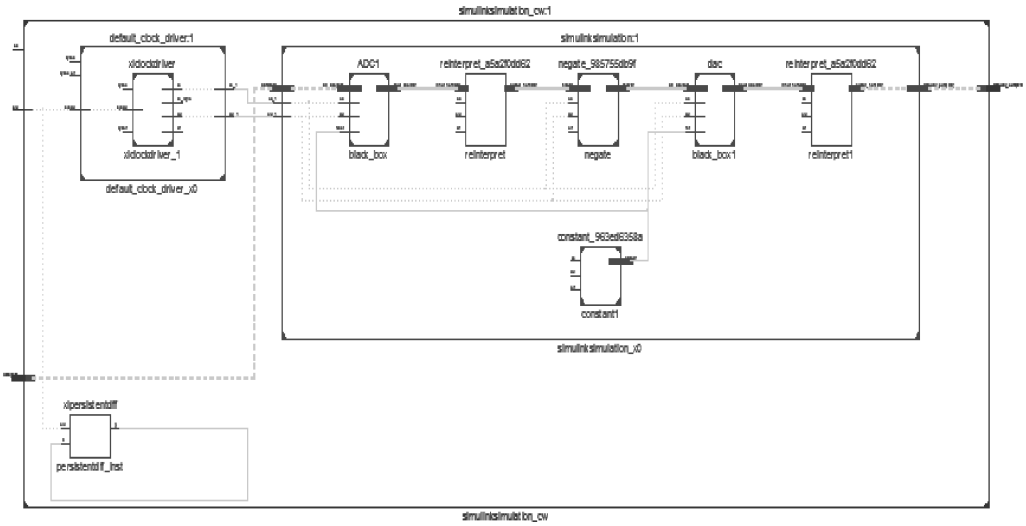

Fig. 10. RTL schematic structure of real-time configurable system for the ADF design implementation on FPGA

7. Conclusion

In this paper, an ADF is presented. Its concept is based on measuring the EMI behaviour and injecting an opposed signal at the determined injecting point in order to eliminate the conducted CM EMI disturbance. The performance of the proposed method is evaluated by simulative results with and without the integration of the digital EMI filter. The ADF is implemented in a reconfigurable logic platform using XSG for MATLAB.

The novel filtering technique proves its efficiency in terms of cost, size and conducted EMI noise attenuation. The hardware software co-simulation proves its efficiency under real-time constraints.

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