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Graphene-based Current Mode Logic Circuits: a Simulation Study for an Emerging Technology

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***Abstract*—In this paper, the usage of graphene transistors is introduced to be a suitable solution for extending low power designs. Static and current mode logic (CML) styles on both nanoscale graphene and silicon FINFET technologies are compared. Results show that power in CML styles approximately are independent of frequency and the graphene-based CML (G-CML) designs are more power-efficient as the frequency and complexity increase. Compared to silicon-based CML (Si-CML) standard cells, there is 94% reduction in power consumption for G-CML counterparts. Furthermore, a G-CML 4-bit adder respectively offers 8.9 and 1.7 times less power and delay than the Si-CML adder.**

***Keywords*—Current mode logic (CML), graphene, graphene FET, low-power design**

I. Introduction

TODAYS, low-power designs are being increasingly important for VLSI developers [1-4]. There are several approaches to reduce the power such as transistor sizing, logic styles, threshold reduction, etc [5-7]. Although these approaches have a positive impact on power consumption, the scaling of the power ignoring the critical performance bottleneck of silicon technology seems to be not viable beyond 2020 [8, 9]. Emerging nanoelectronic devices based on carbon nanotubes and graphene have recently attracted widespread attention due to their potential in solving challenges ahead for silicon technology [10, 11].

Two constituting components of the power consumed by a circuit are called static power and dynamic power [1, 12]. The static power refers to the portion of the power when a constant current passes through a circuit. Leakage currents like oxide leakage usually are a main source for dissipating the static power [13]. The consumption of this power can be managed by disabling the inactive portion of a large circuit. The dynamic power dissipates when the process of switching executes. It is the sum of capacitive load power consumption and transient power consumption [1, 12]. The amount of this power is proportional to frequency of operation, supply voltage, and load capacitances. It is obvious that as the speed (frequency) and complexity of a digital circuit become higher, the amount of the dynamic power increases. So, the dynamic power is expected to be growing in digital systems. This paper examines a new emerging technology, i.e., graphene technology, to explore its potential for mitigating the above issues.

Graphene technology is known as an alternative for post silicon technology due to higher mobility and lower short channel effects [14-17]. The former makes the device faster and increases the cut-off frequency. The latter gives rise to further scaling the transistor dimensions without losing the performance as compared to the silicon counterpart. Moreover, the planar fabrication process of graphene transistors is compatible with current state of the art technologies [18]. The development of graphene integrated circuits can then be more feasible in comparison with other non-planar technologies.

Current mode logic (CML) designs are used for hardware implementation in cryptography and mix-signal applications [19-22]. So far, there is no clear study about the efficiency of graphene-based CML (G-CML) designs. Hence, it is important to study the G-CML designs in standard logic gates. In this paper, we demonstrate the efficiency of power, delay, power-delay product (PDP), energy-delay product (EDP) for inverter, AND, OR, and XOR gates based on the G-CML design. The results are compared with high-performance silicon FINFET technology. Moreover, the performance and frequency analyses of a 4-bit adder are included to give more validity to our results.

The rest of the paper is organized as follows: Section 2 and 3 present an overview of key points related to silicon and graphene field-effect transistors, respectively. Section 4 provides a demonstration of static complementary logic (abbreviated as static) and CML styles particularly for fundamental CML gates namely Inverter, AND, OR and XOR. In Section 5, a detailed case study of an inverter including frequency analysis has been exhibited. Section 6 expresses the results and discussion associated with graphene and silicon-based circuits in the both static and CML styles. Finally, a brief summary is outlined at the last section.

II. Silicon FETs

Silicon FETs have received great deal of attention in semiconductor industry along the past decades. In nanoscale era, the channel controllability of gate is usually lost in the planar silicon FETs [23]. A silicon FINFET with a particular gate shape has presented an option for extending MOSFET scaling where the gate control is deteriorated and short channel effects are appeared [24]. BSIM-CMG model is a well-known approach to model such transistors [25]. In this model, terminal currents and charges over the different regions of operations are expressed by surface potential. The approach starts with the inclusion of long-channel device and then numerous physical effects such as quantum mechanical effect, poly-depletion effect, short channel effects, mobility

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degradation and carrier velocity saturation are attached to the main model. Hereafter, the 16-nm high-performance library from predictive technology model (PTM) is included in circuit simulations [26, 27]. The PTM model, developed by Arizona state university, is a powerful tool for accurately predicting the characteristics of the nanoscale silicon FINFET using the BSIM-CMG model.

III. Graphene FETs

There is a strong motivation to utilize two dimensional materials as transistor channel particularly when successful preparation of graphene samples has been achieved in 2004 [28-30]. Graphene with honeycomb lattice structure explores high electrical and thermal conductivity [31]. It has been introduced to be a possible successor material of conventional semiconductors [39, 40]. Graphene is an allotrope of carbon atoms which is formed by sp^2 hybridization [32]. This arrangement includes three combined orbitals forming σ bonds and a single p orbital forming π bonds. The honeycomb lattice structure of graphene originates from σ bonds. The single p orbital orienting perpendicular to a graphene sheet has a major contribution on electrical properties of grapheme [32]. So, a tight-binding approach within the nearest neighbor approximation is adopted to model the bandstructure of graphene including the single p orbital [30, 32].

A typical demonstration of a graphene nanoribbon (GNR) is shown in Fig. 1. Electrons in graphene behave like massless fermions and so represent much higher mobility [29, 30]. This originates from cone-shaped bandstructure in K points of Brillouin zone. Although large-scale graphene sheets are gapless, it is shown that a finite bandgap is achievable by means of lateral confinement [33].

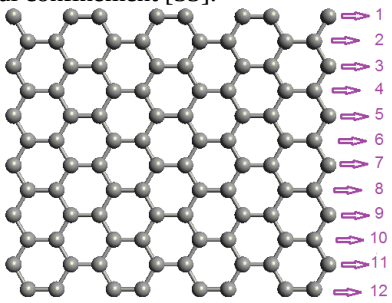

Fig. 1. Lattice structure of an armchair-type GNR with N = 12. N is the number of dimer lines in the armchair orientation

Since any new investment in semiconductor industry is huge, materials posing lower modifications in fabrication process are acceptable. Graphene devices are compatible with current state-of-the-art CMOS fabrication process and are becoming an interesting option among the other similar competitors' materials for post-silicon devices [18].

As a matter of fact, graphene FETs depending on the contact material are divided into two types [34]. The first type is Schottky-barrier FET (SBFET) in which metals with Schottky contacts are connected to the channel. The Second type named as MOSFET-like FET uses ohmic contacts by heavily doping the GNR source and drain extensions. Since MOSFET-like FETs have better device characteristics over SBFETs particularly in on–off current ratio and switching behavior [34], we choose the MOSFET-like type of graphene FET in this work and it is called graphene FET (GFET) in the following discussion.

Modeling of the GFETs is introduced by several different approaches [35-38]. However, the inclusion of either required numerical integrals or a complete set of parameters causes serious challenges in circuit simulation to rebuild the model for a new device [36-38]. Chen et al. have proposed a parameterized, SPICE-compatible model for graphene-based transistors [35]. This allows designers to evaluate custom designs more quickly and straightforwardly.

Fig. 2 illustrates the structure of the GFET consisting of multiple parallel GNRs as the channel [35]. Drain and source contacts are formed by ribbon extensions and known as reservoirs. Each GNR has equal length L_{CH} and width W_{CH} and all the GNRs are located under a single gate. W_G is the gate width and $2W_{sp}$ is the spacing between the GNRs. The GNRs under the gate are assumed to be intrinsic while the reservoirs are doped with doping fraction f_{dop}.

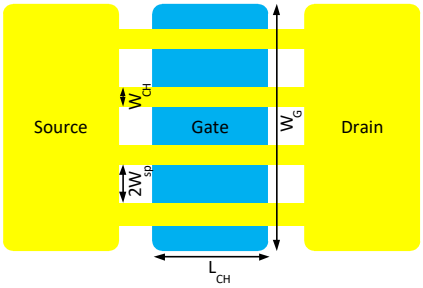

Fig. 2. The structure of a four-ribbon GFET

The equivalent circuit of a GFET is shown in Fig. 3. The model is composed of three parts: a channel potential V_{CH}, channel capacitances ($C_{G,CH}$, $C_{SUB,CH}$, $C_{CH,D}$, and $C_{CH,S}$), and a current source I_{DS}. The channel potential V_{CH} is calculated by equating the accumulated charge across all the capacitances coupling to the channel. The channel charge Q_{CH} is derived from graphene bandstructure which basically is function of subband characteristics, tunneling probability, and external voltages applied to the drain/source contacts (V_D, V_S). Then, the channel capacitances are presented as follows [35]:

$$C_{G(SUB),CH} = \frac{5.55 \times 10^{-11} \varepsilon_r L_{CH}}{\left(1 + \frac{1.5T_{ox}}{W_G}\right) ln\left(\frac{5.98W_{CH}}{0.8T_{ox}}\right)} \tag{1}$$

$$C_{CH,D} = \frac{\partial Q_{CH}}{\partial V_D} \tag{2}$$

$$C_{CH,S} = \frac{\partial Q_{CH}}{\partial V_S} \tag{3}$$

wherein ε_r and T_{ox} are relative permittivity and thickness of the dielectric material, respectively.

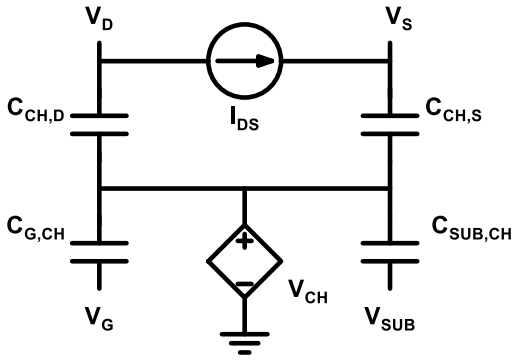

Fig. 3. SPICE model of a single GNR.

Consequently, the current source based on the Landauer-Buttiker formalism is expressed by considering Fermi-Dirac distribution $f(.)$ and subband index α as follows [39-41]

$$I_{DS} = \frac{2q}{h}\sum_{\alpha}\int_{0}^{\infty}\left[f\left(E - E_{FS,C}\right) - f\left(E - E_{FD,C}\right)\right]dE \qquad (4)$$

in which h is Plank's constant, E is the energy level relative to the conduction band E_C, and $E_{FD,C}$ ($E_{FS,C}$) is the difference between E_C in the GNR channel and E_F at the drain (source) contact.

IV. Logic Styles

The traditional logic style widely used in the design of digital integrated circuits is known as static style due to its advantages such as low static power dissipation and high packing density [1]. In this logic style, there are two pull-up and pull-down networks consisting of pure P-type and N-type FETs (PFETs and NFETs), respectively (Fig. 4a). The pull-up network turns on when the output of logic input values should be connected to the supply voltage and yields logic one. In this time, the pull-down network turns off and shows a high resistance path. Similarly, the pull-down network makes a connection between the output and ground when the output of logic input values should be logic zero. In this time, the pull-up network provides a high resistance path.

There is another popular logic style exploiting merits of differential pairs and it is known as current mode logic (CML) style (Fig. 4b) [19]. In fact, a CML gate has two main parts namely a pull-up network and a pull-down network. Setting the DC voltage drop on the output is mostly achieved by the pull-up network in which either two resistors or PFETs are used. On the other hand, the pull-down network is composed of one NFET as a current source and a number of NFETs that work as a functional unit. Some of the CML gates have been shown in Fig. 5. Logic implementation based on this approach has attracted much attention in cryptography and mixed-signal applications [19-22]. In subsequent sections, the static and CML styles in the both graphene and silicon FINFET technologies are evaluated in several standard and arithmetic circuits.

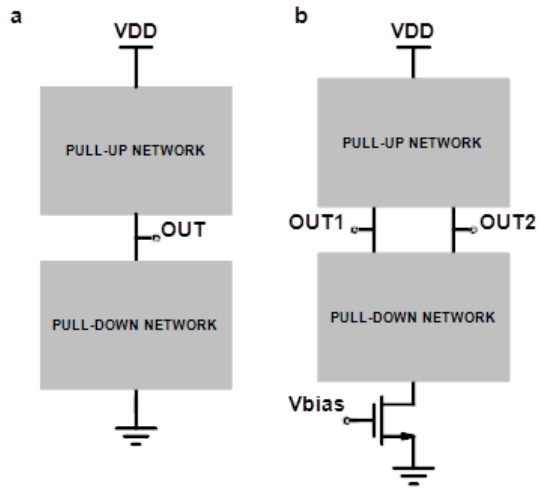

Fig. 4. The universal diagram of logic styles (a) Static (b) CML.

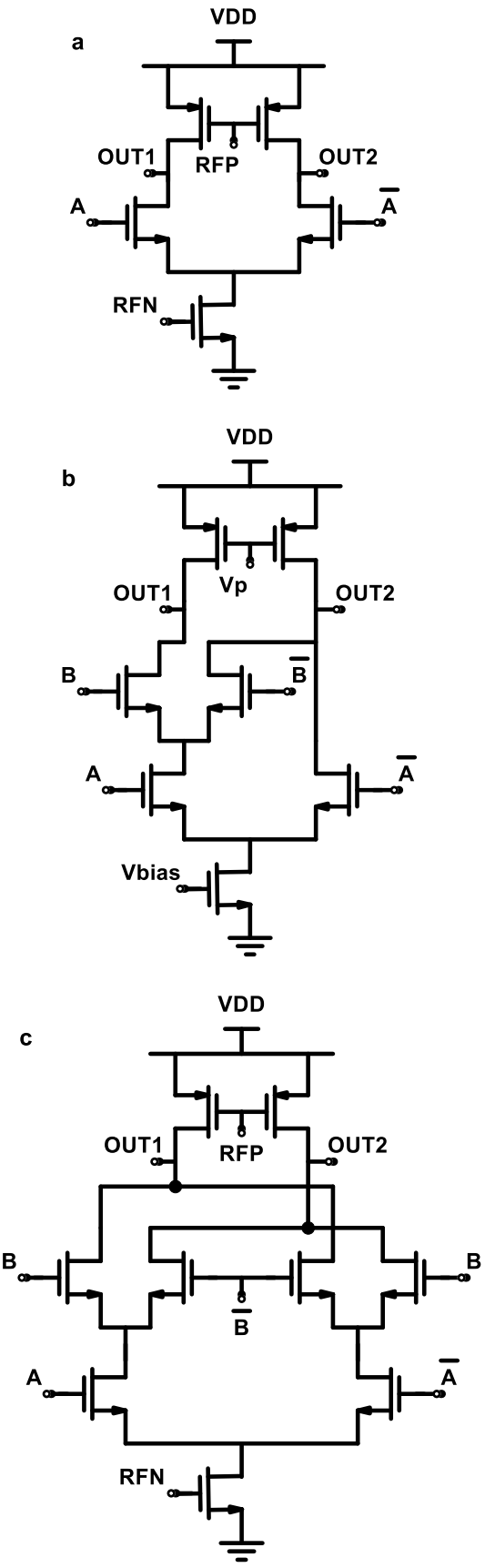

Fig. 5. The schematic structure of three different CML circuits (a) Buffer/Inverter (b) AND/NAND/OR/NOR (c) Exclusive-OR (XOR).

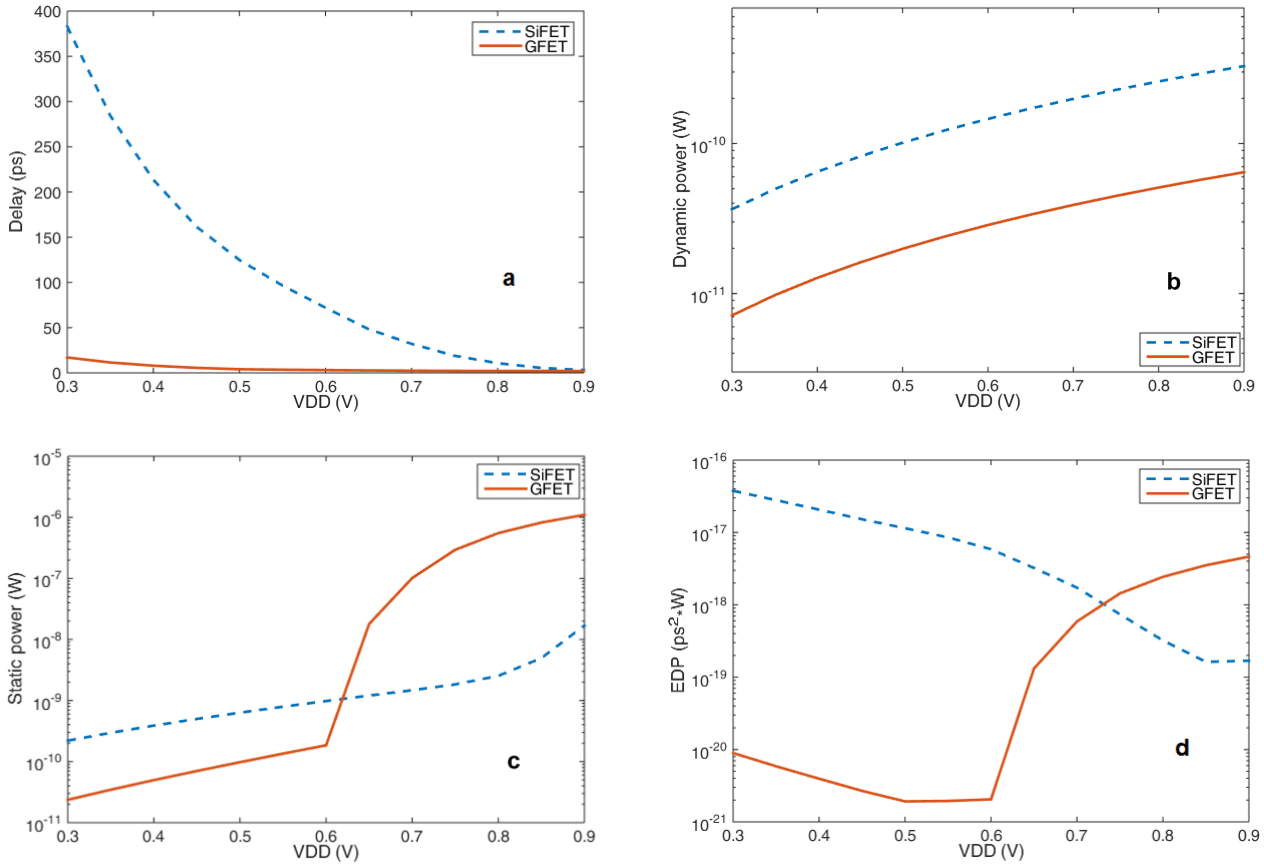

Fig. 6. (a) Delay, (b) dynamic power, (c) static power, and (d) EDP vs. V_{DD}.

V. Case Study: Inverter

In this section, we would like to present a typical inverter (NOT gate) in both the graphene and silicon FINFET technologies and the static and CML styles. To have a fair comparison with the silicon FINFET, the GFETs with a 16nm-long N=12 GNR, T_{ox}=1.35 nm, and f_{dop}=0.001 are considered to match the dimensions. It is noted that all the following simulations are carried out with HSPICE. Fig. 6 shows the delay, static and dynamic powers of a static inverter in the both technologies. The delay and dynamic power smoothly change as the drain voltage rises. However, there is a sharp profile in the static power of the GFET-based inverter, which is attributed to a smaller bandgap of the graphene facilitating band to band tunneling between source and drain contacts [30]. Based on the minimal energy-delay product (EDP) for voltages ranging between 0.3 and 0.9 V, we choose nominal V_{DD}=0.85 V and 0.5 V for the SiFET and GFET, respectively.

The applied input and output of an inverter circuit in two design styles are shown in Figs. 7 and 8. In the CML-based inverter circuits, the output swing is slightly decreased to supply the adequate power for the current source. As can be seen, the reduction in the swing of the G-CML inverter is lower than that in the swing of the silicon-based CML (Si-CML) counterpart.

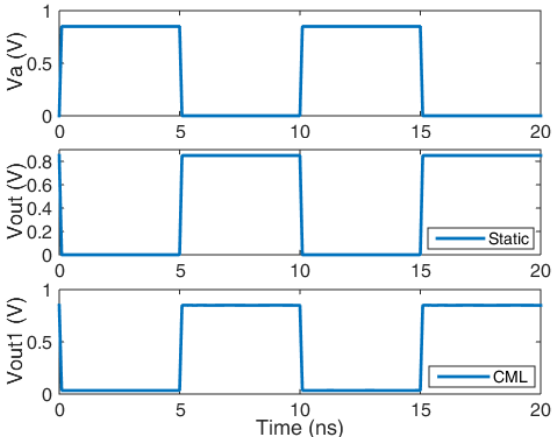

Fig. 7. Inverter simulation results in the silicon technology.

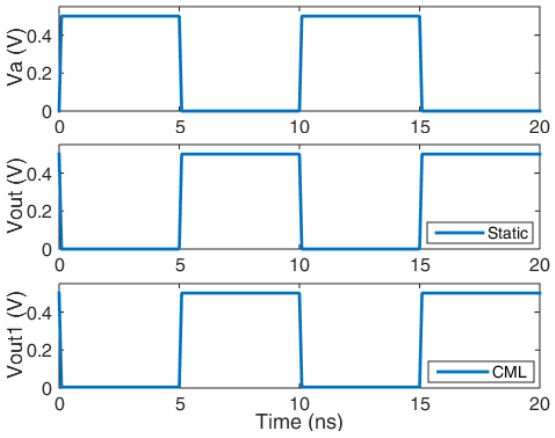

Fig. 8. Inverter simulation results in the graphene technology.

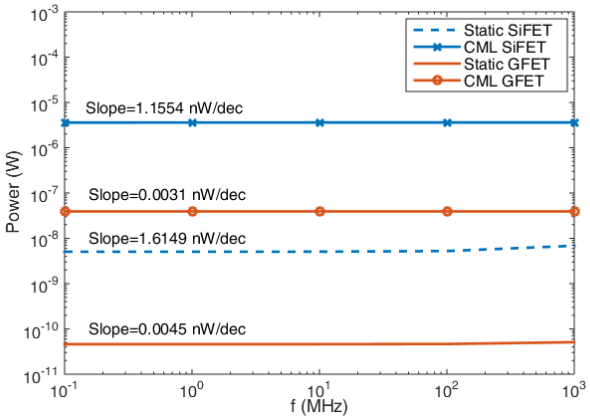

Fig. 9. Power versus frequency in an inverter for silicon and graphene technologies.

The output power versus frequency is demonstrated in Fig. 9. As we would be expected, the CML circuits consume more power than the static circuits in the both technology due to a larger static power. However, the slopes of the power consumption have been reduced in the CML-based circuits compared to the static-based counterparts. It can be seen that the least frequency dependence in the G-CML inverter is achievable and this makes the G-CML design more appealing at higher frequencies.

VI. Simulation Results and Discussion

In this section, the circuit evaluation is divided into two parts namely standard gates (i.e. Inverter, AND, OR and XOR) and arithmetic circuits (i.e. 1-bit and 4-bit adders). The operating frequency is mainly set to 100 MHz for all the following simulations.

A. Standard gates

Tables I and II demonstrate the simulation results in terms of area, delay, power, power-delay product (PDP) and energy-delay product (EDP). Results show that the delay of the static GFET-based circuits approximately is 1.4 times lower than that of the static SiFET-based circuits. The origin of such an observation is attributed to higher mobility and near-ballistic transport in the graphene [29, 30]. The reduction of delay is also observed in the corresponding CML designs. The G-CML circuits on an average yield 5 times lower delay than the Si-CML circuits.

The significant advantage of the GFET-based implementation is relevant to saving power consumption. Generally, the total power of a digital circuit is composed of three terms [42]

$$P_t = P_{static} + P_{chrg} + P_{sc} \tag{5}$$

$$P_{static} = I_{static} V_{DD} \tag{6}$$

$$P_{chrg} = \alpha^* f C_L V_{DD}^2 \tag{7}$$

$$P_{sc} = \alpha^* f V_{DD} I_{peak} t_{sc} \tag{8}$$

wherein I_{static}, V_{DD}, α^*, f, C_L, I_{peak} and t_{sc} are static DC current, voltage of power supply, activity factor of a cell, frequency, the equivalent capacitance of each node, the maximum height of switching current and the width of switching current, respectively.

TABLE I
DELAY AND POWER OF THE SILICON-BASED STATIC AND CML STANDARD CELLS

Design style	Cell	Transistor counts	Delay [ps]	Power [nW]	PDP [nW × ps]	EDP [nW × ps^2]
Static	INV	2	5.5655	5.2409	29.16823	162.3358
	AND2	6	8.375	10.9578	91.77158	768.5869
	OR2	6	5.815	14.4968	84.29889	490.1981
	XOR2	8	2.4	9.46776	22.72262	54.5343
	Total Avg.	5.5	5.538875	10.0408	55.61474	308.0431
CML	INV	5	0.7385	3612.85	2668.09	1970.384
	AND2	7	4.025	3656.46	14717.25	59236.94
	OR2	7	3.375	3581.86	12088.78	40799.62
	XOR2	9	2.33	3739.84	8713.827	20303.22
	Total Avg.	7	2.617125	3647.75	9546.618	24984.69

TABLE II
DELAY AND POWER OF THE GRAPHENE-BASED STATIC AND CML STANDARD CELLS

Design style	Cell	Transistor counts	Delay [ps]	Power [nW]	PDP [nW × ps]	EDP [nW × ps^2]
Static	INV	2	4.035	0.04642	0.187305	0.755774
	AND2	6	6.29	0.47307	2.97561	18.71659
	OR2	6	3.485	0.64913	2.262218	7.88383
	XOR2	8	1.75	0.36118	0.632065	1.106114
	Total Avg.	5.5	3.89	0.38245	1.487731	5.787272
CML	INV	5	0.365	39.3676	14.36917	5.244749
	AND2	7	0.6	281.331	168.7986	101.2792
	OR2	7	0.6	281.176	168.7056	101.2234
	XOR2	9	0.525	281.764	147.9261	77.6612
	Total Avg.	7	0.5225	220.909	115.425	60.30954

The first term of the total power is static power P_{static} and shows the power consumption when no switching event occurs. Two remaining terms are called dynamic power. P_{chrg} is the portion of the dynamic power in which a current flows to charge or discharge the parasitic capacitances at each node. In complementary logic designs, i.e. static designs, there is a short period of time causing a low resistance path when the signal of a cell node is changed [38]. The power consumption in this period is known as P_{sc}. CML designs approximately eliminate P_{sc} because transistors in this logic style do not work complimentarily. In other words, there is no a low resistance path between power supply and ground in CML designs during switching event.

The static and CML GFET-based circuits manifest remarkable lower power dissipation than the SiFET-based circuits. The values for the static and CML styles in the GFETs are 26.3 and 16.5 times lower than those in the SiFETs, respectively. There are other metrics such as PDP and EDP in order to evaluate the performance. PDP shows energy consumption per each switching event, which is defined as the product of the power and the gate delay. At lower frequency, EDP is usually reported and expressed by the product of the PDP and the gate delay. We involve the both metrics and achieve superior improvement in the static and CML styles when silicon and graphene technologies are compared. For example, the PDP and EDP of the G-CML gates are 83 and 414 times lower than those of the Si-CML counterparts, respectively.

B. Arithmetic circuits: 1-bit and 4-bit adders

This part deals with arithmetic circuits including 1-bit and 4-bit adders. This helps to evaluate the results in more complex circuits by considering additional stages. First, the 1-bit CML adder shown in Fig. 10 is compared to the static counterpart. As summarized in Tables III and IV, results reveal that the static and CML GFET-based adders have a positive impact on the performance. The delay and power have been improved in the GFET-based adders. The PDP and EDP of the GFET-based 1-bit adders are about (up to) two orders of magnitude smaller than those of the SiFET-based counterparts.

Secondly, four 1-bit adders are cascaded in parallel to add 4-bit numbers. This adder is called ripple carry adder in which

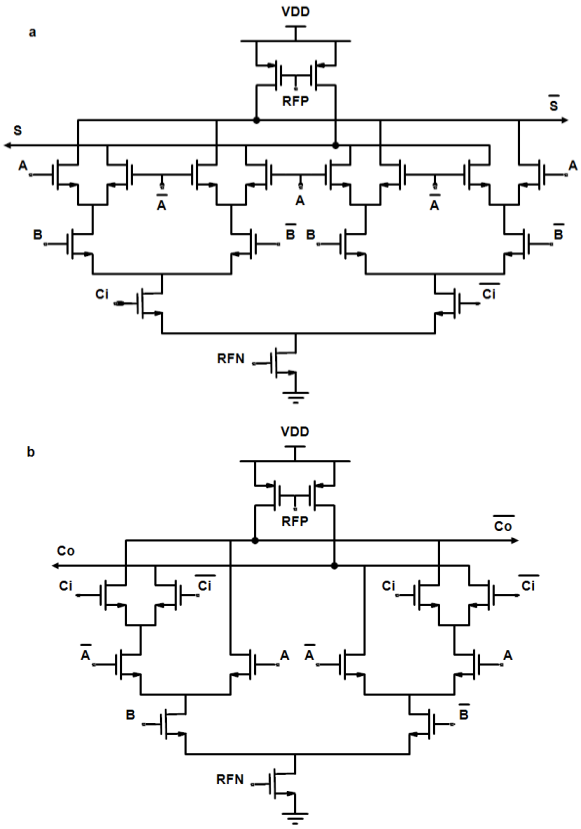

Fig. 10. The schematic structure of a 1-bit adder (a) Sum circuit (b) Carry circuit.

the carry out of each less significant full adder is the carry in of the succeeding full adder. In such a circuit, the equivalent output capacitances of the 1-bit adders are increased and give more validity to our results. It is apparent that the advantages of the GFET-based 4-bit adders in the delay, power and the other metrics are achievable as well (Tables III and IV). The delay of the G-CML adder also represents 40% improvement and the power has been reduced by about an order of magnitude when the CML designs are compared.

TABLE III
DELAY AND POWER OF THE SILICON-BASED STATIC AND CML ARITHMETIC CIRCUITS

Design style	Cell	Transistor counts	Delay [ps]	Power [nW]	PDP [nW × ps]	EDP [nW × ps^2]
Static	ADD	28	11	77.6923	854.6153	9400.768
	ADD4	112	69.5	251.962	17511.36	1217039
	Total Avg.	70	40.25	164.827	6634.287	267030
CML	ADD	30	5.25	7049.83	37011.61	194310.9
	ADD4	120	29	28156.7	816544.3	23679785
	Total Avg.	75	17.125	17603.2	301454.8	5162413

TABLE IV
DELAY AND POWER OF THE GRAPHENE-BASED STATIC AND CML ARITHMETIC CIRCUITS

Design style	Cell	Transistor counts	Delay [ps]	Power [nW]	PDP [nW × ps]	EDP [nW × ps^2]
Static	ADD	28	5.25	5.47113	28.72343	150.798
	ADD4	112	29	8.8	255.2	7400.8
	Total Avg.	70	17.125	7.13411	122.1716	2092.189
CML	ADD	30	1.075	1074.36	1154.937	1241.557
	ADD4	120	17.3	3163.2	54723.36	946714.1
	Total Avg.	75	9.1875	2118.78	19466.29	178846.6

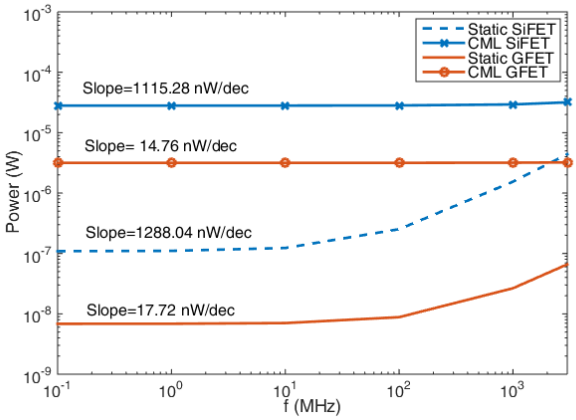

Fig. 11. Power versus frequency in a 4-bit adder for silicon and graphene technologies.

Fig. 11 shows the frequency analysis of a 4-bit adder when different design styles and circuit technologies are included. The power slopes of the static adders are more than those of the CML counterparts. This indicates that the CML designs have less sensitivity to frequency variations. Contrary to the results of the inverter shown in Fig. 9, the G-CML adder in comparison with the static SiFET-based adder outperforms the power consumption at higher frequencies. This is due to larger parasitic capacitances of the silicon-based technology leading to increase dynamic power dissipation. In other words, although static-based designs exploit the inherent privilege of lower power consumption, the circuit technology can reduce the amount of the power even for power-hungry CML designs when the complexity becomes larger.

CONCLUSION

This paper presents a technological approach for enhancing the performance by using GFETs instead of SiFETs. Two design styles namely static and CML have been studied. Standard gates such as inverter, AND, OR and XOR implemented with the GFETs demonstrate the preferable performance over those with SiFETs. A 4-bit adder consisting of four 1-bit adders in the both technologies and styles has been thought of as an arithmetic circuit. The PDP and EDP approximately have been reduced by up to about three orders of magnitude in the GFET-based 4-bit adder. Results reveal that complex G-CML designs are more appropriate for high-frequency applications due to less frequency dependence and power consumption in comparison with silicon technology. These advantages give rise to introduce capabilities of new emerging technologies for solving performance bottlenecks.

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