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Opto-Electronics Review 27 (2019) 291–297

Contents lists available at ScienceDirect

Opto-Electronics Review

journal homepage: http://www.journals.elsevier.com/opto-electronics review

Optical pulse monitoring unit for Free Space Optics

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ARTICLE INFO

Article history:
Received 22 July 2019
Received in revised form 26 August 2019
Accepted 3 September 2019
Available online 10 October 2019

Keywords:
Pulse amplitude monitoring unit
Peak detector
Sample and hold (S&H) circuit
Free space optical communications
Constant fraction discriminator

ABSTRACT

The paper presents a new construction of an optical pulse amplitude monitoring unit (PAMU) used in a transceiver of Free Space Optics. It consists of a buffer, constant fraction discriminator (CFD), delay line, and a sample and hold (S&H) circuit. In the design FSO system, the PAMU provides to monitor transmitted and received optical pulses with duration of few ns. Using this device, there is no need to apply complicated and expensive digitizing systems. The unique aspect of its construction is to control S&H circuit using the CFD. The lab model of this unit allows to perform tests to define some virtues of constant fraction and leading-edge discriminators. The results were implemented in optical signal monitoring of FSO system. The unit was prepared to cooperate with two different detection modules. Using this setup, it was possible, *e.g.* to determine operation characteristics of FSO transmitter, identify interruption of transmission, and control light power to provide high safety of work.

1. Introduction

The paper presents a pulse amplitude monitoring unit of nanosecond optical pulses based on a sample and hold (S&H) circuit triggered with a constant fraction discriminator (CFD). It was developed to work in both receiver and transmitter of Free Space Optics (FSO). An application of pulse monitoring provides a power control of infrared radiation pulses [1]. This power determines, *e.g.*, data link range, power consumption, or laser lifetime. Because of free space operation, the optical pulse monitoring makes it possible to identify interruption of transmission and control light power to ensure high safety of work currently, there are not any commercially available detection modules with integrated pulse monitoring function. Usually, this function is obtained separately using fast signal loggers based on FPGA and ADC technologies [2]. In contrast, the developed unit can be implemented in any optical detection module giving an extra dc signal output corresponding to the peak-pulse level. At the same time, it does not significantly increase complexity and costs of this module. In the design construction, the most important issue was to generate triggering signal for sample and hold operation. If there is an external synchronization signal, the triggering action is basic. However, in many applications such signal does not exist, and the triggering is performed basing on original input pules. To drive S&H circuit, threshold triggering (usually LED-Leading Edge Discrimination) or CFD can be applied. The first configuration is very simple, but obtained results depend on pulses shape (amplitude and rise time). This disadvantage does not exist in CFD operation. The designed device can be also used in many applications in which amplitude monitoring of diagnostic pulses is very important, *e.g.*, in medicine, environment protection, photobiology, security [3,4].

2. Free space optics with signal peak detection

Free Space Optics is a wireless communication technology in which, light is used to carry a signal. It can be a powerful alternative to the existing wireless technologies considering its high bandwidth, low cost and unregulated spectral operation. At the Institute of Optoelectronics, Military University of Technology (MUT), a special FSO device operated at the wavelength of 9.3 μm was design. In its construction, two different detection modules designed at the VIGO System company are used. The first one was applied in a receiving channel to register incoming light pulses. The scheme and view of this channel is presented in Fig. 1.

Using an off-axis parabolic mirror, light is directed into a detection module. The module output signal is processed using a signal conditioning unit (SCU) consisted of, *e.g.*, filters, ADC converter with automatic gain control unit (AGC), and a decoding processor. For analog control of the level of the received optical signal, a peak detection unit can be used. In this configuration, this unit must be designed to preserve the transparency of the connection between the detection module and its SCU. The second detection module is used in monitoring unit of emitted pulse power from the FSO transmitter. The scheme and view of this unit is shown in Fig. 2

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https://doi.org/10.1016/j.opelre.2019.09.001
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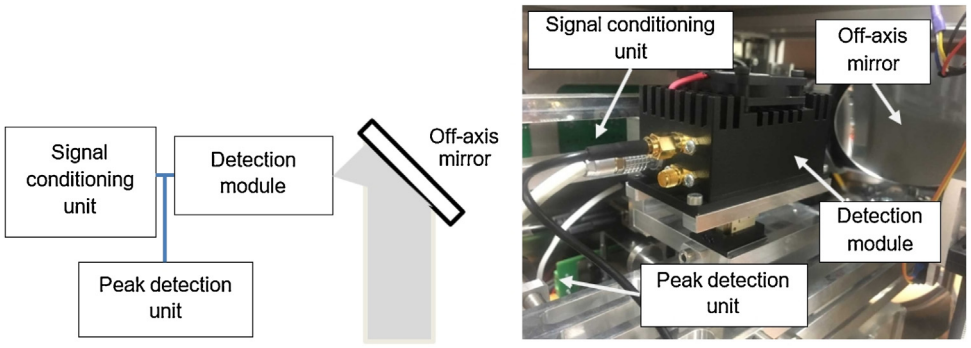

Fig. 1. Scheme and view of FSO receiving channel.

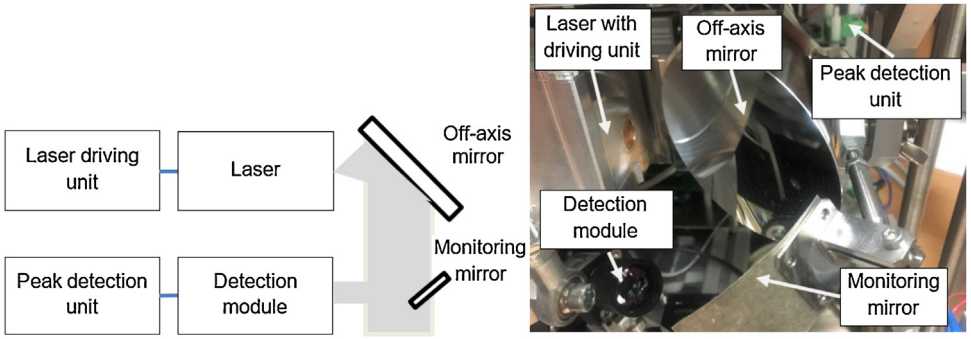

Fig. 2. Scheme and view of FSO transmitting channel.

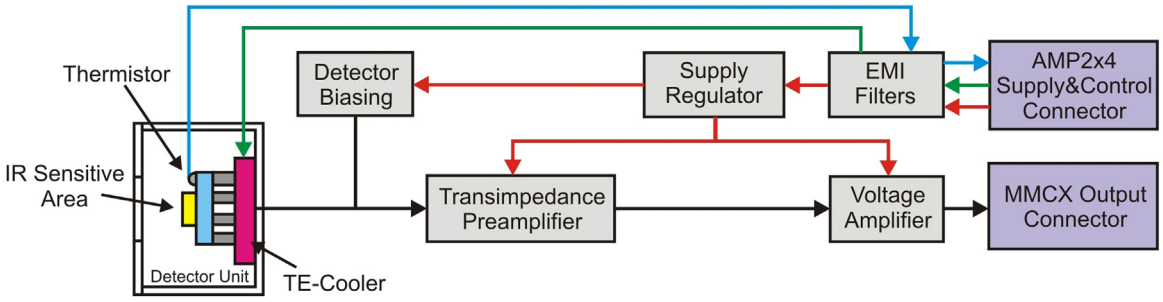

Fig. 3. Schematic diagram of the module electronic circuitry [https://vigo.com.pl/].

The part of the emitted light is reflected into the second detection module using an extra monitoring mirror. This mirror is placed in the cross section of the optical beam to get ca. 1% of the total pulse power. Its output signal is analyzed using the peak detector unit to determine the power of emitted optical pulses. Taking into account the described requirements for both kinds of detection modules, some special fast (FIP) and ultra-small (SIP) devices were developed and manufactured at the VIGO System company. The construction of these devices is common, and the difference is only due to the need for a thermoelectric cooling. This cooling is necessary for FIP modules to provide high level of detectivity. The module consists of a photodetector, a thermoelectric cooler with temperature sensor, and a two-stage amplifier (Fig. 3). The electronics provides optimized condition for the photodetector operation, *i.e.*, the constant voltage bias and current mode readout. The amplifier first stage is a transimpedance preamplifier (TIA) of a low input resistance based on OPA 847 Op-Amp, characterized by a low input noise voltage (0.85 nV/Hz$^{1/2}$) and a moderate input noise current (2.5 pA/Hz$^{1/2}$). The second stage is a ~20 dB voltage amplifier with 50 Ω output resistance.

In these modules, HgCdTe heterostructures obtained from low-temperature metal organic chemical vapor deposition epitaxy was applied. The detectivity of this photodiode was optimized for the LWIR spectral range (Fig. 4). To achieve the ultimate performances, a concept of a photodetector as a monolithic heterostructure chip with integrated optical, detection and electronic functions was implemented.

In construction of the FSO channels, the need to develop a pulse amplitude monitoring unit (PAMU) was also defined. It required to perform analyzes of some S&H circuits configurations with different triggering procedures. It was mainly taken into consideration well-known peak detection configuration based on Op-Amp charging memory capacity with a rectifying diode. It provided to define some significant limitations of these circuits resulting from currents in holding capacitor circuit (*e.g.*, Op-Amp buffer biasing current, diode reverse current). These currents cause discharge of the memory capacity. This phenomenon increases as the signal duty cycle decreases. For this reason, it was decided to use a specially developed PAMU device. Figure 5 shows a scheme of this device. It consists of a buffer, constant fraction discriminator

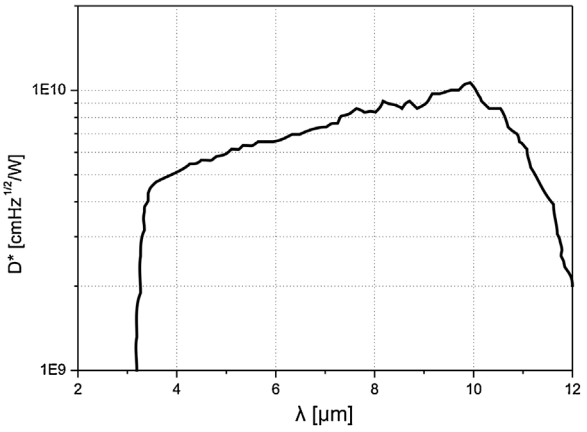

Fig. 4. Spectral detectivity of HgCdTe photodetector.

(CFD), delay line (DL), and a S&H circuit. The analyzed input signal is generated by detection modules [5–7].

The buffer input is adapted to the output impedance of detection modules (50 Ω). After impedance separation, the signal is fed to inputs of both the constant fraction discriminator and the delay line based on active all-pass filter. The discriminator develops a logic pulse to trigger S&H circuit (Sampling Operational Transconductance Amplifier - SOTA). At the same time, delayed pulses reach SOTA non-inverting input. The adjusted delay time provides to obtain full synchronization of both SOTA inputs signals. If there is time-shift, the PAMU works inaccurately. The measured pulse amplitude is underestimated relative to its real level. This is due to a too-short charging time of memory capacity. If the pulses are shifted more than their duty time, noise signal will appear on the output. Correct work of the PAMU provides to analyze dc signal with the level corresponding peak-pulse value [8,9]. In the design FSO, PPM-5 signal modulation with a frequency of 4 MHz and a pulse time duration of 16 ns is applied. These conditions determined a configuration of S&H circuit. The scheme diagram of this circuit is shown in Fig. 6.

To design this unit, OPA615 IC was applied. Its wide bandwidth and significantly shorter propagation time provide a peak detection of nanosecond pulses. This unit is built of SOTA amplifier, memory capacitor (C_m), and a buffer (OTA) [10–11]. It is triggered with the CFD unit. At the output of SOTA, a memory capacitor was used (capacity range from 47 pF to 1 nF). The amplifier is used with the buffer using common collector configuration. If the voltage at the positive input of SOTA is not equal to its negative input voltage and the logic state at the 'Hold control' pin is high, C_m capacitor is respectively charged or discharged. This process has been stopped if both SOTA inputs voltages are equal. This operation allows to monitor amplitude of input pulses.

The scheme diagram of the CFD unit is shown in Fig. 7. It was built using circuit idea described in Ref. [12] with additional logic level converter to obtain TTL signal output.

The input signal fed into two paths. The upper path is equipped with a signal attenuator built of resistor divider R_1&R_2 [13,14].

Application of blocking capacitor C_1 and of extra dc signal reduces the influence of noise and ringing phenomenon. In next step, the analyzed signal is fed to the non-inverting comparator input (MAX9601). This comparator is characterized by a very short signal propagation time of 500 ps. To its inverting input, the delayed pulses are connected. The delay time is achieved by using two cascaded Op-Amps, each forming a single-pole active all-pass filter. The obtained total time delay is expressed:

$$t_{GD} = n(2RC)$$

where, n – number of cascaded Op-Amps.

Due to the PECL (Positive Emitter Coupled Logic) standard of MAX9601 comparator outputs, it was necessary to apply conversion into TTL standard. It was provided by MC10ELT28 converter. Such prepared CFD output signal is fed to 'Hold control' input of S&H circuit.

Basing on the performed analyses, lab model of the PAMU unit was made. Using BUF602 buffers, input and output circuits were designed to match a source impedance of the analyzed signal (detection modules). The PAMU PCB design also provides operation in different configurations, *i.e.*, threshold triggering, full CFD with zero crossing detection, and CFD with additional biasing. It is also possible to place an inverting amplifier (*e.g.* OPA847) to operate with negative pulses.

3. Experimental results

3.1. Test of PAMU

The tests of the PAMU unit were performed basing on a measuring setup presented in Fig. 8. During the first test step, there were determined operation characteristics of a peak detector unit controlled by external triggering pulses. The function of controlled delay time between pulses built into generator was used to synchronize measured pulse signal with S/H trigger signal. In that way, errors caused by triggering procedure were minimized.

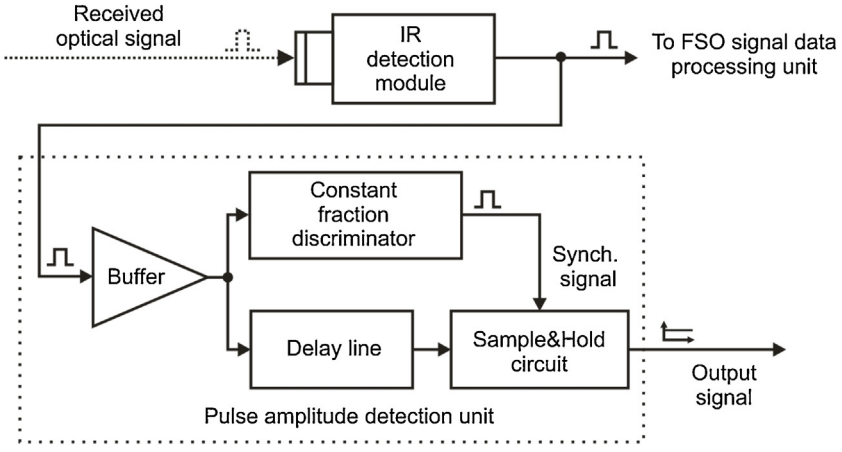

Fig. 5. Block diagram of PAMU device in FSO receiver.

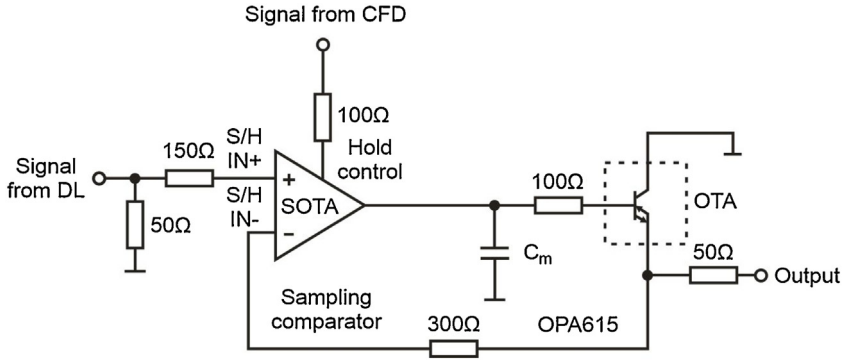

Fig. 6. Schematic diagram of the S&H circuit.

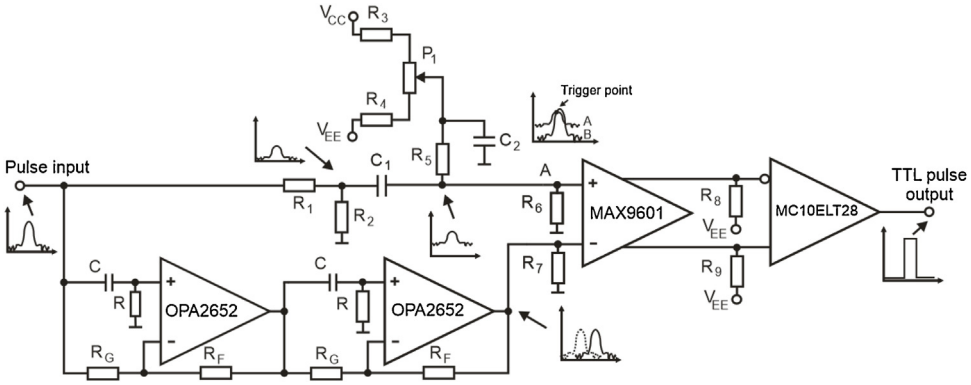

Fig. 7. Schematic diagram of the CFD circuit.

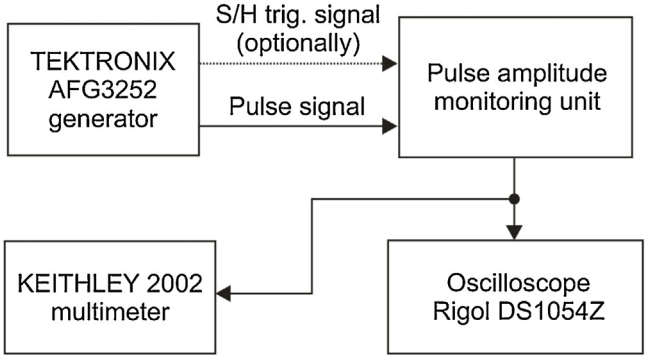

Fig. 8. Block diagram of measurement system.

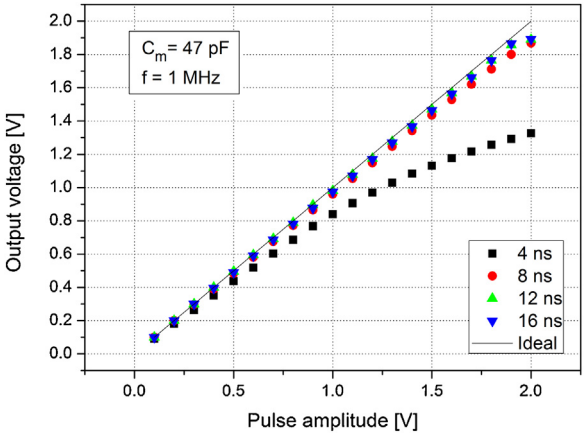

Fig. 9. Output voltage *vs.* pulse amplitude for different pulse widths.

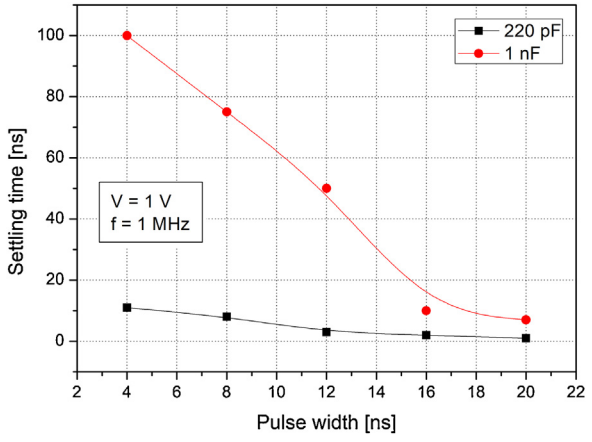

Fig. 10. Characteristics of peak detector settling time *vs.* time duration of input pulses.

In Fig. 9, an influence of amplitude and time duration of analyzed pulses on peak detector signal for $C_m = 47$ pF is presented. It was observed that the peak detector works correctly for pulses with time duration longer than 4 ns. These tests were performed for different values of C_m (also for 220 pF and 1 nF). However, the obtained results were very similar (the difference less than 5%).

The settling time of this peak detector was examined taking into account two memory capacitor values and pulse time duration (Fig. 10). Pulses of 1 MHz frequency and of 1 V amplitude were used. In the case of low value of the memory capacity (220 pF), there is no significant influence of pulse duration (in the range of 4 ns – 20 ns) on the settling time. However, if the capacity increases (up to 1 nF), the influence of pulse shape (its time duration) also growths.

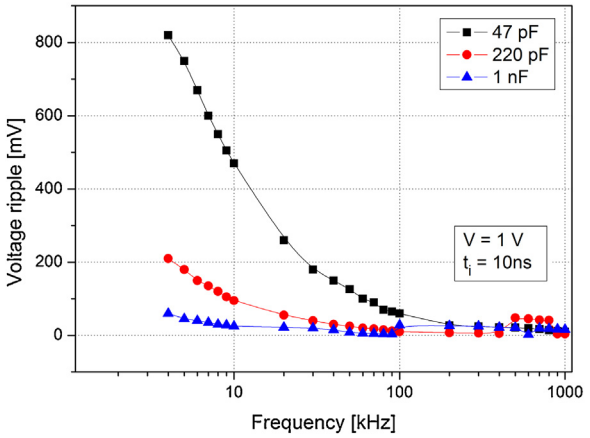

Fig. 11. Characteristics of the voltage drop between pulses (due to the discharging of the storage capacity) to a given input signal with an amplitude of 1 V and a duration of 10 ns.

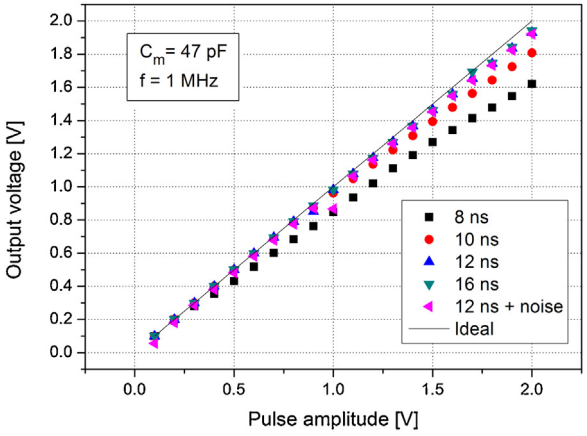

Fig. 12. Operation characteristics of peak detector with memory capacity of C_m = 47 pF and triggered with CFD for pulse signal (f = 1 MHz).

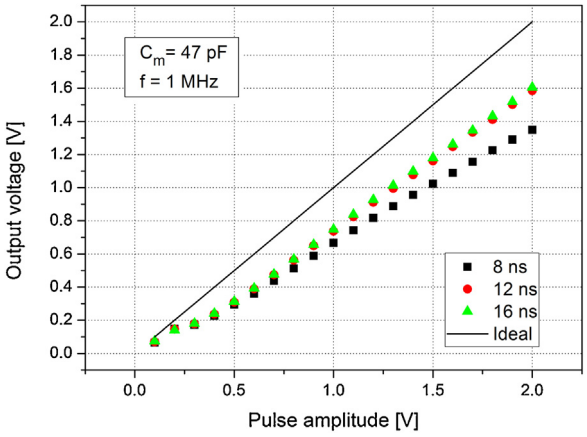

Fig. 13. Operating characteristics of the system for f = 1 MHz, C_m = 47 pF and triggering from the threshold discriminator.

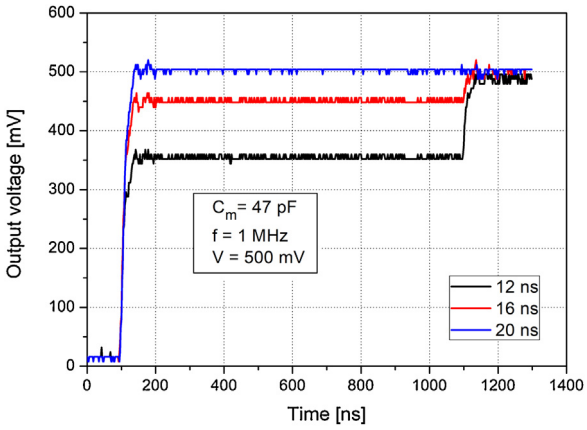

Fig. 14. Output peak detector signals for pulse of 500 mV amplitude, 1 MHz frequency, and 47 pF memory capacity *vs.* different pulse time durations.

These results require to test of the influence of pulse frequency and the memory capacity on peak detector output signal. There was noticed the decrease in the output voltage for pulses with low duty cycle. This is caused by discharge phenomenon of the memory capacity described in Section 2. However, it can be reduced using higher values of this capacity. In practice, the capacity selection also concerns analyzed response time of the unit. In the performed test, for pulses with few kHz frequency, 10 ns time duration, and the memory capacity of 47 pF, the detector output signal changes in the range of the true peak-pulse value to 0 V (Fig. 11).

The presented results were obtained using the external triggering signal. The design of the CFD provides to test the peak detector in real scenario. In that case, S&H circuit is triggered using analyzed input signal. It is normal mode of peak detector operation for both FSO receiver and FSO transmitter. The main issue of the performed tests was to verify the dependence of peak detector signal on the amplitude of input pulses. During that tests, the input pulse signal was also modified with 200 mV_{pp} Gaussian noise one. This modification was important considering the peak detector operation with real noisy signals. Such tests conditions were obtained using arbitrary waveform generator model Tektronix AFG3252. The reduction of noise influence is based on pulses level shift by adding offset. Then the comparator does not respond to voltages from noise sources. It was simply shown in signal sketch in Fig. 7. However, selecting of the additional DC offset voltage should be a compromise between minimizing the effect of noise influence and detecting signals with low amplitude. The results for different pulse time durations are shown in Fig. 12. For the pulse time duration of 12 ns, there is no different results obtained for both noisy and noise-free signals.

To define triggering performance of the CFD, the same measure of peak detector operation characteristics was made using threshold triggering. The results of that tests are presented in Fig. 13.

There is noticed significantly greater discrepancies between the ïdealc̈haracteristics compared to the CFD triggering one. This difference results from well-known error caused by discrimination procedure for which, time of trigger signal generation strictly depends on shape of the analyzed input signal. Usually the shape is described by its rise/fall edges and amplitude. Comparing the presented results, application of the CFD provides better triggering for S&H circuits.

The relationship between pulse time duration and peak detector settling time was also observed. It results from summarized time determined by number of pulses of a specific time duration needed to charge the memory capacity. This capacity is charged in gate time described by the triggering signal and analyzed input one.

Using the CFD, it is possible to generate output peak detector signal corresponding to the amplitude of the first pulse. However, this feature depends primarily on a time duration, amplitude of analyzed pulse, and hold capacity. During the tests, such a phenomenon was observed for input pulses with amplitude of 500 mV and time duration of 20 ns (Fig. 14). For shorter pulses (12 ns and 16 ns), settling time of the peak detector is determined by two-pulses time period. Figure 15 illustrates the registered signals during peak detector

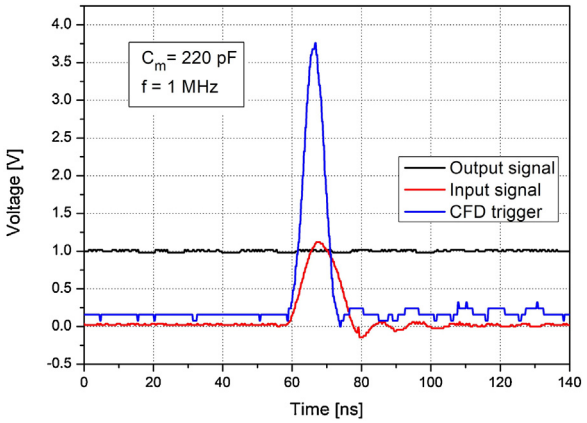

Fig. 15. Operation signals of peak detector triggered by CFD unit.

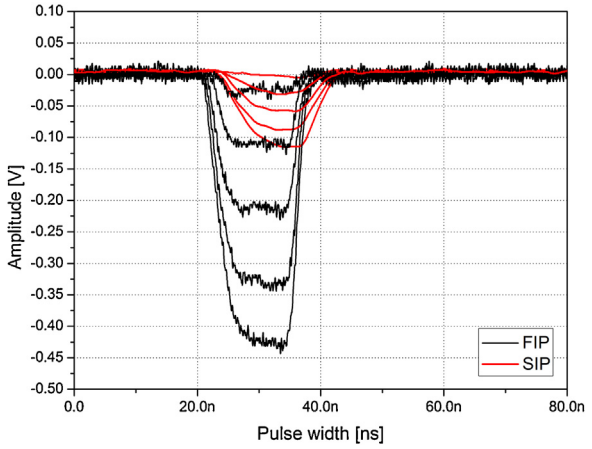

Fig. 16. Shape of registered optical pulses using FIP and SIP detection modules.

operation. There is observed full synchronization of analyzed input signal at the S&H circuit and triggering one generated by the CFD.

3.2. *PAMU test of optical peak power detection*

The preliminary test of the PAMU was performed using two detection modules: FIP to measure peak power of propagated light and SIP to monitor peak power of pulses generated by laser. The FIP module was directly irradiated by light pulses generated by quantum cascade lasers (QCL). In the case of the SIP module, there was applied an extra small flat mirror at the cross section of the lasers beam to direct some part of radiation into the module field of view. The output signals from these modules were given at the inputs of both oscilloscope and the PAMU. The arbitrary level of pulse power was determined basing on ADC conversion of the PAMU output signal. This conversion was performed applying a microcontroller with a special prepared software.

Figure 16 shows shape of optical pulses registered using both detection modules (FIP and SIP). There is observed higher noise influence for the FIP module. But this phenomenon results from its broader signal bandwidth. This can be also noticed comparing rise times of these signals.

The PAMU output signal was measured and recalculated into arbitrary power level. That provided to determine operational characteristics of QCL laser. The laser driver tunes light peak power by control of supplying voltage (laser biasing). In Fig. 17, examples of measured characteristics using FIP and SIP modules are presented.

The operational characteristics have the same shape. There is observed the same level of supply voltage threshold and voltage sensitivity. The correct work of the designed PAMU makes it possible to implement some automatic procedures for control of optical radiation power considering different kinds of operational scenarios.

4. Conclusions

The article presents a peak detector of *ns*-short pulses. It is a fully analog circuit in which, a special constant fraction discriminator is applied. This discriminator generates triggering signal for the S&H circuit built of a transconductance amplifier and a sampling comparator. The performed test confirmed the significant advantage of the designed configuration comparing threshold triggering technique. In addition, it demonstrates better work in the case of noisy signals. The performance of the designed peak detector unit was also analyzed changing the memory capacity and the parameters of the input signal. Particular attention should be paid to the selection of the memory capacity taking into account the settling time and operation with low duty cycle pulses. The developed PAMU is an effective tool for signal analysis and at the same time is competitive for currently used system operated with fast signal acquisition electronics.

Acknowledgement

This research was supported by The Polish National Centre for Research and Development grant DOB-BIO8/01/01/2016.

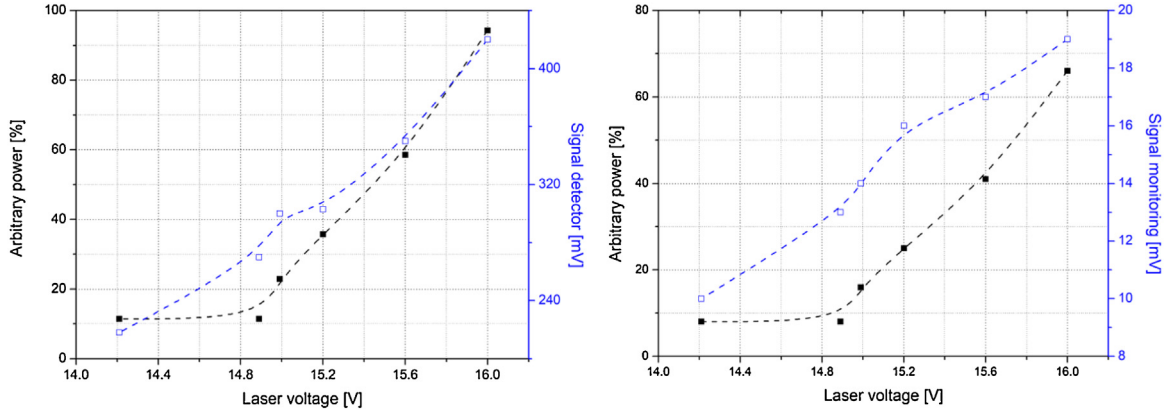

Fig. 17. Processing characteristics of QCL laser registered by detection modules with PAMU: FIP (a) and SIP (b).

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