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REVIEW OF PEAK SIGNAL DETECTION METHODS IN NANOSECOND PULSES MONITORING

Krzysztof Achtenberg, Janusz Mikołajczyk, Dariusz Szabra, Artur Prokopiuk, Zbigniew Bielecki

Military University of Technology, Institute of Optoelectronics, Gen. S. Kaliskiego 2 Str., 00-908 Warsaw, Poland
(✉ *krzysztof.achtenberg@wat.edu.pl*, +48 26 183 7523, *janusz.mikolajczyk@wat.edu.pl*, *dariusz.szabra@wat.edu.pl*, *artur.prokopiuk@wat.edu.pl*, *zbigniew.bielecki@wat.edu.pl*)

Abstract

The paper is a review of analog and digital electronics dedicated to monitor nanosecond pulses. Choosing the optimal peak detector construction depends on many factors for example precision, complexity, or costs. The work shows some virtues and limitations of selected peak detection methods, for example standard peak detector with rectifier, sample and hold circuit with triggering units and ADC fast acquisition. However, the main attention is paid to problems of results from effective triggering signal for sample and hold operation. The obtained results allow for designing a peak detector construction as an alternative for costly and very complex fast acquisition systems based on ADC and FPGA technologies.

Keywords: peak detection, pulse amplitude, free space optics, constant fraction discriminator, leading edge discriminator, sample and hold, ADC, fast acquisition.

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1. Introduction

Peak power detection of nanoseconds pulses is a very important issue in many technologies, *e.g.* medicine [1], spectroscopy [2–3], telecommunications, nuclear technology, security [4] or ultraprecise measurements of optical pulses [5–9]. For example, it enables to estimate the power of received signals [10–12]. In these applications, the main attention focus is on triggered circuits (*e.g.* sample and hold ones) or fast digitizing techniques. When compared with traditional methods using *e.g.* a rectifier, gated devices are more accurate, more resistant to interferences and to noise. The limited accuracy results from a high leakage current of diodes used in peak detection circuits, especially in the case of pulsed signals with a low duty cycle. The current discharges the capacitance lowering the voltage with the detected pulse level, proportionally. This problem leads to a loss in linearity and accuracy of peak detector operation. However, for gated circuits, some problems related to correcting trigger signal generation are very critical. In many cases, the signal shape and noise sources influence the correct operation of such circuits.

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2. Signal peak detection in optoelectronic technology

The performed analyses of peak detection of optical pulse have defined two kinds of technologies basing on digital or analog electronic circuits. The operation of these circuits is schematized in Fig. 1.

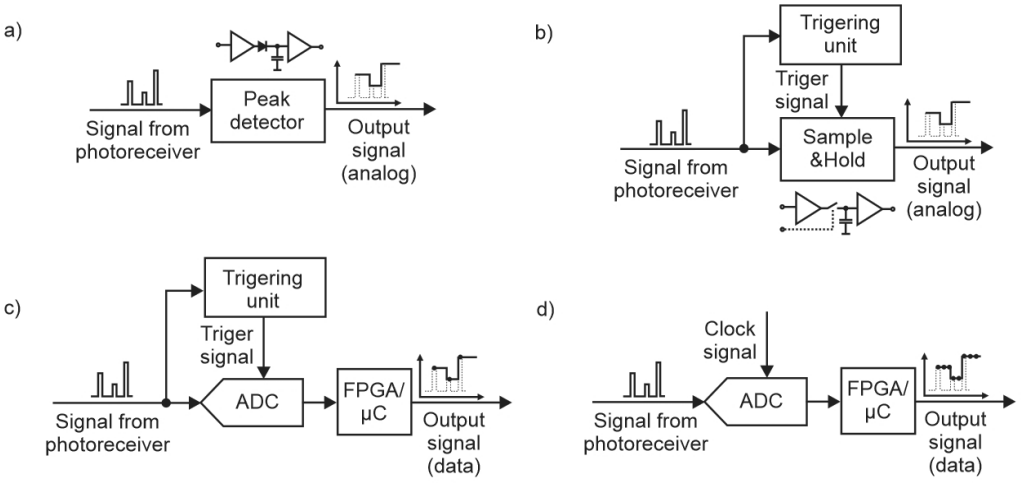

Fig. 1. Technologies of pulse peak detection: a) *standard peak detector* – SPD, b) *sample and hold peak detector* – SHPD, c) *triggered ADC peak detector* – TAPD, d) *fast clocked ADC peak detector* – FCAPD.

Figure 1a shows a block diagram of a *standard analog peak detector* (SPD). It is characterized by the simplest operation but its construction does not enable to detect the amplitude of nanosecond pulses. This is due to the mentioned leakage current of the rectifying diodes (reverse saturation current) as well as input current of the buffer. These currents rapidly discharge the memory capacity. To handle this problem, it is possible to apply the current steering method [13]. This method isolates the memory capacitor from quiescent current of a transconductance amplifier during the peak-hold cycle. The presented scheme of the *Sample and Hold Peak Detector* (SHPD – Fig. 1b) is more complex. A triggering unit is applied to determine the sampling procedure with *Sample and Hold* (S&H) device. The unit task is to develop an external triggering signal (usually the TTL standard) immediately with the analyzed signal. It is critical to synchronize the analyzed signal and the S&H operation. It can be achieved using *e.g.* a *Constant Fraction Discriminator* (CFD). The *triggered ADC peak detector* (TAPD) scheme (Fig. 1c) is similar to the SHPD with the difference of using an *Analog-to-Digital Converter* (ADC). The *fast-clocked ADC peak detector* FCAPD (Fig. 1d) uses the ADC as a signal recorder of the analyzed signal. The ADC clocking source provides a high sampling frequency. Appropriate algorithm implemented in *e.g.* FPGA is capable of analyzing nanosecond pulses. For these pulses, the sampling frequency is of the of order of a few hundreds of MHz, and even of a few GHz. This detector is the most expensive due to use high-costs elements such as ADC converters and FPGA chips. In literature, there are also described other methods of peak detection, *e.g.* the precision peak detector/full-wave rectifier of input sinusoidal signals using dual-output current conveyors or the 0.35 µm CMOS compact and accurate readout system with two-phase peak detector connected to multielement detectors and offset cancellation [14, 15]. Very interesting tool is real time peak detection technique with digitally set noise threshold eliminating noise sensitivity and providing high throughput [16].

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To achieve high resolution, another group of peak detection methods based on some correlation-function techniques are also applied [17].

2.1. A standard peak detector

A complete solution of the SPD circuit is presented in Fig. 2a. During its correct operation, the output signal is basically constant (with low fluctuations and low discharging of memory capacitance), that is why a "slow" ADC can be applied to read-out output signal in the case of digital processing. This configuration is simple but it has some limitations. These are related to the detection of short time or low duty cycle pulses. In this circuit, the output voltage is reduced by the diode voltage drop. This problem is solved in the circuit shown in Fig. 2b using an opamp feedback loop. However, the problem with diode reverse current is still critical. In Fig. 2c D_2 and R elements are added to keep opamp U_1 below the saturation level during reverse biasing of diode D_1. Resistor R limits the current of rectifier diode circuit D_2. The opamp response time is shorter since its output follows the input signal. This also keeps its output from quickly switching to its saturation limits when D_1 cuts off, thus minimizing the transient feedthrough to the memory capacitor via D_1. The applied diode should be characterized by a low reverse saturation current to minimize the leakage current in the reverse operation mode. Reduction of reverse biasing voltage causes a decrease in the diode reverse current. This can be done using the technique of bootstrapping (Fig. 2d) by adding D_3 diode and R_2 resistor. In the holding mode, V_{out} voltage follows the capacitor voltage and R_2 resistor applies this voltage potential to the D_3 diode anode to reduce its voltage to zero. D_1 diode blocks this node from the signal-varying output of opamp U_1 but its leakage is not critical for low values of R_2. When $C_h$is charging, R_2 isolates the diode node from the output of opamp U_2. That is why the need for special low-leakage diodes is not so critical. In the configurations presented in Fig. 2a–c, D_1 can be replaced using a JFET gate-source junction circuit. It typically has a lower leakage current than discrete diodes [18–21]. Some other applications of such circuits are also described in literature [22–23].

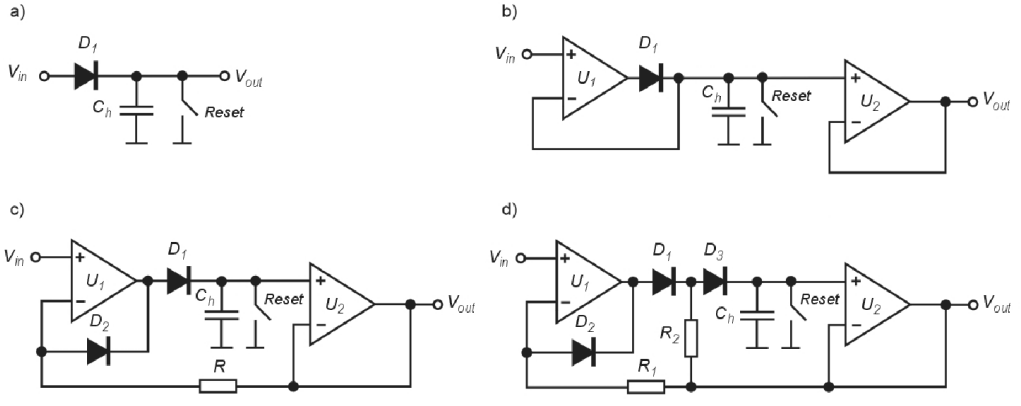

Fig. 2. Standard peak detector circuits.

The opamp selection for peak detector construction depends mainly on both output slew rate and output maximum current. The output voltage follows the input voltage changes with the rate of $dV_{in}/dt = I_{out,max}/C_h$ where $I_{out,max}$ is the maximum output current of opamp. In memory state, the output voltage drops with the rate of $dV_{out}/dt = I_B/C_h$ where I_B is the input bias current

of U_2 opamp. The value of C_h is the compromise between rates of both output voltage drop in memory state and this voltage growth during the charging of the capacitor. This capacitor should be also characterized by a low leakage (high insulation resistance) to minimize the discharge rate. It should be characterized by low dielectric absorption to retain 0 V until recharged by the input signal for the reset mode.

3. A peak detector with a Sample and Hold circuit

The fundamental element of the SHPD circuit is an opamp circuit operated with a switch S_w to control the sampling and hold device (Fig. 3). When this switch is closed, the capacitor C_h is charged up to the voltage level of pulses presented at the input of opamp U_1, The output voltage fluctuations depend on *e.g.* the memory capacitance C_m, signal dynamics and parameters of a buffer U_2 (its input bias current). Critical tasks to deal with in buffer construction are a low input bias current and a large output current recharging the memory capacitor. The switch-off mode causes the peak voltage to be held at the output of U_2 for the time determined by the C_h capacitance and leakage currents [24–27]. However, a design of the S&H device requires analyzing opamp parameters such as input offset voltage, gain error, bandwidth, slew rate, maximum output current, nonlinearity, aperture time. In the SHPD circuit, there is also observed an error resulting from the influence of the S&H control signal on the collected charge [28–31].

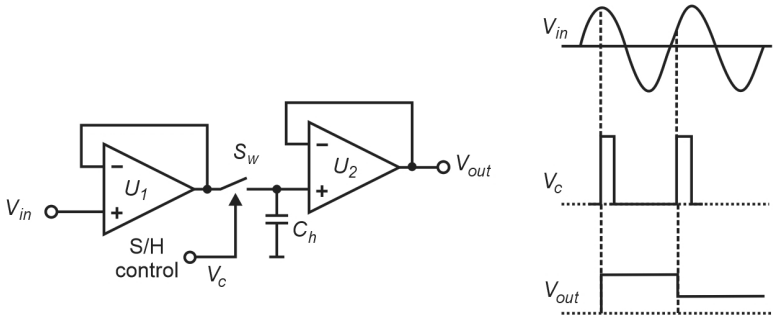

Fig. 3. SHPD peak detector with input-output waveforms.

The triggering signal (TTL/CMOS standards) is necessary for the correct operation of each S&H device. In many scenarios, this signal is not directly available and it is necessary to design an additional triggering unit. This unit produces a triggering signal synchronized in time with the analyzed one. This is a critical requirement (full synchronization of the trigger gate with the input pulse) for proper operation of the peak detection system. For this purpose, a triggering unit with leading edge discriminator or a constant fraction discriminator can be used.

3.1. Leading edge discrimination

In the *leading edge discriminator* (LED) (Fig. 4), a signal comparator is used. Its output signal is set to a high level (the value of the voltage supply) when the amplitude of the analyzed signal exceeds the threshold value determined by resistor divider. In this configuration, the generation of the trigger also depends on the shape of the analyzed signal, *e.g.* its rise time. This feature can be applied in fine matching of temporary synchronization.

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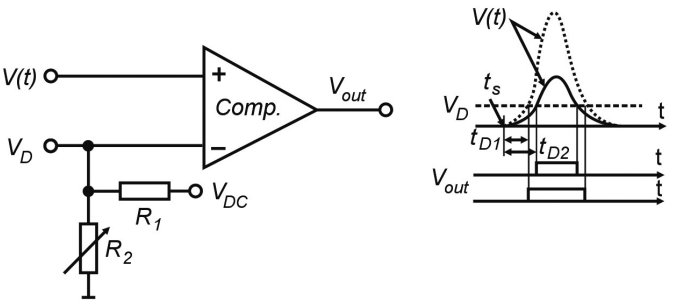

Fig. 4. Triggering system based on threshold comparison.

After the time matching (*e.g.* through a delay line), the S&H circuit is triggered. However, for this unit, there is a delay between the pulse rising edge and the triggering pulse generation. This delay is described as the *walk effect*. Due to this phenomenon, the moments of response (time from t_{event}) are different ($t_{trA} < t_{trB}$) (Fig. 5).

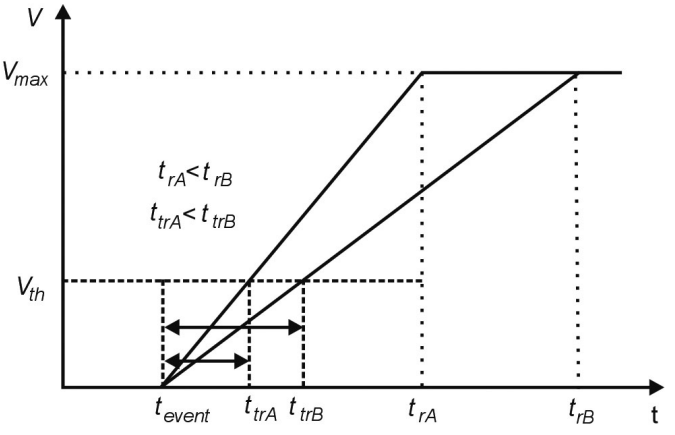

Fig. 5. Influence of rising time on response delay time of LED.

It can be expressed by:

$$t_{tr} = f(t_r)\Big|_{V_{max}=const}. \tag{1}$$

The influence of the shape of the input signal on the *walk effect* is expressed by its deterministic parameters. This phenomenon is responsible for *e.g.* the jitter effect. It is also determined by signal noises (from both the detector and the read-out electronics) as well as the stochastic process of signal generation in this detector. Figure 6 shows the impact of the noise signal on the jitter effect.

The solid line corresponds to "noiseless" pulse and noise envelope defines the standard deviation of σ_v. In terms of stochastic processes, uncertainty of the trigger time caused by the noise is expressed by the mean standard deviation σ_{tr}:

$$\sigma_{tr} = \frac{\sigma_V}{\dfrac{dV(t)}{dt}\Big|_{t_{tr}}}. \tag{2}$$

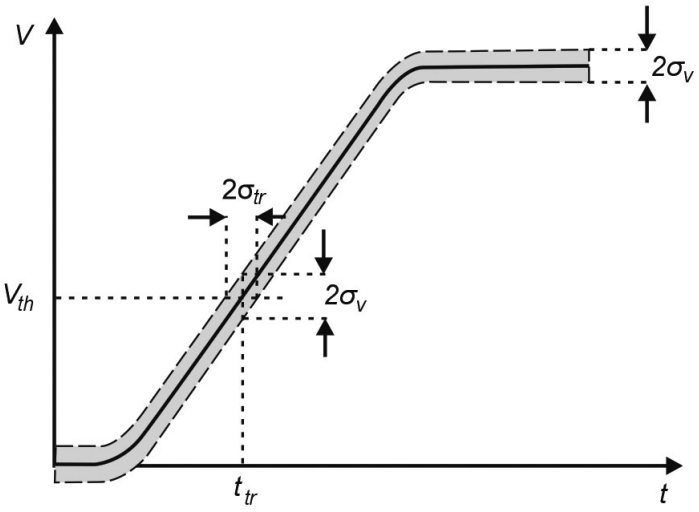

Fig. 6. Influence of noise on indeterminacy trigger time due to jitter effect.

3.2. Constant Fraction Discriminator – CFD

The block diagram of a CFD circuit is shown in Fig. 7. Only one comparator is used here. Its task is to determine the time intersection of an attenuated input signal with the time-delayed one. Thanks to this, the circuit defines a point with a constant time fraction in relation to the input signal (time of event occurrence), regardless of its amplitude. Its operation idea is presented in Fig. 7.

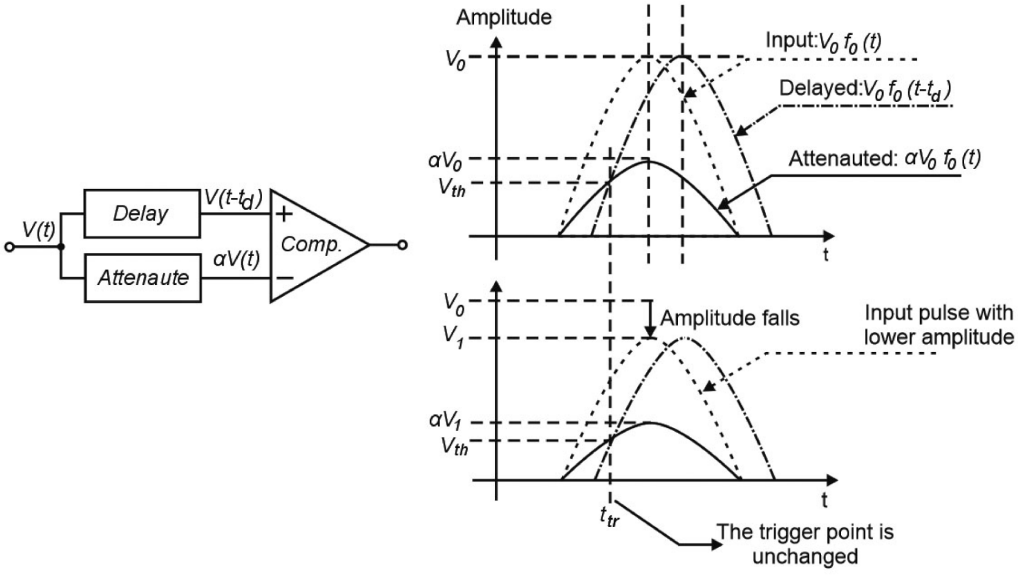

Fig. 7. Block diagram of a basic CFD and its operation idea [32].

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The time point of the signals' intersection t_T (trigger time) depends on the time delay t_d and the attenuation coefficient α However, there is no dependence related to the amplitude of the input signal. It could be analyzed determining the trigger factor p as:

$$p = \frac{V_{t_T}}{V_0} = \frac{V_o \cdot f_0(t_T)}{V_0} = \frac{f_0(t_T - t_d)}{\alpha}, \tag{3}$$

where: V_{t_T} – threshold voltage, f_0 – shape of the input signal, V_0 – signal amplitude, $f_0(t_T - t_d)$ – normalized coefficient of the delayed input signal.

The p value is constant and there is no component of the signal amplitude. The input signal is characterized by a specific value of the *signal to noise ratio* (SNR). To avoid false triggering signals from the CFD, a low bias voltage V_{DC} can be added. Finally, the trigger factor can be expressed as:

$$p = \frac{c_0\,(t_T - t_d) - \dfrac{V_{DC}}{V_0}}{\alpha}. \tag{4}$$

However, in this case the p value depends on the amplitude of the input signal. For this reason, the bias voltage should be as low as possible.

In Fig. 8 some solutions are shown aimed at minimizing the triggering error caused by the input signal noise. The first unit consists of a CFD discriminator and a LED one. The LED discriminator produces a triggering pulse when the input signal crosses a threshold level. It allows to minimize false triggering signals resulting from noise. Output signals from these discriminators are given at the input of the AND gate. In some applications, a flip-flop can be applied. The other circuit, with a zero crossing point detector, is also very effective and the idea of its operation was described in [33].

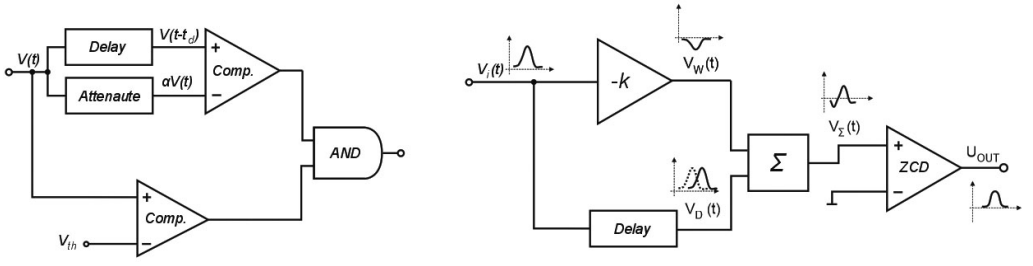

Fig. 8. CFD: with a threshold one (left) and with zero crossing detector (right), where $V_i(t)$ is the input signal, $V_w(t)$ is the inverted and attenuated signal, $V_d(t)$ is delayed signal, V_Σ is the summarized bipolar pulse.

4. Peak detection using the S/H method with a transconductance amplifier

Peak detection can be implemented using *operational transconductance amplifier* (OTA) to charge the memory capacitor (Fig. 9). This device amplifies the voltage difference of $V_{in} - V_{out}$. For $V_{out} < V_{in}$, the output current from the amplifier G charges the capacitor C with the diode D. If $V_{out} > V_{in}$, the diode is reversely biased so the voltage at this capacitor is unchanged. The function of the constant current source is to provide static operation for the OTA amplifiers. To detect very short pulses, the OTA peak detector should be characterized by a short response time, high droop rate and high bandwidth. It is also recommended to use a trigger signal if the OTA is equipped with an S&H function. It reduces leakage currents discharging capacitor C. There

are some integrated circuits (IC) equipped with the S/H function available on the market. These devices are called SOTAs (Sampling Operational Transconductance Amplifiers), *e.g.* OPA615. The S/H signal can be generated by a CFD or LED discriminator [34–37]. When the S/H signal is applied, the use of the diode is not required.

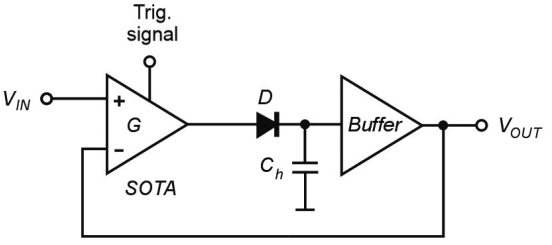

Fig. 9. Peak detector with SOTA amplifier.

For forward biased diode D, the output voltage V_{out} is given by:

$$V_{\text{out}} = \frac{1}{C} \int i \, \mathrm{d}t, \tag{5}$$

where $i = g(V_{\text{in}} - V_{\text{out}})$, and g is transconductance of the amplifier G.

5. Peak detection using sampling by an ADC

5.1. Fast constant sampling

Theoretically, the simplest method to detect a peak pulse is signal sampling (Fig. 1d). However, for short pulses, a high sampling frequency is required. Figure 10 shows sampling processes of three pulsed signals. The shape of the signal presented in Fig. 10(A) reflects an ideal situation in which the pulse is flat with duration time several times longer than the sampling period. Figure 10(B) presents a pulse signal with ringing and overshoot effects. In this case, it is possible to record a sample with different amplitudes. However, it distorts the measurements. For very

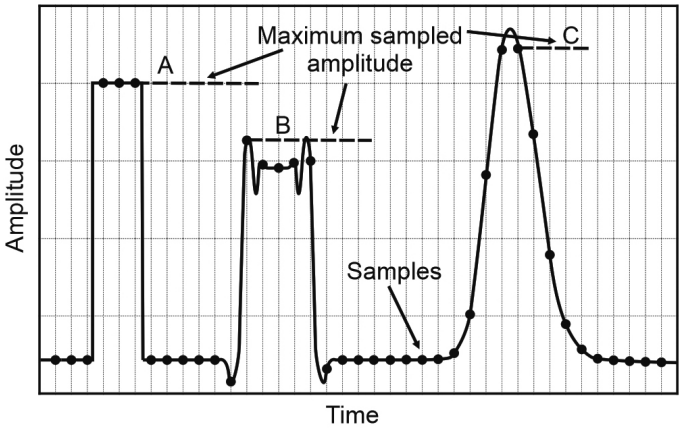

Fig. 10. Operation of peak a detector with fast signal sampling.

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short Gaussian pulses, it is difficult to record a sample at the peak signal (Fig. 10(C)). There is a need to use the high sampling rate to obtain enough samples [38–43]. As a result, the peak detector will work correctly with a hard-defined error or amplitude underestimation, respectively.

5.2. Sampling with triggering

To detect signal amplitude, it also possible to use a low ADC converter. In this method, a peak detector should be developed using a triggering system to generate an ADC trigger/clock signal. This can be applied using *e.g.* a LED or CFD discriminator. The diagram of these devices is presented in Fig. 1c. For this method, it is important to synchronize the input signal and the triggering one to accurately detect signal amplitude (Fig. 11). The ADC converter samples an input signal after the time of t_d (usually called the aperture delay time). This method uses the Sample & Hold circuit built in the ADC chip.

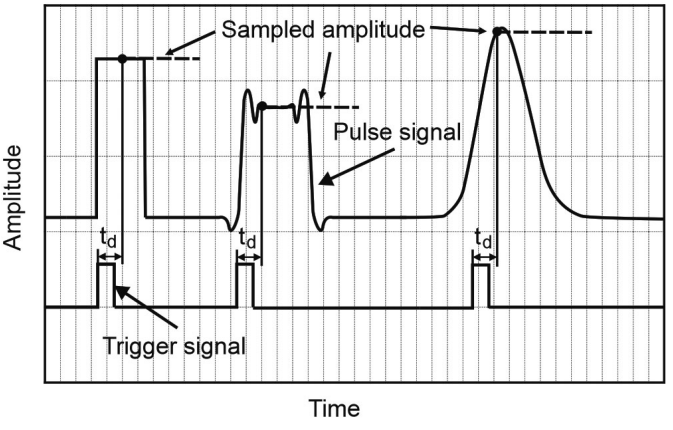

Fig. 11. Operation of the peak detector with an ADC low sampling frequency converter.

5.3. Peak detection using the method with an emitter-coupled logic output comparator

Some different peak detection methods were described by Krehlik and Śliwczyński in Design Ideas (Fig. 12) [44]. For example, a fast comparator (U_1) is used with an *emitter-coupled logic* (ECL) as a capacitor charger. It charges the capacitance C_1 and works as a peak detector. The U_2

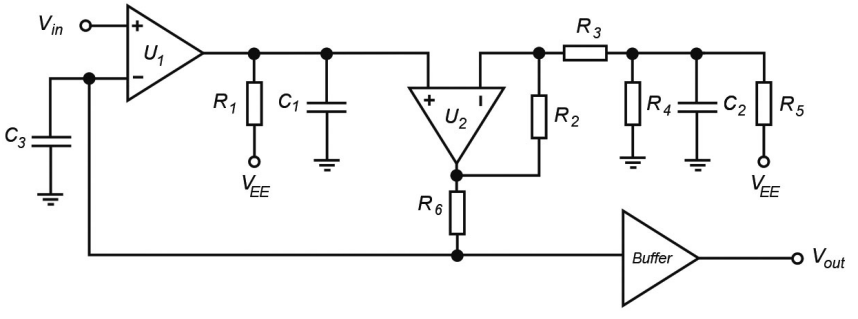

Fig. 12. Fast peak detector with an ECL comparator.

opamp compensates a voltage shift by the ECL comparator outputs to provide the same voltage level at its inputs. The output stage is a voltage follower built with the use of the opamp buffer. Using an ultra-fast comparator, this circuit can detect pulses with time duration of even a few nanoseconds.

6. Simulation results

In the first step of analysis, the operation of an SPD circuit was simulated using the SPICE software. For this purpose, a circuit with MOS input opamps with (for low bias current) and a memory capacitor of 100 pF was constructed. Figure 13 shows the SPD output signal (thick line) registered for input pulses with positive polarity. A significant error can be noticed in the pulse amplitude measurement.

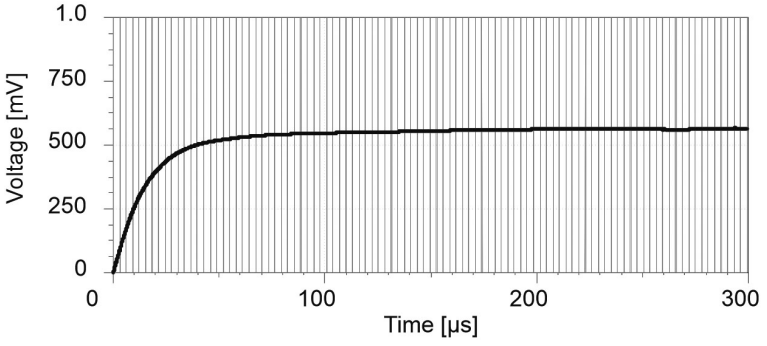

Fig. 13. Simulation results of a standard peak detector
(for pulse parameters of: 50 ns time duration, 3 µs period, 1 V amplitude).

In the next step, characteristics of output voltage versus pulse width from 10 ns to 80 ns were tested. For very short pulses, the measure error was very high. However, increasing the pulse duration reduced that error (Fig. 14). For pulse width of 80 ns, this error was less than one percent.

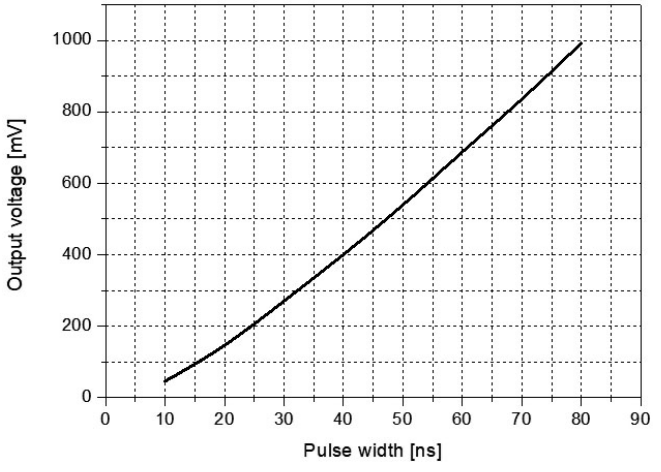

Fig. 14. Peak detector signal versus pulse time duration.

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To show the difference between SPD and S&H circuits, some simulations with the SOTA device (OPA615) were made for pulses with 1 V amplitude, 10 ns time duration and 250 ns period. In these circuits, the same memory capacitors of 100 pF were used. The results are shown in Fig. 15. The correct operation of the S&H circuit is observed for pulses with time duration of even about 10 ns.

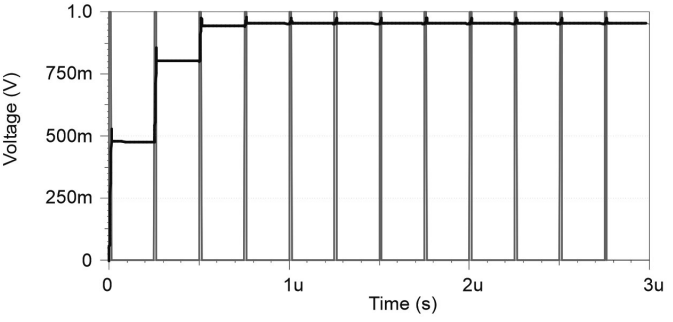

Fig. 15. Simulation results of a peak detector with SOTA.

7. Our work

7.1. A peak detector with an ECL comparator to monitor light pulses

A pulse monitoring unit with an emitter-coupled logic output comparator based on the circuit presented in Section 5.3 was built of a two-sided PCB circuit with 50 Ω impedance matching the detection module, model AIP-10k-200M produced by the *VIGO System S.A*. This setup was described by the authors in [45]. Using this setup, laser pulses at the wavelength of 9.3 μm with the frequency of 4 MHz, time duration of 16 ns and 400 mW peak power were detected. The light pulse shape and output signal of the developed monitoring unit were recorded using a DSA 70404 digital analyzer (Fig. 16). The levels of both signals are basically comparable and the differences are less than 5%.

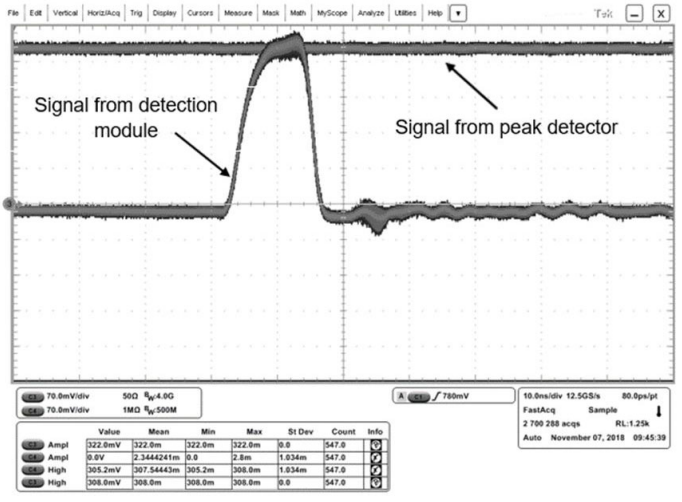

Fig. 16. Pulse shape registered with detection module and output signal from the monitoring unit [45].

There is a linear dependence observed between the amplitude of input pulses and the output signal level with the adjustment R-squared value of 0.9996. The determined linear coefficient is 1.04 and the estimated processing error of the monitoring unit is at the level of approx. 4%.

7.2. A peak detector based on the S/H and a CFD

The block diagram of the built CFD circuit is shown in Fig. 17. The proposed method has been implemented to verify the dependence of the peak detector signal on the amplitude of input pulses. These pulses were modified with a 200 mV_{pp} Gaussian noise signal using a Tektronix AFG3252 generator. Fig. 18 presents the peak detector response for different pulse time durations. This circuit allows to monitor pulses with time duration above of 8 ns. For such time duration, the error is high, *i.e.* about 20%. However, it decreases quickly for longer pulses. For example, the error decreases to the value of 5% for 12 ns pulses. There is also observed a lower influence of the noise signal.

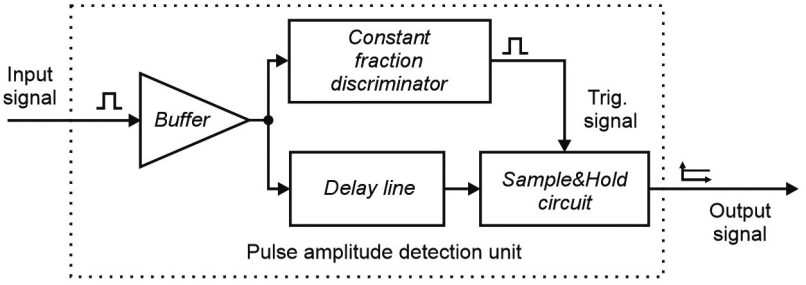

Fig. 17. Block diagram of an S/H peak detector controlled by a CFD.

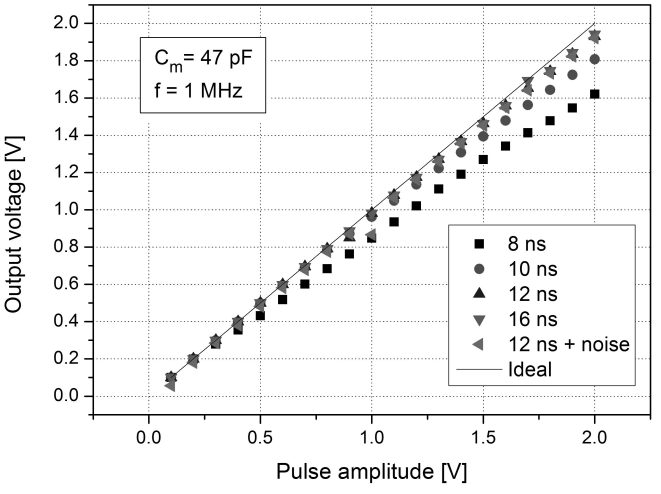

Fig. 18. Operation characteristics of peak detector triggered with CFD (for Cm = 47 pF f = 1 MHz) [46].

Summarizing, the performances of some peak detection methods are listed in Table 1. The typical (standard) peak detectors are characterized by simple construction but it is difficult to

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achieve correct amplitude estimation for nanosecond pulses. In the case of long-time pulses, they are accurate and resistant to noise. For precision estimation of nanosecond pulses the S&H method can be used to synchronize operation and hold the accumulated voltage. The transconductance amplifier PD (in SOTA PD) is useful for fast memory capacity charging. Another approach uses digital data acquisition with an ADC. It is possible to obtain very high precision of amplitude estimation but in the case of nanosecond pulses it needs a very high sample rate or accurate synchronization of input pulses.

Table 1. Dimensions of a bowtie patch antenna (mm).

Peak detection Technology	Pulse duration Example	Noise resistance	Complexity	Costs	Precision
Typical analog PD	min. 300 ns [12][1] 10 ns to 250 ns [13][2] 65 ns [18][3]	high	low	low	medium/high
Sample and Hold PD	500 ns [27][4] 1 µs [24][5] [29][6] min. 8 ns [46][7]	high	medium	medium	medium/high
SOTA PD	100 ns [36][8] 20 ns [37][9]	high	medium	medium	medium/high
Fast ADC acquisition PD	50 kHz [42]	medium	high	high	high
Triggered ADC PD		medium	medium	medium	high

[1] 4 V of amplitude and the highest value of repetition rate equal to 1 ms
[2] in this range the output voltage dependency was ±5%, the specific compensation of capacitor discharging current was used
[3] for pulses with time duration higher than 65 ns the detector error is lower than 5%
[4] for 200 mV of amplitude and 1 µs repetition rate and 5 V the supply error is 1%
[5] the voltage drop is about 2.16 µV/µs and the voltage error less than 0.5 mV
[6] designed for an ASK receiver (860 kHz)
[7] S&H triggered by a CFD, pulse duration vs. error dependency (above 12 ns pulse time duration, error less than 5%)
[8] repetition frequency 20 kHz, voltage drop 25 mV/µs
[9] pulse width extended to 200 ns in the circuit, voltage drop 5.7 mV/s

8. Conclusions

The paper presents a review of several peak pulse detection methods. These methods can be applied in optical detection modules to analyze the level of light pulses. The main attention was paid to peak detection of ultra-short pulses (with duration of a few *ns*). For S&H circuits, some analyzes of various signal triggering circuits are described. The influence of signal noise on peak detection errors was also discussed. There are identified some advantages of the CFD circuit considering commercial solutions or other triggering methods. The paper is a guide to select the best peak detector construction considering *e.g. size, weight and power* (SWaP) requirements. As was shown, the S&H circuit is a very effective tool to operate with short pulses ($t_i \approx 10$ ns). Under the same conditions, a standard peak detector demonstrates a significant error which is not acceptable in many applications.

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References

[1] Stacewicz, T., Bielecki, Z., Wojtas, J., Magryta, P., Mikolajczyk, J., Szabra, D. (2016). Detection of disease markers in human breath with laser absorption spectroscopy. *Opto-electronics Review*, 24(2), 82–94.

[2] Wojtas, J., Bielecki, Z., Stacewicz, T., Mikolajczyk, J., Mędrzycki, R., Rutecka, B. (2011). Application of Quantum Cascade Lasers in Nitric Oxide and Nitrous Oxide Detection. *Acta Physica Polonica A*, 120(4), 794–797.

[3] Stacewicz, T., Wojtas, J., Bielecki, Z., Nowakowski, M., Mikolajczyk, J., Mędrzycki, R., Rutecka, B. (2012). Cavity ring down spectroscopy: detection of trace amounts of substance. *Opto-electronics Review*, 20(1), 53–60.

[4] Wojtas, J., Stacewicz, T., Bielecki, Z., Rutecka, B., Mędrzycki, R., Mikolajczyk, J. (2013). Towards optoelectronic detection of explosives. *Opto-electronics Review*, 21(2), 210–219.

[5] Rogalski, A., Bielecki, Z., Mikolajczyk, J. (2017). Detection of optical radiation. Dakin, J.P., Brown R. (eds.). *Handbook of Optoelectronics: Concepts, Devices, and Techniques*. Boca Raton: CRC Press, 65–124.

[6] Mikolajczyk, J., Bielecki, Z., Bugajski, M., Piotrowski, J., Wojtas, J., Gawron, W., Szabra, D. (2017). Analysis of free-space optics development. *Metrology and Measurement Systems*, 24(4), 653–674.

[7] Bardelli, L., Poggi, G. (2006). Digital-sampling systems in high-resolution and wide dynamic-range energy measurements: Comparison with peak sensing ADCs. *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, 560(2), 517–523.

[8] Henniger, H., Wilfert, O. (2010). An Introduction to Free-space Optical Communications. *Radioengenineering*, 19(2), 203–212.

[9] Graeme, J., (1995). *Photodiode Amplifiers OP AMP Solutions*. New York: McGraw-Hill Education.

[10] Brillant, A. (2008). Laser Power and Temperature Control Loops. *Digital and Analog Fiber Optic Communications for CATV and FTTx Applications*. Bellingham: SPIE, 591–625.

[11] Barna, A., Bohus, J. (2015). Active stabilization of the beam pointing of a high-power KrF laser system. *Metrology and Measurement Systems*, 22(1), 165–172.

[12] Barna, A., Földes, I.B., Gingl, Z., Mingesz, R. (2013). Compact energy measuring system for short pulse lasers. *Metrology and Measurement Systems*, 20(2), 183–190.

[13] Haas, W., Dullenkopf, P. (1986). Novel Peak Amplitude and Time Detector for Narrow Pulse Signals. *IEEE Transactions on Instrumentation and Measurement*, IM-35(4), 547–550.

[14] Petrovi, P.B. (2013). A New Precision Peak Detector/Full-Wave Rectifier. *Journal of Signal and Information Processing*, 4(1), 72–81.

[15] De Geronimo, G., Kandasamy, A., O'Connor, P. (2002). Analog peak detector and derandomizer for high-rate spectroscopy. *IEEE Transactions on Nuclear Science*, 49(4), 1769–1773.

[16] Jordanov, V.T., Hall, D.L., Kastner, M. (2002). Digital Peak Detector with Noise Threshold. *Proc. of IEEE Nuclear Science Symposium and Medical Imaging Conference*, 1, 140–142.

[17] Jordan, J.R., Manook, B.A. (1981). Correlation-Function Peak Detector. *IEE Proceedings E – Computers and Digital Techniques*, 128(2), 74–78.

[18] Wright, J. (1992). Peak Detectors Gain in Speed and Performance. *Linear Technology Design Note 61*.

[19] Bhagat, S. (2015). High Speed Peak Detection. *International Journal of Engineering Research and General Science*, 3(6), 442–446.

Metrol. Meas. Syst., Vol. 27 (2020), No. 2, pp. 203–218
DOI: 10.24425/mms.2020.132770

[20] Dlugosz, R., Iniewski, K. (2007). High-precision analogue peak detector for X-ray imaging applications. *Electronics Letters*, 43(8), 440–441.

[21] Feucht, D.L. (1990). *Handbook of Analog Circuit Design*. Academic Press.

[22] Meyer, R.G. (1995). Low-Power Monolithic RF Peak Detector Analysis. *IEEE Journal of Solid-State Circuits*, 32(1), 65–67.

[23] Jayaraman, K., Khan, Q.A., Chiang, P., Chi, B. (2009). Design and analysis of 1-60 GHz, RF CMOS peak detectors for LNA calibration. *Proc. International Symposium on VLSI Design, Automation and Test*, 311–314.

[24] Pelgrom M. (2013). *Analog-to-Digital Conversion*. New York: Springer-Verlag, 155–174.

[25] Cheuk, J., Wong, W. (2001). *CMOS Sample-and-Hold Circuits ECE 1352 Reading Assignment*. Toronto: University of Toronto.

[26] Buckens, P., Veatch, M. (1992). A High Performance Peak-Detect & Hold Circuit for Pulse Height Analysis. *IEEE Transactions on Nuclear Science*, 39(4), 753–757.

[27] Kruiskamp, M., Leenaerts, D. (1994). A CMOS Peak Detect Sample and Hold Circuit. *IEEE Transactions on Nuclear Science*, 41(1), 295–298.

[28] Chow, H., Hor, Z. (2008). A High Performance Peak Detector Sample and Hold Circuit for Detecting Power Supply Noise. *Proc. of APCCAS 2008 – 2008 IEEE Asia Pacific Conference on Circuits and Systems*, 672–675.

[29] Chow, H.C., Wang, I.H. (2002). High performance automatic gain control circuit using a S/H peak-detector for ASK receiver. *Proc. of the 9th IEEE International Conference on Electronics, Circuits and Systems*, 2, 429-432.

[30] Mandal, S., Dasgupta, S. (2018). Modified CMOS Peak Detector and Sample Hold Circuit for Biomedical Applications. *Proc. of IEEE Conference on Emerging Devices and Smart Systems*, 113–116.

[31] Gupta, S.K., Hayashi, Y., Jain, A., Karthikeyan, S., Kawakami, S., Ravindran, K.C., Tonwar, S.C. (2005). A high-performance, low-cost, leading edge discriminator. *Pramana – Journal of Physics*, 65(2), 273–283.

[32] Zheng, R., Wu, G. (2012). Constant fraction discriminator in pulsed time-of-flight laser rangefinding. *Frontiers of Optoelectronics*, 5(2), 182–186.

[33] Zhao, P., Yao, P., Wang, X., Tu, B., Zhang Y. (2015). A high performance constant fraction discriminator for pulsed laser proximity fuze. *Proc. of Conferences of the Photoelectronic Technology Committee of the Chinese Society of Astronautics, Part II*, 9522.

[34] Costin, D.A.N., Opris, P. (1995). High speed peak detector for glitch-catching used in digital storage scopes. *Proc. of IEEE International Semiconductor Conference*, 233–236.

[35] Li, X., Wang, H., Yang, B., Huyan, J., Xu, L. (2017). Influence of time-pickoff circuit parameters on LiDAR range precision. *Sensors (Switzerland)*, 17(10).

[36] Hao, L., Zhang, Y., Na, Y., (2013). Research on amplification and peak-holding circuits of nanosecond light pulse. *Proc. of Sixth International Symposium on Precision Mechanical Measurements*, 8916.

[37] Zhang, W., Zhang, H., Zhang, X., Chen, Y. (2016). Laser pulse peak holding circuit for low cost laser tracking applications. *Advanced Laser Manufacturing Technology*, 10153.

[38] Dabas, A., Grover, K. (2018). Peak Detector using Low Voltage Operational Transresistance Amplifier. *International Journal of Engineering Trends and Technology*, 58(3), 109–112.

[39] Takahashi, H., Kodama, S., Kawarabayashi, J., Iguchi, T., Nakazawa, M. (1993). A new pulse height analysis system based on fast ADC digitizing technique. *IEEE Transactions on Nuclear Science*. 40(4), 626–629.

[40] Bidégaray-Fesquet, B., Fesquet, L. (2016). Levels, peaks, slopes. . . which sampling for which purpose?. *Proc. of the 2nd Second International Conference on Event-based Control, Communication, and Signal Processing*, 1–6.

[41] Singhai, P., Roy, A., Dhara, P., Chatterjee, S. (2012). Digital pulse processing techniques for high resolution amplitude measurement of radiation detector. *Proc. of the 9th International Workshop on Personal Computers and Particle Accelerator Controls*, 279–281.

[42] Wang, P., Wang, Z. (2011). Improvement of peak detection for digital storage oscilloscope. *Proc. of the IEEE 10th International Conference on Electronic Measurement & Instruments*, 222–225.

[43] Zet, C., Catalin, D., Fosalau, C. (2005). An FPGA Based Peak Detector for Magnetostrictive Current Sensors. *Proc. of the 14th Symposium on New Technologies in Measurement and Instrumentation and 10th Workshop on ADC Modelling and Testing*, 179–182.

[44] Krehlik, P., Śliwczyński, Ł. (2002). High-speed peak detector uses ECL comparator. *EDN – Design Ideas*, 47(21), 98–100.

[45] Achtenberg, K., Mikołajczyk, J., Szabra, D., Prokopiuk, A., Bielecki, Z. (2019). Peak detection unit for Free-Space-Optics receiver. *Metrology and Measurement Systems*, 26(2), 377–385.

[46] Achtenberg, K., Mikołajczyk, J., Szabra, D., Prokopiuk, A., Bielecki, Z. (2019). Optical pulse monitoring unit for Free Space Optics. *Opto-Electronics Review*, 27(3), 291–297.