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Performance evaluation of ZVS/ZCS high efficiency AC/DC converter for high power applications

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Abstract. The increased power density, reduced switching losses with minimum electromagnetic interference (EMI), and high efficiency are essential requirements of power converters. To achieve these characteristics, soft power converters employing soft switching techniques are indispensable. In this paper, a ZCS/ZVS PWM AC/DC converter topology has been emphasized, which finds applications in high power systems such as automobile battery charging and renewable energy systems. This converter scheme maintains zero current and zero voltage switching conditions at turn on and turn off moments of semiconductor switches, respectively and soft operation of rectifier diodes that lead to negligible switching and diode reverse recovery losses. Moreover, it improves power quality and presents high input power factor, low total harmonic distortion of the input current (THD_I) and improved efficiency. The validity of theoretical analysis of the proposed converter has been carried out experimentally on a 10 kW laboratory prototype. Experimental results prove that the soft switching operation of the semiconductor switches and diodes is maintained at 98.6% rated load efficiency. In addition, the performance evaluation has been performed by comparative analysis of the proposed converter with some prior art high power AC/DC converters. Efficiencies of the proposed and prior art high power topologies have been determined for different load conditions. The highest efficiency, power factor and lower THD_I of the proposed converter topology complies with international standards.

Key words: switching loss, zero current switching, zero voltage switching, power quality, reverse recovery loss.

1. Introduction

Nowadays, efficient high power front-end rectifiers are in high demand due to utilization in widespread applications such as battery chargers, renewable energy applications [1], electric vehicles [2], motor drives [3], fuel cells [4], photovoltaic applications [5] and traction systems [6]. These efficient high power converters usually require continuous current mode (CCM) operation in grid-tied applications [7]. The high power density and efficiency requirement can be fulfilled by increased switching frequency [8, 9]. However, drawbacks associated with switching frequency including switching losses and electromagnetic interference (EMI) must be addressed. If these problems are not carefully resolved, the increased switching frequency is ineffective to reduce the weight and volume of a converter but in some cases, it may increase the volume of a converter [10]. To meet the increased switching frequency requirement, soft switching conditions must be provided [11, 12]. To achieve soft switching, special circuits know as snubber circuits [13, 14] are employed to decrease the switching losses and improve the converter efficiency. These snubber circuits may cause problems such as increased components count, complexity of power and control circuitry, and ringing issues, but at the same time, they provide zero voltage switching (ZVS) and zero current switching (ZCS) operations of the semiconductor switches at turn on and turn off instants [15]. In literature, many snubber circuits have been introduced for converters [16–21]. In [16], the snubber circuit provides soft switching but a voltage ringing is observed during the switch turn off resulting in semi-ZVS condition. In [17], employed snubber circuits increased not only the number of components but also the cost by utilizing two different cores for snubber inductors. Besides providing ZVS and ZCS conditions at turn on and turn off instants respectively, for flyback converter, circulation losses have been increased [18]. In [19], the proposed snubber circuit has increased conduction losses as well as size of the converter. In [20], the saturable inductor used as a snubber circuit has produced voltage ringing at turn off. The snubber circuit in [21] provides ZCS at turn on. However, it loses soft switching at turn off. Beside snubber circuits, other methods such as load resonant, resonant transition and resonant link are also recommended [22] to achieve soft switching. Among these methods, quasi-parallel resonant dc-link inverters (QRDCLI) have advantages of zero voltage switching of main switches, PWM capability due to flexible resonant link on/off instants, low number of auxiliary switches and minimum voltage stress of main switches [23–25]. However, converters using quasi-parallel resonant dc-link, such as presented in [25, 26] usually require complicated control systems and total cost is high. The latest research related to these converters is to reduce the number of auxiliary switches to simplify the control circuit and decreases the cost. The number of auxiliary switches is reduced at the expense of employing additional elements such as diodes, coupled inductors and capacitors [24]. Sometimes, control over the dc-link zero voltage is also lost, resulting in hard switching of switches [25]. In various

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soft switched topologies, the EMI reduction is not significant due to undesired resonances and parasitic components [27]. In addition to soft switching operation and efficiency improvement, EMI of the proposed converter scheme has also been reduced significantly due to low di/dt rate and low dv/dt rate of the semiconductor switches. However, its evaluation is not the scope of this paper.

Several three phase converter topologies have been proposed in the literature for high power applications. A comprehensive literature on converter topologies suitable in high power applications highlighting the pros and cons of techniques to achieve desirable characteristics has been presented in [7]. For example, the full-bridge six-switch rectifier topology discussed in [28] is a potential high power topology, however, it has high cost and low efficiency in comparison to similar topologies. Similarly, the high EMI caused by discontinuous operation is a challenge in [29]. Modular multilevel and interleaved converter topologies have remarkable achievements in high power applications [30–32]. However, requirement of complicated control system due to current sharing issues in these topologies is one of the major concerns [33]. The traditional power converters i.e. diode bridge or multi-pulse converters have been in use for decades due to high efficiency, reliability and availability of power electronic devices [34]. However, high input current harmonics, low power factor, heavy weight, large volume and high maintenance cost are the main factors that limit their use as front-end converters [35].

The active three level boost converter topologies are assumed a recent trend in high power applications because of the low device voltage rating benefit, which is specifically important for high voltage applications [36]. Among the three level boost topologies, vienna topology is considered a preferred choice for high power density requirements such as power supplies, motor drives and vehicular applications [37]. Moreover, it has potential characteristics such as reduced input filter size and conduction losses, high voltage conversion ratio and better efficiency. The fault tolerance ability of the vienna rectifier topology is comparably better than others [38]. The drive circuit of the semiconductor switches in the three level circuit structure is simple because of the connection of switches [39]. Apart from three level topologies, hybrid rectifier topologies [34] as front-end converters stage is a current research direction in high power applications due to the following advantages:

- Hybrid rectifiers incorporate the leading characteristics of passive rectifiers such as simplicity, reliability, robustness and low cost [40] and the excellent features of active rectifiers such as low THD_I and unity power factor [41, 42],
- Higher overall efficiency of the system because of integrating units of the hybrid system process portion of the active power in an optimized ratio [43];
- Greater flexibility in following the grid interconnection standards i.e. THD_I of desired rating can be achieved easily using the current control of the active unit [35],
- Cost effective compared to switched PFC pre-regulators [34, 40],
- Simplicity in control technique [44].

Owing to above characteristics and extensive literature survey, the high power converter topologies considered for comparative analysis with the proposed high power converter scheme are the three phase three level T-type vienna boost rectifier topology and three phase hybrid rectifier topologies. These converter systems are the mainstream PFC technologies for the next generation due to high performance in high power front-end converter applications. The circuit configurations of these high power rectifier topologies considered for comparative analysis with the proposed converter scheme are shown in Fig. 1. These converters operate with high power factor and less total harmonic distortion of the line current. Figure 1a shows an active three level vienna boost converter. The vienna rectifier system is considered as a promising candidate for high power applications due to its attractive inherent characteristics [45]. Figure 1b and Fig. 1c represent hybrid rectifier systems formed by parallel combination of a three phase diode bridge rectifier and DC/DC boost converter with a unidirectional three level T-type vienna and three phase full bridge (FB) boost converter, respectively. In hybrid rectifier system based on unidirectional T-type vienna rectifier [34, 40], the positive instantaneous input power maintains sinusoidal input currents. Furthermore, an optimal ratio of power distribution between constituent circuits of the hybrid system is set to obtain high power factor operation

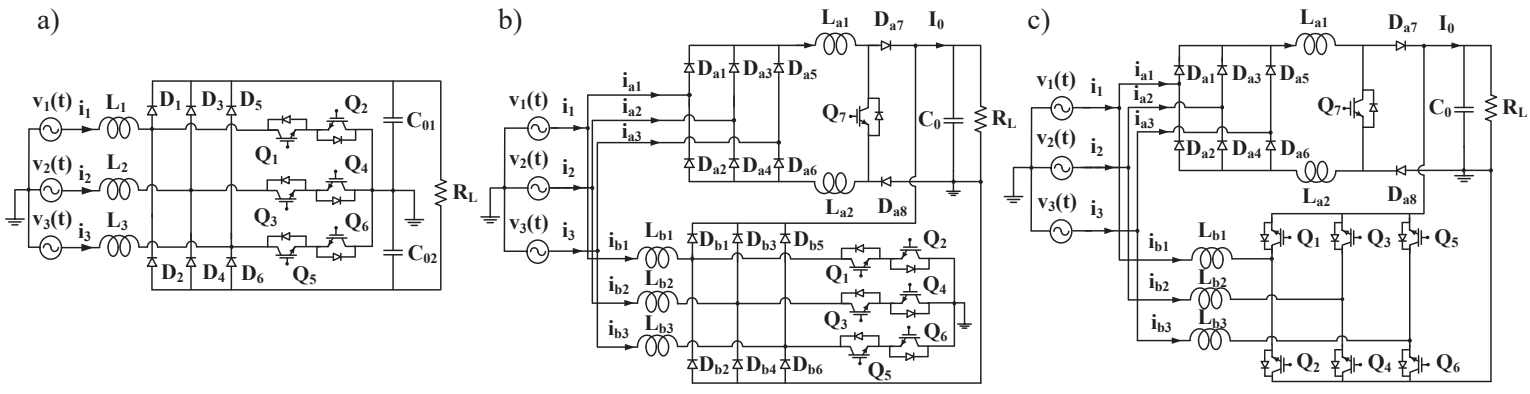

Fig. 1. Prior art high power rectifier topologies, (a) an active three level vienna boost converter system, (b) a hybrid system based on a single switch boost and vienna rectifier units, and (c) a hybrid rectifier system employing a single switch boost and FB boost converter units

limit. For hybrid rectifier system employing a FB boost converter [34], the high power factor operation can theoretically be achieved for any power sharing ratio between the integrating rectifier units [cf. Fig. 1c]. For instance, if the line-commutated rectifier part processes 100% of the load power, the FB boost converter will compensate only current harmonics resulting in an improved power factor operation. In this case, the FB boost converter unit works as a shunt active power filter.

In this paper, a soft switched PWM AC/DC converter topology employing a resonant switching network is investigated. The proposed converter circuit helps in carrying out soft commutation of both the semiconductor switches and the rectifier diodes. Theoretically, the arrangement of semiconductor switches in the proposed converter inherently favors high current high power applications. The circuit description, principle of operation and design considerations of the proposed converter are covered in the following sections. The proposed soft switched converter is implemented in practice to verify its soft switching operation and performance evaluation. Besides investigation and implementation, a comparative study of the proposed soft switched converter topology has been carried out with some prior art high power AC/DC converters [cf. Fig. 1]. For calculation of switching losses and hence, efficiency determination, a MATLAB/Simulink measuring subsystem developed in [46] is utilized to estimate switching power losses of semiconductor devices of the hard switched prior art high power converter topologies. The performance assessment of these converters is carried out by considering their important characteristics such as switch stresses, THDs, power factors, component counts and efficiencies.

The paper is further organized into the following sections. The circuit description, steady state analysis and resonant circuit design of the proposed converter are carried out in Section 2. Section 3 briefly describes control strategy of the proposed soft switched AC/DC converter. The simulation results illustrating soft switching behavior and dynamic response of the proposed scheme are shown in Section 4. Section 5 shows important simulated results of the candidate prior art high power converter circuits [cf. Fig. 1]. These high power rectifier topologies are compared with the proposed soft switched PWM AC/DC converter scheme to determine its significance in the high power industrial applications. A MATLAB/Simulink measuring subsystem is used to calculate switching losses of semiconductor devices in these hard switched prior art high power topologies. The comparison of important characteristics of the proposed converter with the prior art high power rectifier topologies is carried out in Section 6. The experimental results of the proposed converter are illustrated in Section 7. Section 8 concludes the paper.

2. Proposed soft switched PWM AC/DC converter

2.1. Circuit description and principle of operation. The proposed soft switched PWM AC/DC converter consists of three uniform single phase converter stages as illustrated in Fig. 2a. Each single phase converter stage has a line inductor, a pair of

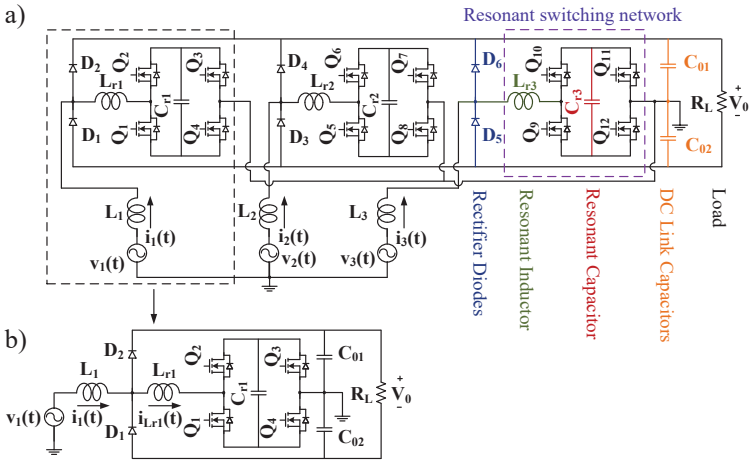

Fig. 2. (a) Proposed soft switched PWM AC/DC converter, (b) Decoupled single phase configuration of the proposed soft switched PWM AC/DC converter

rectifier diodes and a resonant switching network. Each resonant switching network consists of a resonant inductor, a resonant capacitor and a semiconductor bridge. The midpoint of one arm of each semiconductor bridge configuration is connected to the center point of output DC link capacitors C_{01}, C_{02}. The output DC link capacitors center point is connected to the neutral point of input voltage source. The output DC link capacitance values are normally chosen higher than the calculated values, taking the equivalent series resistance and ripple requirements into account. Considering the fact that the DC link capacitors are sufficiently large, the proposed three phase circuit can be decoupled into three isolated single phase circuits, as shown in Fig. 2b. The resonant inductor helps to mitigate the reverse recovery loss of rectifier diodes by presenting a low impedance path and controlling switch turn on current transients. The resonant capacitor, which is parallel to semiconductor bridge minimizes the problem due to dv/dt rates. Due to resonant inductor, resonant capacitor and semiconductor bridge arrangement, the semiconductor devices and the rectifier diodes operate under soft switching conditions, leading to appreciably reduced switching losses and hence, higher efficiency.

During turn on transition, the resonant inductor current flows in the diagonal semiconductor switches while discharging the resonant capacitor and returns to the input voltage source through midpoint of output DC link capacitors. When the resonant capacitor is almost completely discharged, the current divides between the switch and other switch diode in the same arm of semiconductor bridge, which ultimately, leads to decreased average current switch stress. During turn off transition, the resonant inductor current flows only through the diagonal diodes of switches of semiconductor bridge while gradually charging resonant capacitor (hence, leading to switch turn off at ZVS) and back to the input voltage source through midpoint of output DC link capacitors. When the switching network is inactive, energy from the source is transferred to the load via rectifier diode. The key theoretical waveforms describing operation of the single phase configuration [cf. Fig. 2b]

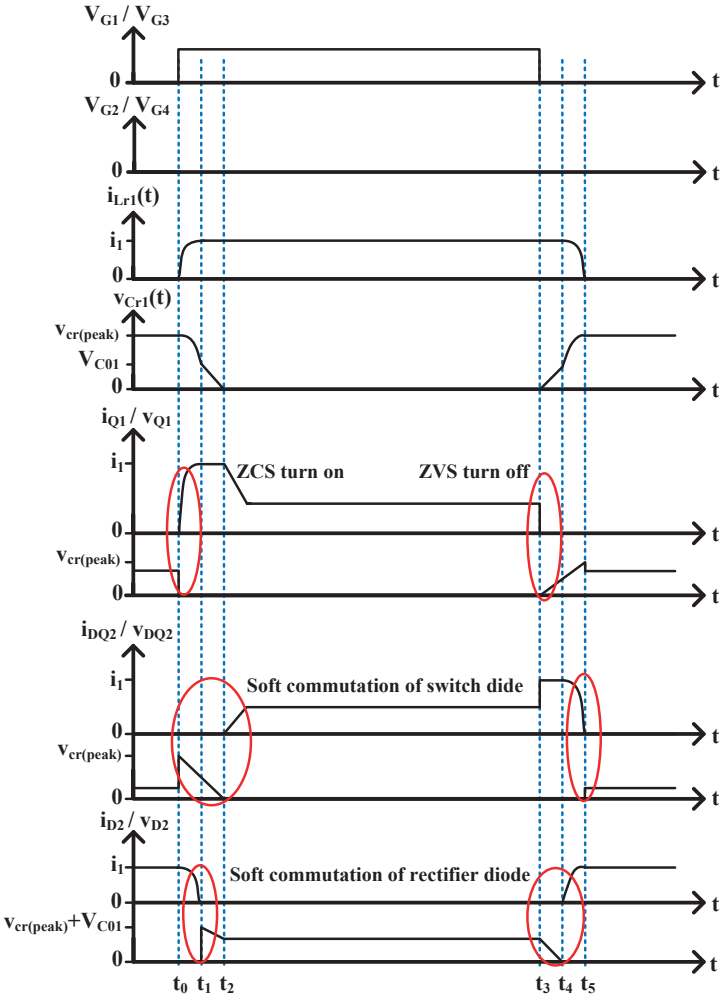

Fig. 3. Key theoretical waveforms of the proposed soft switched PWM AC/DC converter during positive half cycle of input voltage $v_1(t)$, V_{G1}, V_{G2}, V_{G3}, V_{G4}: gate signals of switches Q_1, Q_2, Q_3, Q_4 respectively; i_{Lr1}: resonant inductor current; v_{Cr1}: resonant capacitor voltage; i_{Q1} and v_{Q1}: semiconductor switch current and voltage; i_{DQ2} and v_{DQ2}: semiconductor switch diode current and voltage; i_{D2} and v_{D2}: rectifier diode current and voltage; $v_{cr(peak)}$: resonant capacitor peak voltage; i_1: line inductor current; and V_{C01}: DC link capacitor voltage

of the proposed soft switched AC/DC converter are shown in Fig. 3. Due to symmetry, these waveforms describe the operation of the proposed circuit only in the positive half line cycle. The equivalent circuits corresponding to various intervals, as shown in Fig. 3 are illustrated in Fig. 4. The input voltage $v_1(t)$ and input inductor L_1 can be approximated by a steady source current I_s, since the commutation interval is smaller than the switching frequency of the converter.

In the resonant switching circuit, energy stored in the resonant capacitor is released by resonant inductor through semiconductor switches resulting in ZCS turn on of the semiconductor switches and delivered to the input voltage source and later on, transfered to the output through rectifier diodes. In some cases, for instance, in [18], the resonant capacitor energy is transferred to input source voltage, which results in increasing the circulation losses. The resonant inductance

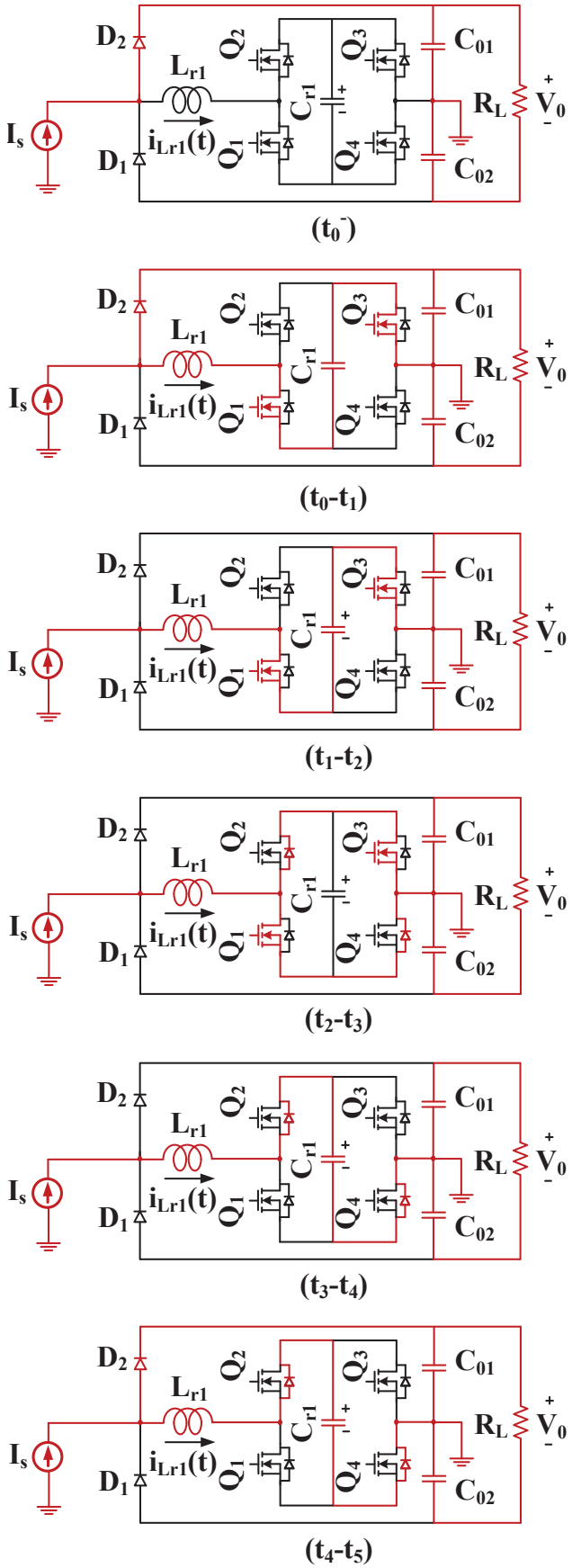

Fig. 4. Equivalent circuits corresponding to various stages of the proposed converter scheme during positive half cycle of the input voltage

value is smaller in magnitude and, hence, its voltage is low and considered constant. The current flowing in resonant inductor cannot surpass the source current value. This limited current value results in decreased average power loss. Moreover, the gradual increase/decrease of current in the resonant inductor is similar to the gradual decrease/increase in the rectifier diode current, leading to its soft commutation. Natural compatibility with the high current high power applications is the distinguishing feature of the proposed soft switched rectifier topology. The proposed converter [cf. Fig. 2b], proportional to two parallel arms, each with a pair of semiconductor devices, carrying out ZVS/ZCS and switching operation phenomena at the same switch count, results in low cost.

2.2. Mathematical analysis. The steady state analysis of the proposed ZVS/ZCS PWM AC/DC converter for positive half cycle of the grid voltage is given by the following equation:

$$v_1(t) = L_1 \frac{di_1}{dt} + M\left[V_{Q(1,3)} + V_{Q(D2,D4)}\right] + \\ + (1-M)V_0 + V_N, \tag{1}$$

where v_1 is input phase voltage, i_1 represents phase current, L_1 is line inductance, $V_{Q(1,3)}$ represents voltage across switch Q_1 and switch Q_3, $V_{Q(D2,D4)}$ represents diode voltage of Q_2 and Q_4, and V_N is the DC link capacitor midpoint voltage with respect to the mains neutral. L_{r1} value is very small and hence can be ignored in (1).

$$M = \begin{cases} 0 & \text{if switching network is inactive} \\ 1 & \text{if switching network is active} \end{cases} \tag{2}$$

$$V_{Q(1,3)} = \begin{cases} v_{Cr1} & \text{if switch is turned off} \\ 0 & \text{if switch is turned on} \end{cases} \tag{3}$$

$$V_{Q(1,3)} = (1-s)v_{Cr1} \tag{4}$$

s represents switching function defined as

$$s = \begin{cases} 0 & \text{if switch is turned off} \\ 1 & \text{if switch is turned on} \end{cases} \tag{5}$$

$$V_{Q(D2,D4)} = \begin{cases} v_{Cr1} & \text{unless resonant capacitor} \\ & \text{is fully discharged} \\ 0 & \text{otherwise} \end{cases} \tag{6}$$

v_{Cr1} is the voltage of resonant capacitor.

The output dc link capacitors are defined by (7) and (8) as follows:

$$C_{01}\frac{dv_{C_{01}}}{dt} = (1-s).i_1 - \frac{V_0}{R_L} \tag{7}$$

$$C_{02}\frac{dv_{C_{01}}}{dt} = -(1-s).i_1 - \frac{V_0}{R_L}. \tag{8}$$

The elements of resonant circuit L_{r1} and C_{r1} are selected so as to ensure the following requirements.

- The semiconductor device and rectifier diode stresses are kept under allowable limits.
- Soft switching of the semiconductor devices and rectifier diodes can be achieved.
- The resonant inductance value is such that it ensures resonant capacitor to charge and discharge to its peak voltage and null voltage, respectively.
- The selected resonant inductance value meets the loss requirement of rectifier diode.

$$L_{r1} = \left[\frac{V_0}{2} + v_{C_{r1}}(t)\right]\left(\frac{di_D}{dt}\right)^{-1}, \tag{9}$$

where $\mathrm{d}i_D/\mathrm{d}t$ is the rate of change of current in rectifier diode during turn off and L_{r1} value is approximated for smaller value than the $(\mathrm{d}i_D/\mathrm{d}t)_{max}$, mentioned in the data sheet. The minimum resonant inductance L_{r1} value is selected through simulation and experimentation such that it produces minimum power loss in rectifier diode, while considering the maximum value of current. The C_{r1} value is calculated for the selected L_{r1} value.

The inequality fulfilled is as follows:

$$L_{r1} \le \frac{t \times V_0}{I_s} \tag{10}$$

$$C_{r1} = \frac{4t^2}{\pi^2 L_{r1}} \tag{11}$$

t represents the time interval $(\mathrm{t}_0 - \mathrm{t}_1)$, in which the current in the rectifier diode has decreased to zero and the resonant inductor current has reached a steady state source current value I_s.

The peak current through resonant inductor L_{r1} and peak voltage across resonant capacitor C_{r1} are as follows:

$$i_{Lr1}(peak) = I_s \tag{12}$$

$$v_{Cr1} = V_{C01} + z_0 I_s \tag{13}$$

V_{C01} is the voltage of output dc link capacitor C_{01} and

$$z_0 = \frac{1}{\omega_0 C_{r1}} \tag{14}$$

At light load/around zero crossing of phase current, the resonant current value is not high enough to charge and discharge the resonant capacitor properly. During turn off period t, the resonant capacitor C_r starts charging and its voltage increases, as follows:

$$v_{cr} = \frac{i_{Lr} \times t}{C_r} \tag{15}$$

The instantaneous value of resonant current i_{Lr} can be calculated as follows:

$$i_{Lr} = I_m \sin\theta_r \tag{16}$$

I_m represents peak value of resonant inductor current.

At boundary condition, in $(1 - d)T_s$ interval, the resonant current is only sufficient to charge resonant capacitor C_r to its peak value $v_{cr(peak)}$, which is expressed as follows:

$$\theta_r = \arcsin\sqrt{\frac{v_{cr(peak)} \times C_r \times V_0 \times f_s}{I_m \times V_1}}\,. \tag{17}$$

This expression shows the boundary of effectiveness of switching conditions in the proposed converter. Beyond this condition, the converter operates either in continuous conduction mode (CCM) or in discontinuous conduction mode (DCM). In DCM, the resonant current is not high enough to fully discharge the resonant capacitor, which produces hard switching at turn off. However, losses associated with this hard switching are lower due to low switch current. Also, the resonant capacitor has less voltage due to discharge, which further reduces the losses. Similarly, the resonant current is not enough to charge the resonant capacitor to its peak value, however, it has no effect on the zero current switching at turn on.

The curves shown in Fig. 5 represent various values of maximum resonant inductor current versus instantaneous resonant current and angles around the zero crossing of the line current. These curves illustrate that in the vicinity of zero crossing of line current, the chances of effectiveness of switching conditions are low.

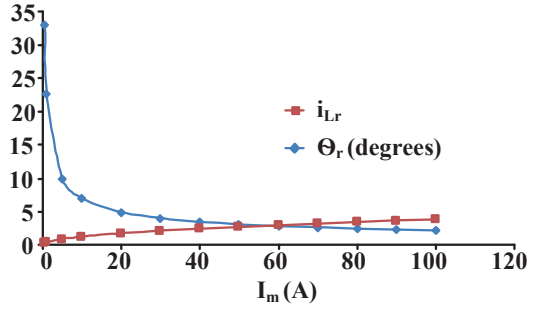

Fig. 5. Curve representing effectiveness of resonant inductor current near zero crossing

3. Control strategies of candidate high power topologies

The control system of the proposed soft switched PWM AC/DC converter is depicted in Fig. 6. This scheme aims to achieve regulated output voltage, sinusoidal input current and soft switching operation of the proposed converter. The control scheme of the proposed circuit is simple which consists of an outer voltage control loop and an inner current control loop [37, 47]. The actual output voltage $V_0 = V_{01} + V_{02}$ is compared with the reference voltage V_0^*, where V_{01} and V_{02} are voltages across output DC link capacitors, C_{01} and C_{02}, respectively. The

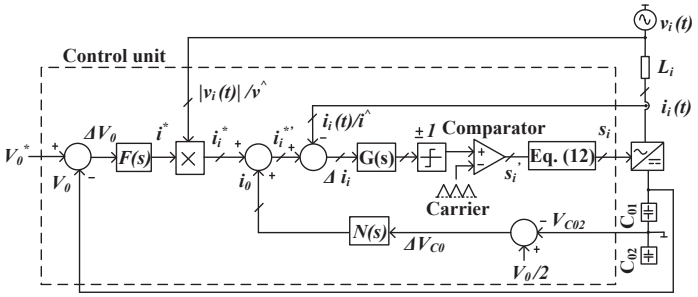

Fig. 6. Control scheme of the proposed soft switched PWM AC/DC converter, F(s): controller of output voltage V_0; N(s): balancing controller of output DC link capacitor voltages V_{C01}, V_{C02}; G(s): current controller of the phase currents $i_i(t)$, i = 1, 2, 3; s_i: switching signals generated according to (12) and (13); the three phase signals are shown by cross lines, for the sake of clarity

signal $\triangle V_0$ thus produced is compensated by voltage controller $F(s)$. Detailed explanation of the output voltage controller is omitted here for the sake of brevity. The phase current reference magnitude $i_i^{*\prime}$ (derived from phase voltage for resistive mains behavior) given by output voltage controller $F(s)$ is superimposed on the inner control loop. The current controller $G(s)$ generates a modulating signal which is compared with a triangular carrier signal of converter switching frequency. The control signals s_i are thus produced for the semiconductor switches taking the influence of the sign of input phase voltage v_i on that of the associated phase current i_i. Any change in the measured quantities changes the duty ratios, and therefore, helps to keep the input current shapes sinusoidal for all possible switching states.

$$s_i = \begin{cases} s_i' & \text{if } i_i^* \geq 0 \\ NOT\, s_i' & \text{if } i_i^* < 0 \end{cases} \tag{18}$$

$$s_i' = \begin{cases} 0 & \text{if } i_i(t) > i_i^* + 1 \\ 1 & \text{if } i_i(t) < i_i^* - 1 \end{cases} \tag{19}$$

Besides output voltage regulation and mains current control, an equal distribution of output voltage on DC link capacitors is guaranteed by control system $N(s)$ of the converter. Control schemes of the prior art high power rectifier systems [cf. Fig. 1] are designed to ensure regulation of output DC voltage, distribution of an optimal load power ratio between compounding units of the hybrid rectifier systems, mitigation of input current harmonics and correction of power factor. Details of the control schemes adopted for these systems may be found in [34, 37, 40, 48].

4. Simulation results of the proposed scheme

A model of the proposed ZVS/ZCS PWM AC/DC converter circuit has been developed in MATLAB/Simulink using design specifications enlisted in Table 1. Equations (10) and (11) are

Table 1
Specifications used in simulation and experimental validation

Parameters	Description	Values
V_i	Input voltage (RMS value)	220 V
V_0	Output voltage	800 V
P_0	Output power	10 kW
f_s	Switching frequency	40 kHz
L_i	Line inductance	1 mH
C_{01}, C_{02}	DC link capacitances	10 mF
L_r	Resonant inductance	1:323 µH
C_r	Snubber capacitance	0.0020426 μF
Q_1, Q_2, Q_3, Q_4	Semiconductor devices	STY139N65M5
D_1, D_2	Rectifier diodes	DSEI2×101 – 12A

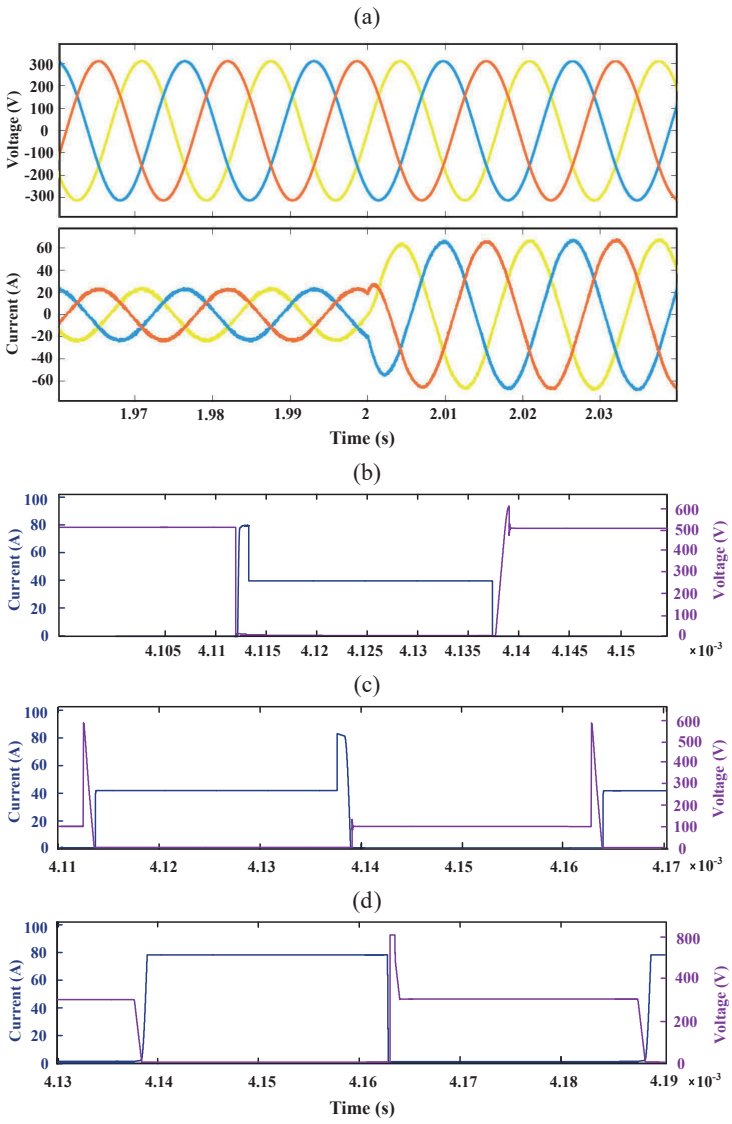

Fig. 7. Simulated results, (a) input voltage and current, (b) switch current and voltage waveforms, (c) switch diode current and voltage, and (d) rectifier diode current and voltage waveforms

used to select resonant circuit elements L_r and C_r. Figure 7 shows the input voltage and current, switch current and voltage, switch diode current and voltage, and rectifier diode current and voltage waveforms of the proposed converter. Figure 7a justifies the PFC operation and dynamic performance of the proposed circuit. At time t = 2*s*, the increase in load has produced a proportional increase in the input current without deviation from sinusoidal waveform. The switch current and voltage waveforms in Fig. 7b reveal that it turns-on and -off with ZCS and ZVS, respectively. The soft commutation of the switch diode is shown in Fig. 7c. Figure 7d verifies the soft commutation of the rectifier diode.

5. Simulation results and comparative analysis of the high power topologies

The purpose of this Section is to determine standing of the proposed soft switched AC/DC converter topology among the candidate prior art high power rectifier topologies through simulation verification of their important characteristics such as phase current and voltage waveforms, and input current THDs. The three phase models of the active three level vienna boost converter [cf. Fig. 1a], and hybrid rectifier systems based on three level unidirectional vienna converter [cf. Fig. 1b] and FB boost converter [cf. Fig. 1c] are built in MATLAB/Simulink environment. The steady state simulations of these high power converter systems and the proposed converter are computed for 20 kW load and 10 kHz switching frequency. The reduced switching frequency for these three phase high power systems have been considered because of the hard switching losses of the candidate high power topologies. The IGBT used is power module *SK*60*GAR*123 from Semikron company. Figure 8a illustrates the three phase grid injected current and voltage waveforms of the three level vienna boost rectifier. The grid injected current is in phase with the grid voltage ensuring the unity power factor phenomenon. Figure 10a shows the harmonic spectrum of its input current with $THD_I = 1.71\%$. The proposed soft switched PWM scheme gives displacement power factor 0.9998 and $THD_I = 2.45\%$. Figure 8b and Fig. 10b illustrate the grid injected current and voltage waveforms, and harmonic spectrum of the input current, respectively, of the proposed soft switched PWM converter. The harmonic spectrum of the proposed converter exhibits relatively higher contribution of 3rd, 5th and 7th order harmonics, however overall total harmonics distortion (THD) is less than 5% according to grid interconnection standards. Currents of constituent converters of the vienna based hybrid rectifier system are integrated to construct a low harmonic nearly sinusoidal input current waveform shown in Fig. 9b. Figure 8c presents its three phase voltage and current waveforms confirming PFC operation. The currents are nearly sinusoidal with $THD_I = 15.06\%$, as verified in Fig. 10c. A sinusoidal harmonic-free current waveform can be achieved from non-sinusoidal current waveforms of constituent rectifiers of the hybrid rectifier system employing a FB boost converter, as demonstrated in Fig. 9a. The voltage and current waveforms of each phase are indicated in Fig. 8d verifying power factor

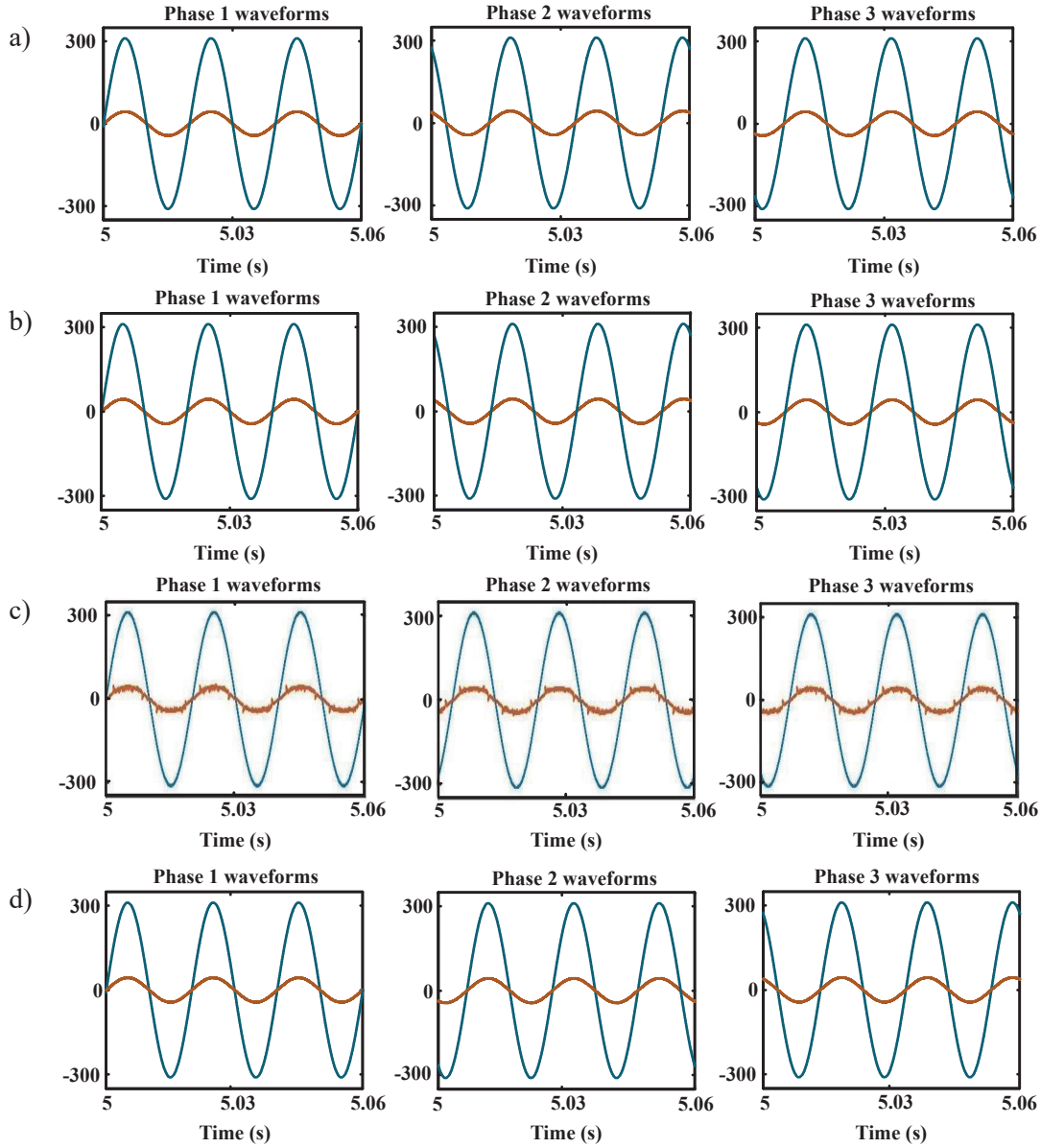

Fig. 8. Grid injected current and voltage waveforms, (a) three level vienna boost rectifier, (b) proposed soft switched PWM AC/DC converter, (c) hybrid rectifier system based on three level vienna rectifier, and (d) hybrid rectifier system based on FB boost converter

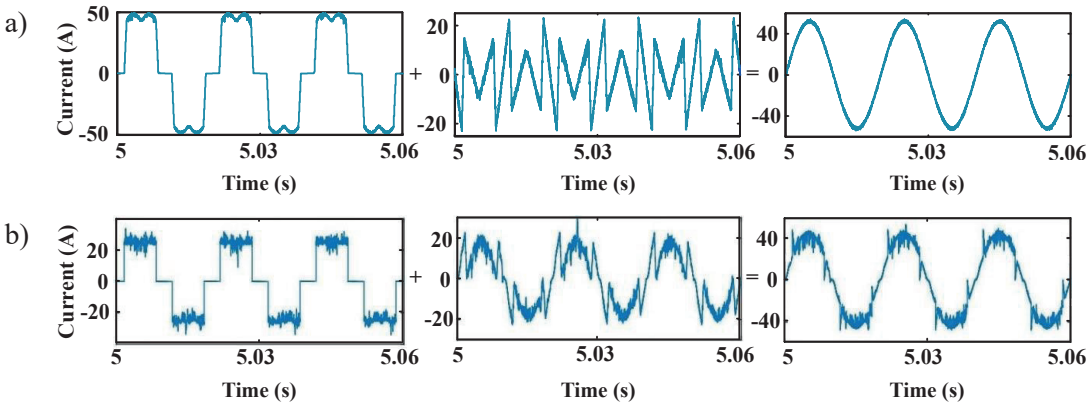

Fig. 9. Composition of the desired sinusoidal waveform from input current waveforms of compounding units, (a) hybrid rectifier system based on FB boost converter, and (b) hybrid vienna based rectifier system

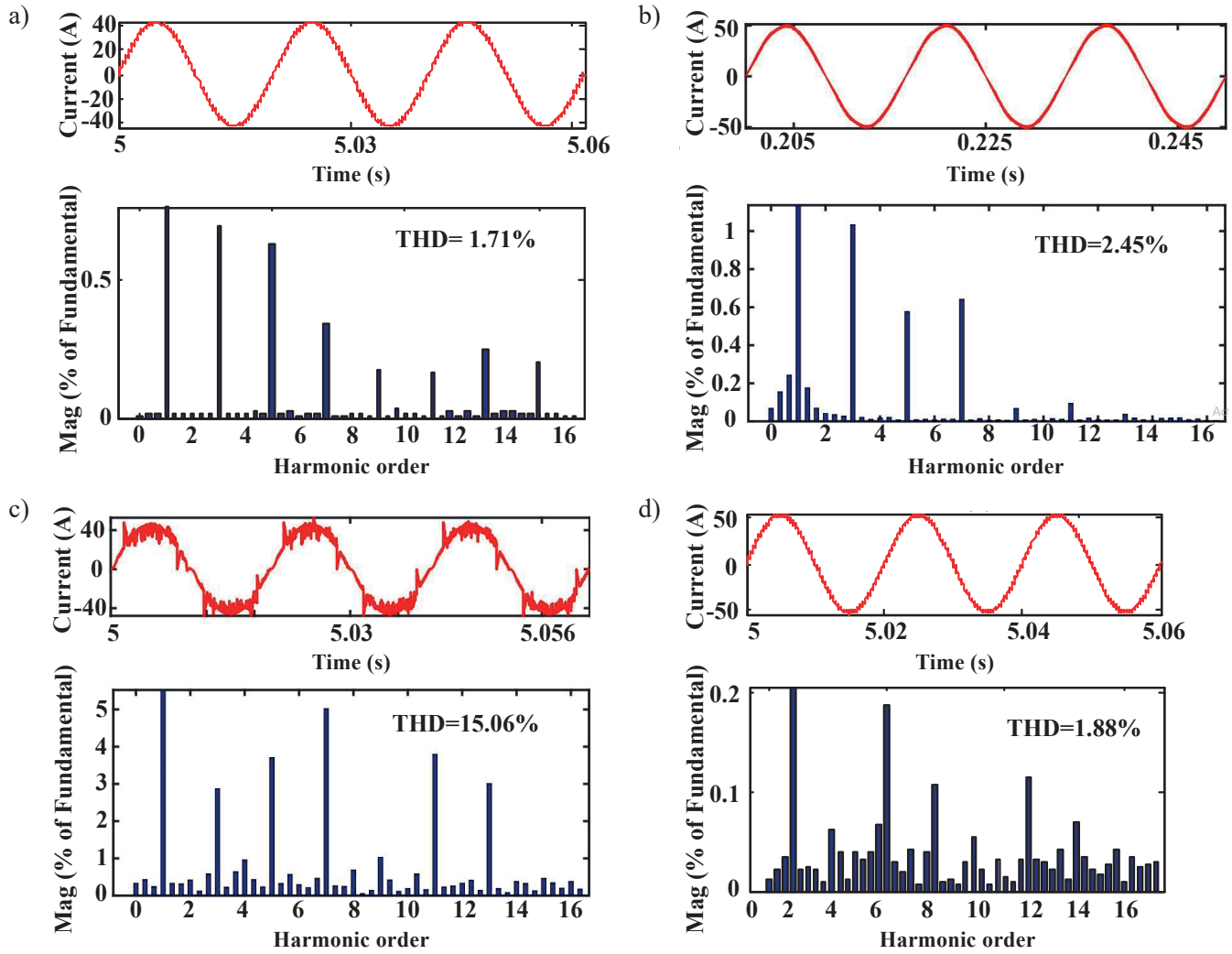

Fig. 10. Input current harmonic analysis, (a) three level vienna boost rectifier, (b) proposed soft switched PWM AC/DC converter; (c) hybrid vienna based rectifier system, and (d) hybrid rectifier system based on FB boost converter

correction operation with low harmonic current content i.e. $\mathrm{THD}_I = 1.88\%$, depicted in Fig. 10d.

5.1. Determination of switch power losses. The semiconductor switch power losses are predominantly influenced by conduction and switching losses. The conduction losses can be calculated by linearly approximating volt-ampere characteristics of the power switch, that correspond to an equivalent circuit, which consists of a voltage source with a known value of threshold value V_T and a series on-state resistance R_{on}. The average power conduction loss is as follows:

$$P_{conduction} = I_{av} V_T + I_{rms}^2 R_{on} \tag{20}$$

I_{av} and I_{rms} are average and effective currents of power switch, respectively.

The switching losses are calculated based on energy dissipations at turn on and turn off instants. The average switching power loss of a semiconductor device switching at frequency f_s can be determined from the following equation:

$$P_{switching} = (E_{on} + E_{off}).f_s \tag{21}$$

$$\begin{aligned} E_{on}(actual) &= E_{on}(ref).\frac{I_c(actual)}{I_c(ref)}.\left(\frac{V_{cc}(actual)}{V_{cc}(ref)}\right)^{k_v} \\ E_{off}(actual) &= E_{off}(ref).\frac{I_c(actual)}{I_c(ref)}.\left(\frac{V_{cc}(actual)}{V_{cc}(ref)}\right)^{k_v} \end{aligned} \tag{22}$$

$\mathrm{I}_c(actual)$, $\mathrm{V}_{cc}(actual)$ are actual values of semiconductor switch current and voltage, $\mathrm{I}_c(ref)$, $\mathrm{V}_{cc}(ref)$ denote reference values, specified in the datasheet and the value of exponent k_v ranges from 1.20 to 1.40.

The total average power loss of the semiconductor switch can be obtained as follows:

$$P_{total} = P_{conduction} + P_{switching}. \tag{23}$$

The semiconductor devices and rectifier diodes of the proposed converter operate softly, hence, the switching power losses are

appreciably small and can be ignored. However, the conduction power losses of the proposed converter are considered, whose values are reasonably low. To estimate switching power losses of the prior art hard switched high power topologies discussed above, a MATLAB/Simulink block to calculate switching energy dissipations E_{on}/E_{off} and average power losses P_{on}/P_{off}, is developed shown in Fig. 11 and its detail is given in [46]. In this design, the value of L_{r1} is not required to be very large, hence its rate of change is large and fast. During the switching transient, its value cannot exceed the source current value. This limited resonant current leads to reduced conduction losses. The designed value of resonant inductance has been realized in the experimental setup by manually winding the ferrite core with few turns of Litz wire and its inductance value is confirmed by LCR meter. The winding resistance of the resonant inductor is 1.67 mΩ, which produces negligible conduction loss.

6. Performance analysis of the candidate high power converters

To evaluate the performance, a comparative analysis of the proposed ZVS/ZCS PWM AC/DC converter with existing high power converter topologies mentioned above is carried out. The important characteristics considered for the candidate converters include number of components (complexity), components utilization, components voltage and current stresses, switching aspect and rated efficiency.

To determine the required characteristic quantities, digital simulations are based on the following assumptions:

- Sinusoidal symmetrical mains voltage,
- Internal mains impedance is neglected,
- Ideal passive components (no eddy and hysteresis loss of inductors and no ESR of capacitors),
- Unidirectional power flow.

Results of simulations are compiled in Table 2. This Table shows that the active three level vienna boost rectifier has a low blocking voltage stress on the semiconductor devices, which is equal to half the output voltage as compared to the proposed soft switched AC/DC converter and hybrid rectifier systems. The proposed rectifier scheme achieves a switch voltage stress equal to half the output voltage plus $i_{i=1,2,3} \times z_0$, while the hybrid rectifier systems show as much voltage across semiconductor switches as the output voltage. The peak current stress of the semiconductor devices in the proposed and other high power converters is similar. The peak current switch stress is equivalent to the source current. The switch stress aspect of a converter is important to determine because the cost (total silicon area required to realize the semiconductor devices of the converter) and utility of the converter are mainly dependent upon this parameter. The number of semiconductors plays a vital role to determine the complexity of a circuit. The proposed soft switched scheme includes higher number of semiconductor switches, which is almost double those of the three level vienna boost and hybrid rectifier circuits. However, the active semiconductor switches of the proposed circuit are half of the total switch count during positive and negative half cycles of the main period. The vienna based hybrid rectifier system is at the top in course of diode count. The size of energy storage elements must also be considered in the comparative evaluation of converters. Because of the three level characteristic of bridge legs of three level vienna boost rectifier and proposed converter circuits, a significant reduction of the mains side inductances for a given input current ripple amplitude is observed com-

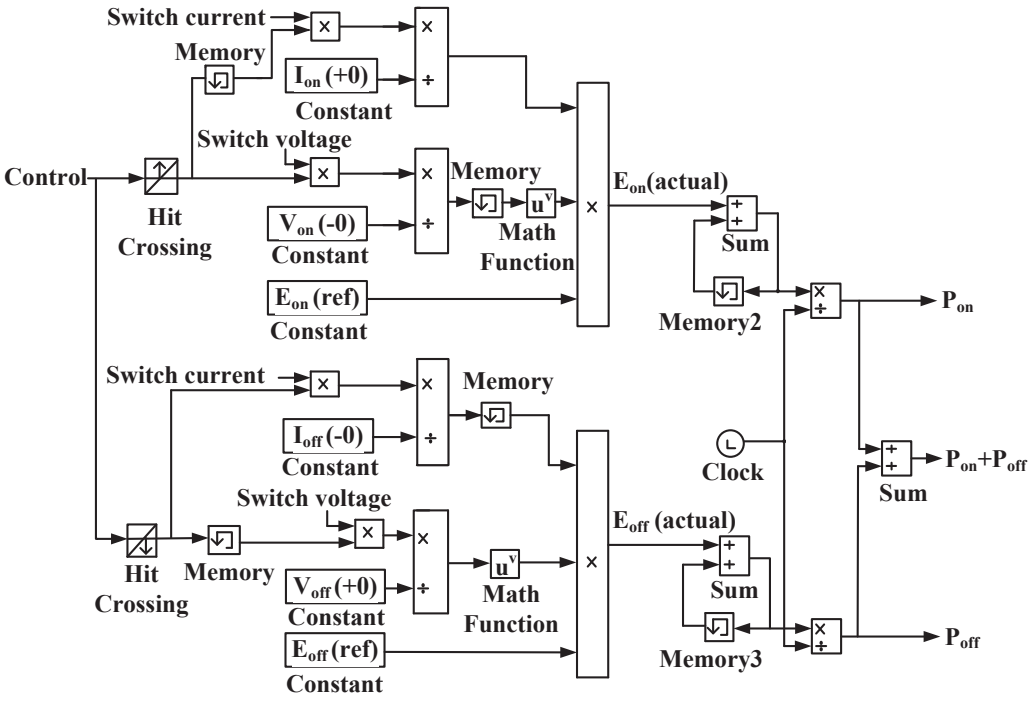

Fig. 11. Simulink system block for E_{on}, E_{off} and average power loss calculation

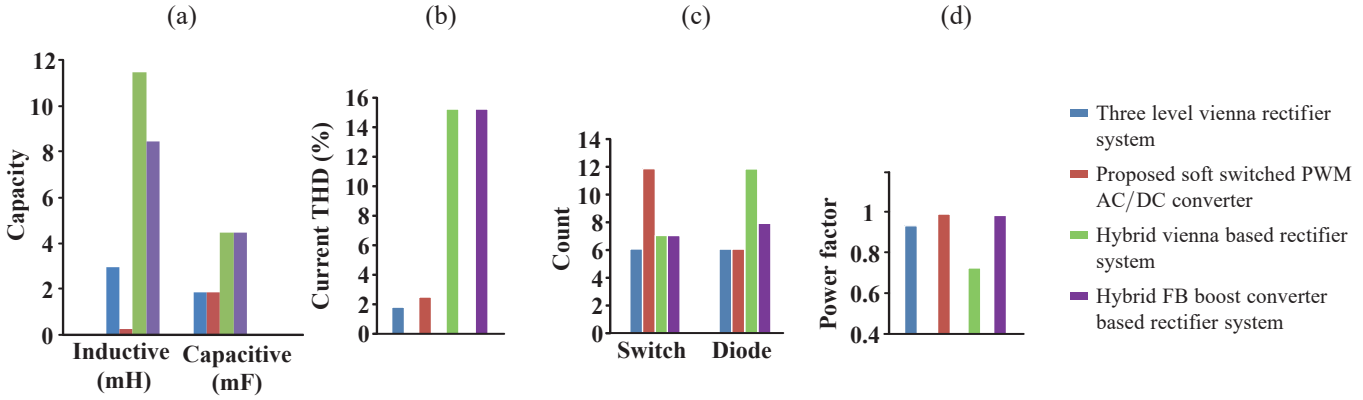

Fig. 12. Graphical illustrations, (a) energy storage passive components capacities, (b) input current THDs, (c) semiconductor device and rectifier counts; and (d) power factor corrections of the high power converter topologies

pared to hybrid rectifier systems. The hybrid rectifier systems require inductive capacity almost three times more than that of vienna and proposed converter circuits. The rated capacity of capacitive components of the hybrid rectifier systems is also higher, almost two to three times of the vienna and proposed converter schemes. The proposed converter is operating softy while the vienna and hybrid rectifiers are showing hard switching operations. The soft switching operation of the proposed converter is attained by inclusion of a series resonant inductor and a parallel resonant capacitor of fractional sizes in the proposed scheme. More importantly, the proposed converter together with three level vienna boost converter and hybrid rectifier system based on FB boost converter show a high mains current quality, representing an ideal solution for realizing unidirectional rectifier systems. Moreover, the proposed scheme achieves the highest power factor (99%), obviously showing its increased efficiency. The important characteristics of the above mentioned candidate high power rectifier topologies are graphically illustrated in Fig. 12a–12d. Total losses are calculated on the basis of simulation analysis for the proposed and prior-art high power converter schemes at a 20 kW rated power. As evident from Table 2, the total power loss calculated for the proposed converter scheme is less than that calculated for other candidate schemes. The reason is that the semiconductor switches and rectifier diodes of the proposed converter turn on and off softly, hence, switching losses are significantly smaller and may be ignored. However, the switch and diode conduction losses considered are reasonably low. The switching losses of the prior-art high power converters have been calculated by using the Simulink block developed in [46], shown in Fig. 11. The Simulink block developed calculates the switching loss without taking the tail current of IGBT into account. This will further increase the total power loss of the prior art high power converters.

Table 2
Characteristics of the proposed ZVS/ZCS AC/DC converter and prior art high power topologies

Parameters	Three level vienna boost rectifier	Proposed ZVS/ZCS PWM AC/DC converter	Hybrid vienna based rectifier system	Hybrid rectifier system based on FB boost converter
Voltage stress	$V_0/2$	$V_{cr(peak)} = V_0/2 + i_{i=1,2,3}z_0$	V_0	V_0
Current stress	$i_{i(peak)}$	$i_{i(peak)}$	$i_{i(peak)}$	$i_{i(peak)}$
Switch count	06	12	07	07
Diodes count	06	06	12	08
Inductors count	03	06	03	03
Inductors by size	3 mH	0:30066 mH	11:5 mH	8:5 mH
Capacitors count	02	05	01	01
Capacitors by size	1880 µF	1880:0765 µF	4500 µF	4500 µF
Switching aspect	Hard	Soft	Hard	Hard
Current THD (%)	1.71	2.45	15.06	1.88
Power factor	0.89	0.99	0.55	0.98
Total losses	910:216 W	247:32 W	683:456 W	724:92 W

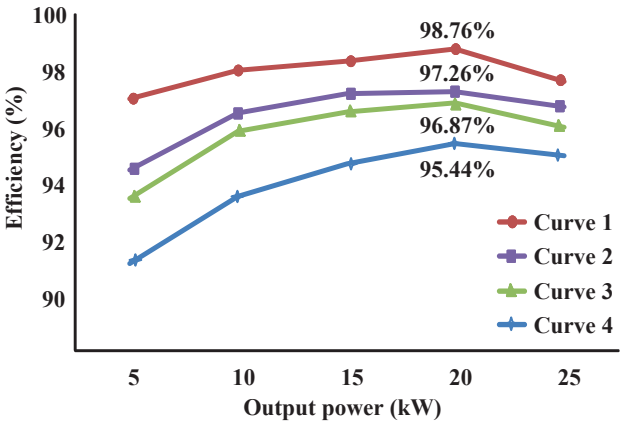

Fig. 13. Efficiency curves of high power converters, Curve 1: Proposed soft switched PWM AC/DC converter, Curve 2: Hybrid system based on FB boost converter, Curve 3: Hybrid vienna based rectifier system, Curve 4: Three level vienna rectifier system

The efficiency curves obtained from simulation examination for the proposed soft switched and other prior-art high power AC/DC converter schemes are illustrated in Fig. 13. It can be noticed that the efficiency of the proposed converter scheme is better than the other converter schemes and improves with increase in the output power. Thanks to the proposed topology performing soft switching operation, the total efficiency at the rated power reaches 98.76%.

7. Experimental validation of proposed scheme

To validate the theoretical and simulation analysis, an experimental arrangement of the proposed soft switched PWM AC/DC converter system is constructed in the laboratory, depicted in Fig. 14 as per specifications, listed in Table 1. To practically implement the control algorithm, a customized control board TMS320C28346^{TM} 32-bit microcontroller unit is utilized. The gate signals are provided to the semiconductor switches through gate driver cards. Figure 15a shows the dynamic response of grid injected current, when load is increased. The ZCS turn on and ZVS turn off of the semiconductor switch can

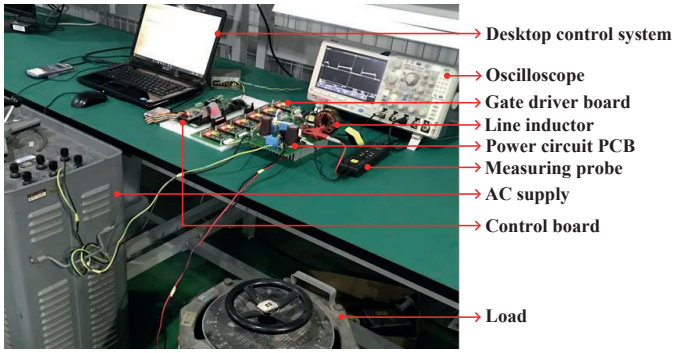

Fig. 14. Experimental setup diagram of the proposed soft switched PWM AC/DC converter

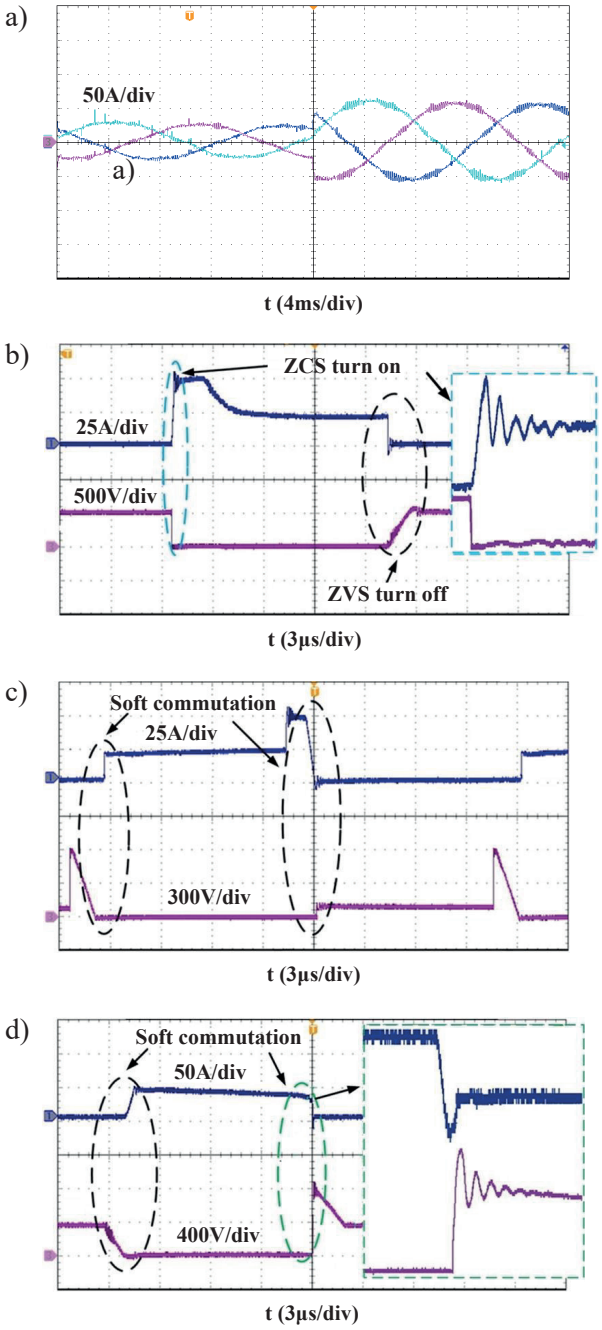

Fig. 15. Experimental results, (a) grid injected current dynamic response, (b) semiconductor switch current and voltage, (c) semiconductor switch diode current and voltage, and (d) rectifier diode current and voltage waveforms

be experimentally verified by Fig. 15b with enlarged portion of the switching instant during turn on, showing zero current switching with more clarity. The soft switching operations of the switch diode and rectifier diode are illustrated in Figs. 15c and 15d, respectively. Figure 15d is showing reverse recovery current in the rectifier diode of proposed converter, which produces reverse recovery loss of negligible value and hence, has negligible effect on the efficiency of the converter. The minimum diode power loss is estimated from non-linear sim-

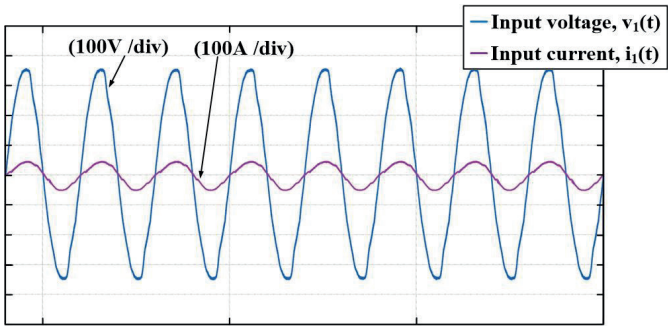

Fig. 16. Grid voltage and current waveforms of the proposed soft switched PWM AC/DC converter showing PFC operation

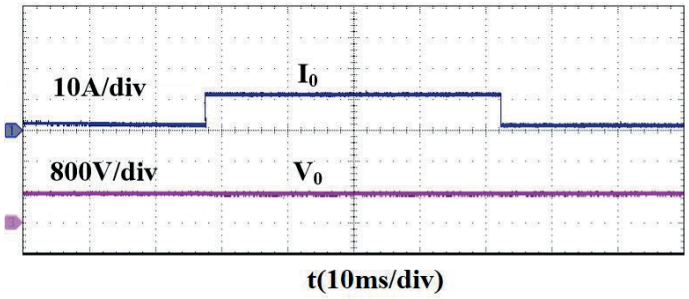

Fig. 17. Output characteristic of the proposed soft switched PWM AC/DC converter

ulations and through experimentation using different values of resonant inductor L_r values. Figure 16 shows that the grid injected current and voltage are in phase, confirming unity power factor operation. In order to examine the robust performance of the proposed converter, the experimental results illustrating the converter output voltage (V_0) and output current (I_0) under the step variation between no-load and full load is shown in Fig. 17. The converter output voltage ($V_0 = 800$ V) is insensitive to variation of loads due to closed loop control and small output voltage ripple. The MATLAB/Simulink calculated THD of the experimental input current waveform of the proposed converter is illustrated in Fig. 18. Figure 19 illustrates the measured efficiency comparison of the proposed soft and hard switched converters at different current ratings. The efficiency with proposed soft switched converter achieved is higher than 97% at the rated current. There is a clear improvement in efficiency of the proposed soft switched converter at different input currents. The efficiency of the proposed converter is satisfactory, even at light load. The switching losses of the semiconductor devices are less than 10% of the total power loss, which are calculated from the experimental prototype using Power MOSFET SYT139N65M5.

Hence, the simulation and experimental results verify that the proposed converter scheme is completely soft switched. The resonant circuit plays a vital part in realizing soft switching conditions for the proposed circuit. The resonant inductor causes semiconductor switch to turn on at ZCS and at the same time softly turns off the rectifier diode. The resonant capacitor

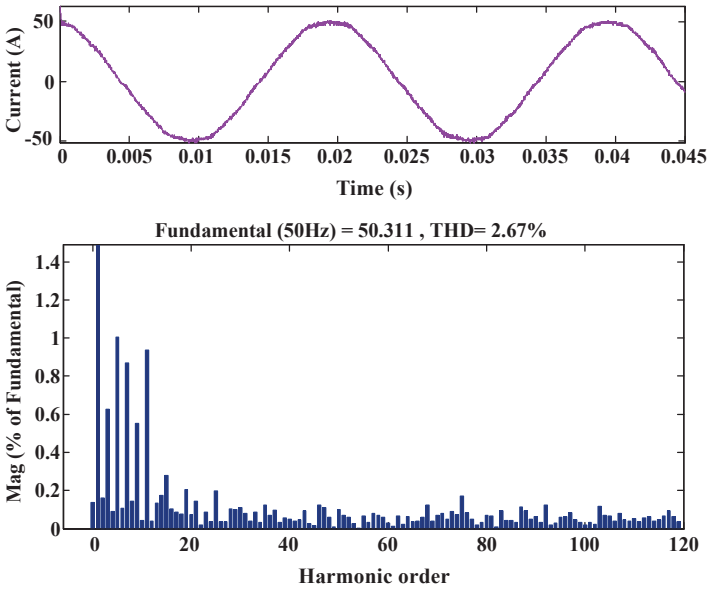

Fig. 18. THD_I of the proposed soft switched PWM AC/DC converter

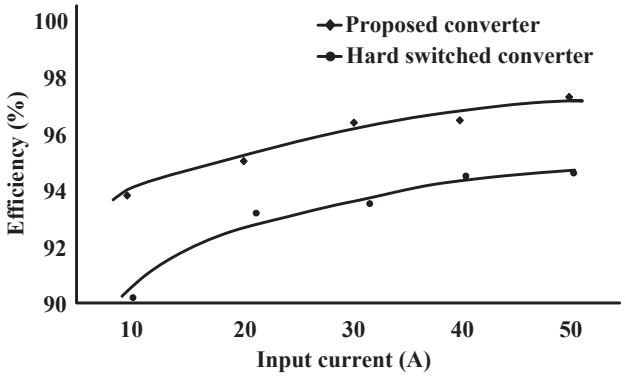

Fig. 19. Efficiency comparison of the proposed soft switched and hard switched PWM AC/DC converters

causes switch diode to commutate softly and semiconductor switch to turn off with ZVS. The rectifier diode is softly turned on, when resonant circuit retains its initial state (i.e resonant capacitor charges to its peak voltage value and current in resonant inductor reduces to zero). Moreover, the proposed converter scheme operates with almost unity power factor along with improved THD_I and efficiency.

8. Conclusion

This paper has investigated a soft switched PWM AC/DC boost rectifier topology. The soft switching behavior along with assessment of power quality parameters (THD_I, PF) of the proposed converter has been validated by simulation and experimental results. A procedure for comparison of the proposed topology with some prior art high power boost rectifier topologies has been illustrated for a given set of specifications.

The performance evaluated on the basis of parameters such as voltage and current stresses, sizes of energy storage devices, components count, power quality parameters and efficiencies suggested that the proposed converter is better than the prior art high power converters in terms of capacities of energy storage devices, current THD, power factor and total power loss. The proposed converter showed THD_I of 2.45% and the highest efficiency of 98.76% at rated load condition.

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