ARCHIVES OF ELECTRICAL ENGINEERING VOL. 70(1), pp. 203–218 (2021)

DOI 10.24425/aee.2021.136062

# Improved virtual space vector modulation for neutral point voltage oscillation and common-mode voltage reduction in neutral point clamped three-level inverter

JUNLONG FANG, GUANGYA WANG, RAN LI, SIYUAN LIU, SHUYU WANG

*School of Electricity and Information, Northeast Agricultural University*
*China*

*e-mails: junlongfang@126.com, wgy1187825293@163.com, 1187825293@qq.com*

(Received: 03.04.2020, revised: 23.10.2020)

**Abstract:** The neutral point clamped (NPC) three-level inverter is widely used in high-voltage and high-power applications. However, neutral point voltage oscillation (NPVO) and common-mode voltage (CMV) problems exist in the NPC three-level inverter. In this paper, an improved virtual space vector modulation (VSVM) is proposed based on the reconstruction of a virtual small vector and a virtual medium vector. Compared with the traditional VSVM, an improved VSVM can effectively reduce the CMV. On this basis, a vector conversion method is proposed to further reduce the NPVO in the whole range. Simulation results verify the effectiveness and superiority of the improved VSVM.

**Key words:** three-level inverter, vector conversion, virtual space vector modulation

## 1. Introduction

Compared with traditional inverters, neutral point clamped (NPC) three-level inverters have better output waveform, a lower distortion rate, and low voltage stress of switching components, which have been widely used in the photovoltaic grid-connected system, motor drive, wind power generation, and other middle and high voltage fields [1, 2]. Due to the neutral point voltage oscillation (NPVO) and common-mode voltage (CMV), the overall performance of the NPC three-level inverter is limited, and the security and stability of the system operation are affected [3, 4].

There are two design methods to deal with the NPVO and CMV of the NPC three-level inverter, namely a hardware method and software method [5–7]. The hardware method requires additional

circuit design, resulting in cost and size disadvantages [8]. As a result, the software method is more popular. The software method is mainly used to reduce the NPVO and CMV by improving the modulation strategy. In [9], the neutral point voltage (NPV) control method based on the carrier-based pulse width modulation (CBPWM) was proposed. But the control effect of these methods is subject to the modulation index $m$ and power factor (PF). The relationship between the CBPWM and SVM is analyzed in [10]. In [11, 12], several improved modulation strategies are proposed based on the SVM. The main design idea is to control the NPV by distributing the duty ratio of the redundant state of a small vector. However, when $m$ is very high or very low, the redundant state of a small vector does not always exist in some modulation sectors, resulting in the low-frequency oscillation of the NPV.

To overcome the shortcomings of the CBPWM and SVPWM, the virtual space vector pulse width modulation (VSVM) is proposed in [13]. In [14], The VSVM based on an imbalance factor is proposed. Although the methods proposed in the paper have certain effects on the NPVO, they will lead to the problem of an excessive CMV. The CMV generated by the output side of the NPC three-level inverter has a certain influence on the operation performance of motors [15–17]. Higher CMV on the motor axis will induce a high amplitude of shaft voltage, and shaft current, damage insulation, shorten the motor service life [18, 19]. In [20], a new virtual vector construction method is proposed. Since virtual medium vectors are not constructed in this method, the switching between vector sequences cannot be smooth during modulation, which leads to output waveform distortion.

The main contributions of this paper are as follows:

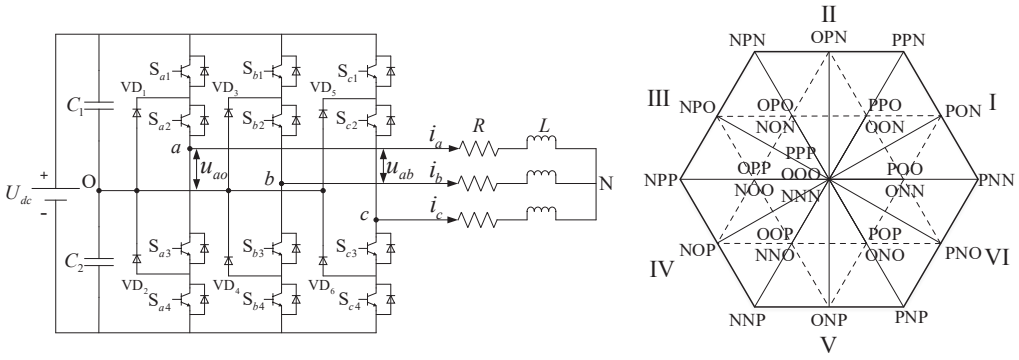
1. By improving the virtual vector construction method, the neutral point current, as the most important factor causing the NPVO, is effectively controlled.
2. In the design of the modulation sequence, the amplitude of the CMV is reduced to less than by carefully selecting the basic space vector.
3. A vector conversion method for the improved VSVM proposed is analyzed and designed to eliminate the influence of switching delay and insertion of dead-time in practice, thus further reducing the NPVO.

## 2. NPC three-level inverter

### 2.1. Working principle

Fig. 1(a) shows that the three-phase current of the NPC three-level inverter represents $i_a$, $i_b$ and $i_c$, respectively, and the direction of the output inverter is the positive direction of the current. The NPC three-level inverter consists of three bridge arms, including 12 power switching tubes and 6 diodes. The three output states are, respectively, P(1), O(0), and N(–1), which can be obtained by controlling four switching tubes ($s_{x1}\sim s_{x4}$, $x = abc$) on each phase bridge arm. The switching function $S_x$ can be expressed as:

$$S_x = \begin{cases} 1 & (s_{x1}, s_{x2}, s_3, s_{x4}) = (1, 1, 0, 0) \\ 0 & (s_{x1}, s_{x2}, s_3, s_{x4}) = (0, 1, 1, 0) \\ -1 & (s_{x1}, s_{x2}, s_3, s_{x4}) = (0, 0, 1, 1) \end{cases}. \tag{1}$$




(a) (b)

Fig. 1. The NPC three-level inverter

The NPC three-level inverter contains three-phase bridge arms, which means there are 27 different output results, namely 27 space vectors, as shown in Fig. 1(b). According to the length of the vector, the space vector can be divided into four types. Besides, according to the different phase angles of the space vector, the basic vector diagram can be divided into 6 sectors (I to VI), including 30 subsectors. The voltage between the DC side neutral point O and the load neutral point N is known as the CMV, which is defined as:

$$U_{com} = \frac{U_{dc}}{6}\left(S_a + S_b + S_c\right). \tag{2}$$

In the above formula, $S_a$, $S_b$, and $S_c$ are the switching functions of each phase bridge arm, respectively, and $U_{dc}$ is the DC bus voltage. 27 output states were analyzed respectively to obtain the CMV generated by each output state, as shown in Table 1.

Table 1. Analysis of switching states

| **Vector** | **Basic vector** | **CMV** |
|---|---|---|
| Large vector | PNN(0) NPN(0) NNP(0) | $\pm U_{dc}/6$ |
| | PPN(0) NPP(0) PNP(0) | |
| Medium vector | PON($i_b$) OPN($i_a$) NPO($i_c$) NOP($i_b$) ONP($i_a$) PNO($i_c$) | 0 |
| Small vector | ONN($i_a$) NON($i_b$) NNO($i_c$) | $\pm U_{dc}/3$ |
| | PPO($i_c$) OPP($i_a$) POP($i_b$) | |
| | OON($-i_c$) NOO($-i_a$) ONO($-i_b$) | $\pm U_{dc}/6$ |
| | POO($-i_a$) OPO($-i_b$) OOP($-i_c$) | |
| Zero vector | PPP(0) NNN(0) | $\pm U_{dc}/2$ |
| | OOO(0) | 0 |

### 2.2. Traditional VSVM

The space vector diagram of sector I is shown in Fig. 2:

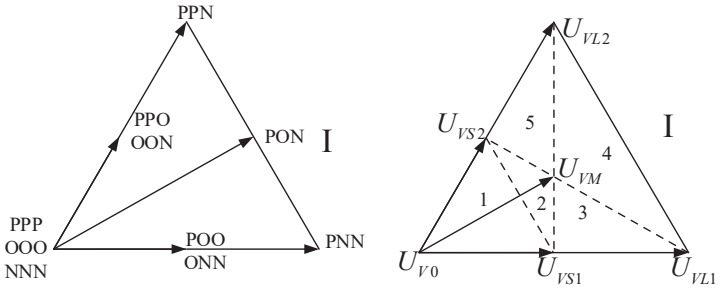



Fig. 2. The sector I diagram

a) Traditional virtual small vector

$$U_{VS1} = \frac{1}{2}\left(U_{\mathrm{ONN}} + U_{\mathrm{POO}}\right), \qquad U_{VS2} = \frac{1}{2}\left(U_{\mathrm{OON}} + U_{\mathrm{PPO}}\right). \tag{3}$$

b) Traditional virtual medium vector

$$U_{VM} = \frac{1}{3}\left(U_{\mathrm{ONN}} + U_{\mathrm{PPO}} + U_{\mathrm{PON}}\right). \tag{4}$$

c) Virtual large vector and virtual zero vector

$$U_{V0} = U_{\mathrm{OOO}}, \qquad U_{VL2} = U_{\mathrm{PNN}}, \qquad U_{VL2} = U_{\mathrm{PPN}}. \tag{5}$$

Although the traditional VSVM method has a certain effect on the NPVO, it has a high CMV. Also, in practice, there will be such factors as switch delay, dead zone setting, and component parameter asymmetry, resulting in the unsatisfactory effect of NPVO suppression.

## 3. Improved VSVM

Sector I, for example, shows the use of the proposed improved VSVM method to build novel virtual vectors, as shown in Fig. 3.

a) Improved virtual small vector

$$U_{VS1} = \frac{1}{2}\left(U_{\mathrm{OON}} + U_{\mathrm{PNO}}\right), \qquad U_{VS2} = \frac{1}{2}\left(U_{\mathrm{POO}} + U_{\mathrm{OPN}}\right). \tag{6}$$

In one control cycle, $i_{NP}$ of $U_{VS1}$ and $U_{VS2}$ can be obtained as:

$$i_{NP-VS1} = \frac{1}{2}(-i_c + i_c) = 0, \qquad i_{NP-VS2} = \frac{1}{2}(-i_a + i_a) = 0, \tag{7}$$

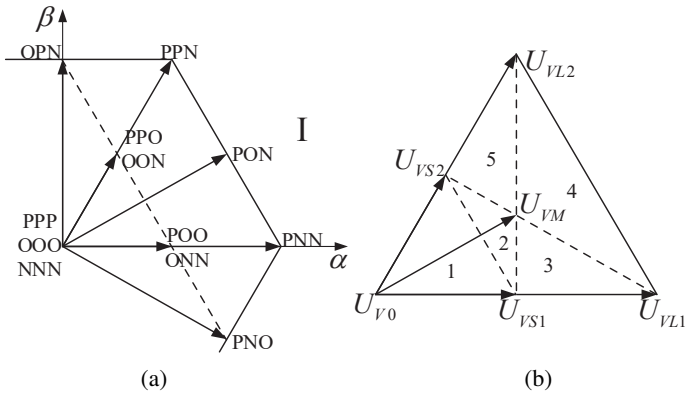



Fig. 3. The sector I diagram

where: $i_{NP-VS1}$ and $i_{NP-VS2}$ represent $i_{NP}$ generated by $U_{VS1}$ and $U_{VS2}$, respectively. For example, $U_{VS1}$ is synthesized by $U_{\mathrm{OON}}$ and $U_{\mathrm{PNO}}$ in equal proportions. $i_{NP}$, generated by $U_{\mathrm{OON}}$ and $U_{\mathrm{PNO}}$, is represented by $-i_c$ and $i_c$. Therefore, $i_{NP-VS1}$ is zero. Similarly, $i_{NP-VS2}$ is also zero in a control cycle.

b) Improved virtual medium vector

$$U_{VM} = \frac{1}{3}\left(U_{\mathrm{OPN}} + U_{\mathrm{PON}} + U_{\mathrm{PNO}}\right). \tag{8}$$

In one control cycle, $i_{NP}$ of $U_{VM}$ can be obtained as:

$$i_{NP-VM} = \frac{1}{3}(i_a + i_b + i_c) = 0, \tag{9}$$

where: $i_{NP-VM}$ is $i_{NP}$ generated by $U_{VM}$. $U_{VM}$ is synthesized by $U_{\mathrm{OPN}}$, $U_{\mathrm{PON}}$ and $U_{\mathrm{PNO}}$ in equal time, and $i_{NP}$, generated by them, is represented by $i_a$, $i_b$ and $i_c$, respectively. Therefore, $i_{NP-VM}$ is zero in a control cycle.

c) Virtual large vector and virtual zero vector

$$U_{VL1} = U_{\mathrm{PPN}}, \quad U_{VL1} = U_{\mathrm{PNN}}, \quad U_{V0} = U_{\mathrm{OOO}}. \tag{10}$$

$i_{NP}$, generated by a virtual large vector and virtual zero vector, is zero.

The reference voltage vector $U_{\mathrm{ref}}$ located in subsector I-3 as an example, is shown in Fig. 4. In this subsector, $U_{VS1}$, $U_{VM}$, and $U_{VL1}$ are used to synthesize $U_{\mathrm{ref}}$. The synthesis rule is expressed as:

$$\begin{cases} U_{VS1}T_{VS1} + U_{VM}T_{VM} + U_{VL1}T_{VL1} = U_{\mathrm{ref}}T_S \\ T_{VS1} + T_{VM} + T_{VL1} = T_S \end{cases}, \tag{11}$$

where: $T_{VS1}$, $T_{VM}$ and $T_{VL1}$ represent the dwell time of $U_{VS1}$, $U_{VM}$, and $U_{VL1}$, respectively. It can be seen that the CMV of $U_{VS1}$, $U_{VM}$ and $U_{VL1}$ is $\pm\frac{u_{dc}}{6}$, $\pm\frac{u_{dc}}{6}$ and 0, respectively, and $T_S$ is the switching frequency.

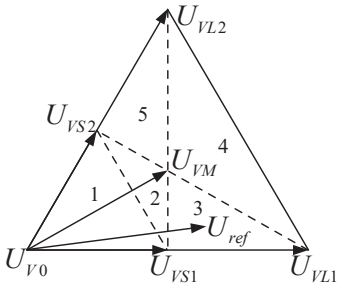



Fig. 4. State of the virtual space vector diagram in I sector

In one control cycle, $i_{NP}$ can be obtained as:

$$i_{NP} = i_{NP-VS1} + i_{NP-VM} + i_{NP-VL1} = 0, \tag{12}$$

where: $i_{NP-VS1}$, $i_{NP-VM}$ and $i_{NP-VL1}$ are $i_{NP}$ generated by $U_{VS1}$, $U_{VM}$ and $U_{VL1}$, respectively. Since $i_{NP-VS1}$, $i_{NP-VM}$ and $i_{NP-VL1}$ are zero, $i_{NP}$ is zero when $U_{\text{ref}}$ is located in subsector I-3. Besides, in the improved method, only basic vectors with a low CMV are selected, so only a low CMV will be generated during the modulation process. Vector sequences of the improved VSVM are as shown in Table 2.

Table 2. 1 sector switching sequences in subsectors

| Subsector | Vector sequence |
|---|---|
| 1 | OPN → OON → OOO → POO → PNO → POO → OOO → OON → OPN |
| 2 | OPN → OON → PON → POO → PNO → POO → PON → OON → OPN |
| 3 | OPN → OON → PON → PNN → PNO → PNN → PON → OON → OPN |
| 4 | OPN → PPN → PON → PNN → PNO → PNN → PON → PPN → OPN |
| 5 | OPN → PPN → PON → POO → PNO → POO → PON → PPN → OPN |

## 4. Vector conversion

Since $i_{NP}$ of the improved method is zero during each control cycle, the NPVO is eliminated in theory. However, in practice, there will inevitably be errors in upper and lower capacitance values, switching delay, and so on, which will lead to the NPVO. Therefore, it is necessary to study this problem. To further enhance the performance of reducing the NPVO, a novel method named vector conversion is proposed in this paper. When the NPVO occurs, the voltage of $C_1$ and $C_2$ is no longer equal. The offset factor of the NPV is indicated by $k(-1 < k < 1)$. Then, the voltage of $C_1$ and $C_2$ can be expressed as:

$$U_{C1} = \frac{(1-k)}{2} U_{dc}, \qquad U_{C2} = \frac{(1+k)}{2} U_{dc}, \tag{13}$$

where: $U_{dc}$, $U_{C1}$ and $U_{C2}$ are, respectively, the dc-link voltage, the voltage of $C_1$ and $C_2$.

To further reduce the NP voltage oscillation, on the premise of following the nearest three virtual vector principle (NTV$^2$) and without introducing new basic vectors, the existing vectors in a subsector are converted into equivalent vectors according to $k$. This process is used to generate the corresponding NP compensated current $i_{cmp}$ and reduce the NPVO.

It is shown, for example, when $U_{\text{ref}}$ is located in the subsector I-3. According to the NTV$^2$, the dwell time of the nearest three virtual vectors can be expressed as:

$$T_{VS1} = \left[2 - 2\sqrt{3}\sin\left(\frac{\pi}{6} + \theta\right)\right] T_S, \quad T_{VL1} = \left(\sqrt{3}\cos\theta - 1\right) T_S, \quad T_{VM} = (3\sin\theta)\, T_S\,. \tag{14}$$

In subsector I-3, the required virtual vectors are $U_{VS1}$, $U_{VM}$, and $U_{VL1}$, and the basic vectors involved are OPN, OON, PON, PNN, and PNO. It is worth noting that the following relationships exist in the vector sequence.

$$U_{\text{OON}} = \frac{2}{3}U_{\text{OPN}} + \frac{1}{3}U_{\text{PNO}}\,. \tag{15}$$

According to Table 2, the NP currents of $U_{\text{OON}}$, $U_{\text{OPN}}$ and $U_{\text{PNO}}$ can be obtained to be $-i_c$, $i_a$ and $i_c$, respectively. When $U_{\text{OON}}$ is converted to $U_{\text{OPN}}$ and $U_{\text{PNO}}$, that means decrease the dwell time of $U_{\text{OON}}$, and increase the dwell time of $U_{\text{OPN}}$ and $U_{\text{PNO}}$ at the same time. The NP compensated current $i_{com}$ in this process can be expressed as:

$$i_{cmp} = -(-i_c) + \frac{2}{3}i_a + \frac{1}{3}i_c = \frac{2}{3}i_a + \frac{4}{3}i_c\,. \tag{16}$$

The NP voltage offset $\Delta U$ is

$$\Delta U = \frac{1}{2}(U_{C_2} - U_{C_1}) = \frac{k}{2}U_{dc}\,. \tag{17}$$

To suppress the NPVO more, the average compensating current was applied. In a control cycle, the average compensated current $\bar{\imath}_{cmp+}$ and $\bar{\imath}_{cmp-}$ for $\Delta U > 0$ and $\Delta U \leq$ can be expressed as:

$$\bar{\imath}_{cmp\pm} = \frac{1}{2\pi}\int_0^{2\pi} i_{cmp\pm}(\omega t)\,\mathrm{d}\omega t = \pm\frac{1}{2\pi}\int_0^{2\pi}\left(\frac{2}{3}i_a(\omega t) + \frac{4}{3}i_c(\omega t)\right)\mathrm{d}\omega t. \tag{18}$$

When $\Delta U > 0$, that means $0 < k < 1$, it should lower the NP voltage. At this point, the direction of $i_{cmp}$ should be flowing out of the NP, namely $i_{cmp} > 0$. Based on (15) and (18), $U_{\text{OON}}$ is converted to $U_{\text{OPN}}$ and $U_{\text{PNO}}$, generating $\bar{\imath}_{cmp+}$. By controlling the action time of $\bar{\imath}_{cmp+}$, the purpose of eliminating the NPVO is achieved. The adjustment time $\Delta T$ can be obtained as:

$$\Delta T = C \cdot \frac{\Delta U}{\bar{\imath}_{cmp-}} = \frac{kCU_{dc}}{\bar{\imath}_{cmp-}}, \tag{19}$$

where: $C$ is the value of the capacitance on the dc side.

After the vector adjustment, the dwell time of OON, OPN, PNO is expressed as:

$$T'_{\mathrm{OON}} = \frac{1}{2}T_{VS1} - \Delta T, \quad T'_{\mathrm{OPN}} = \frac{1}{3}T_{VM} + \frac{2}{3}\Delta T, \quad T'_{\mathrm{PNO}} = \frac{1}{3}T_{VM} + \frac{1}{2}T_{VS1} + \frac{1}{3}\Delta T. \tag{20}$$

In Fig. 5, the adjustment of the residence time of the base vector is marked with red lines and blue arrows and it is notable that $T'_{\mathrm{OON}}$, $T'_{\mathrm{OPN}}$, $T'_{\mathrm{PNO}}$ should not be less than zero. The adjustment range of $\Delta T$ is as follows:

$$0 \geq \Delta T > -\frac{1}{2}T_{VM}\,. \tag{21}$$

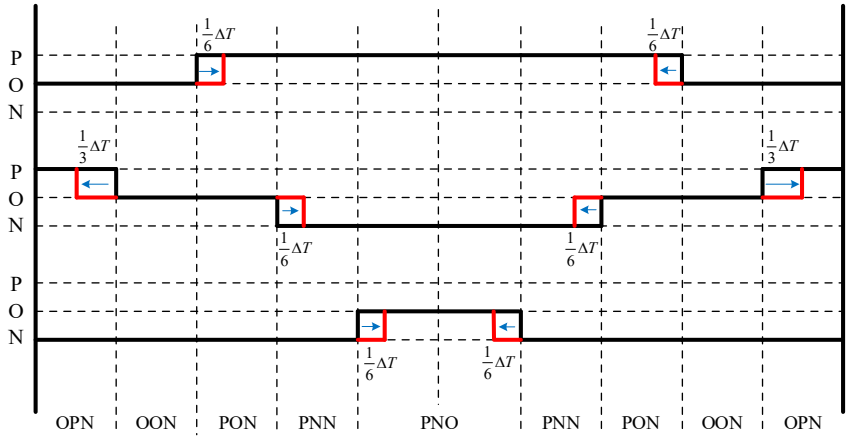



Fig. 5. The adjustment of $\Delta T$ when $\Delta U > 0$

Similarly, when $\Delta U \leq 0$, that means $-1 < k \leq 0$, it should raise the NP voltage. At this point, the direction of $i_{cmp}$ should be flowing into the NP, namely $i_{cmp} \leq 0$. Adjust the corresponding $\Delta T$ in the opposite direction. The vector conversion relationship in sector I, is as shown in Table 3. Similarly, other sectors can be analyzed in the same way.

Table 3. The vector conversion relationship in sector I

| **Subsector** | **Relationship** |
|---|---|
| 1 and 2 | $U_{\mathrm{OON}} = \frac{2}{3}U_{\mathrm{OPN}} + \frac{1}{3}U_{\mathrm{PNO}}, \quad U_{\mathrm{POO}} = \frac{1}{3}U_{\mathrm{OPN}} + \frac{2}{3}U_{\mathrm{PNO}}$ |
| 3 | $U_{\mathrm{OON}} = \frac{2}{3}U_{\mathrm{OPN}} + \frac{1}{3}U_{\mathrm{PNO}}$ |
| 4 | $U_{\mathrm{PON}} = \frac{1}{2}U_{\mathrm{PPN}} + \frac{1}{2}U_{\mathrm{PNN}}$ |
| 5 | $U_{\mathrm{POO}} = \frac{1}{3}U_{\mathrm{OPN}} + \frac{2}{3}U_{\mathrm{PNO}}$ |

## 5. Simulation and analysis

To verify the method proposed, a simulation model was established in Simulink, and different modulation coefficients were designed, as shown in Table 4.

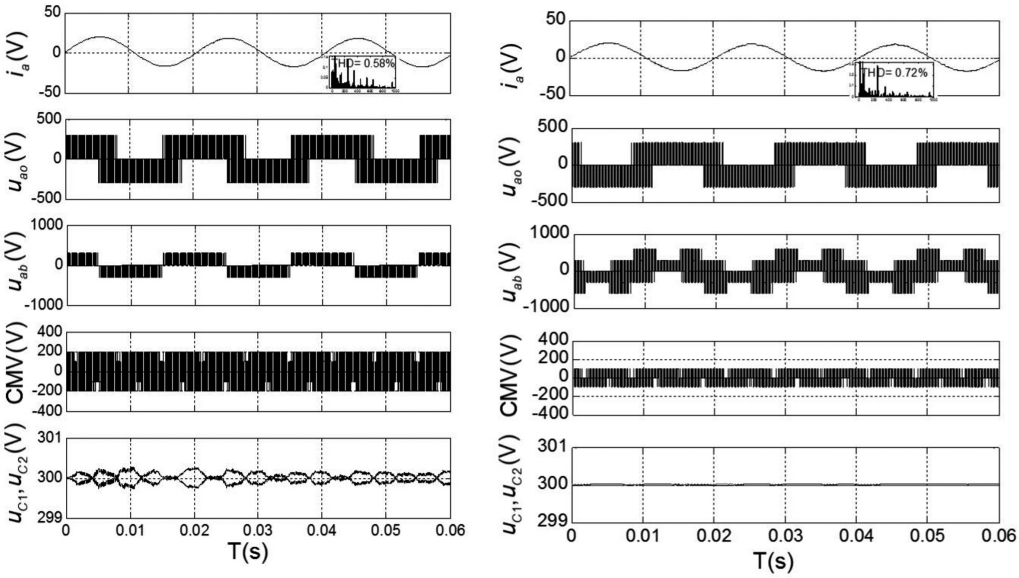
Table 4. Simulation coefficients

| Parameter name | Value |
|---|---|
| DC-link voltage ($U_{dc}$) | 600 V |
| $C_1, C_2$ | 1000 $\mu F$ |
| Load for low power factor (PF) | $2e^{\frac{j5\pi}{12}}\,\Omega$ ($R$ = 0.52Ω; $L$ = 6.15mH) |
| Load for high power factor (PF) | $2e^{\frac{j\pi}{12}}\,\Omega$ ($R$ = 1.93Ω; $L$ = 1.65mH) |
| Switching frequency | 8 000 Hz |
| Fundamental frequency | 50 Hz |

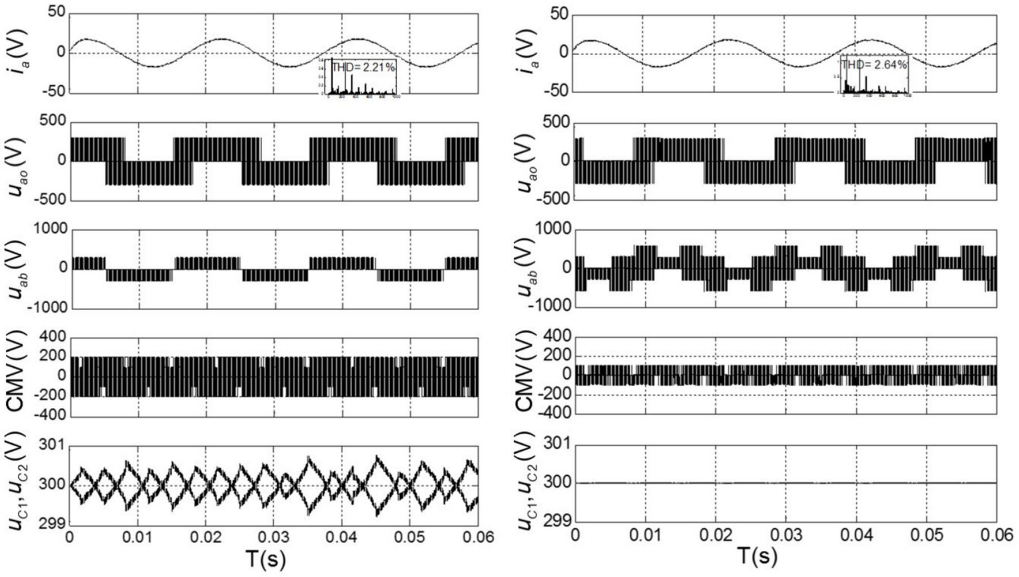
An NPC three-level inverter model modulated by traditional and improved VSVM methods was constructed in MATLAB/Simulink, and the simulation was carried out under the conditions of setting the modulation index $m$ $\left(m = \dfrac{\sqrt{3}U_{\text{ref}}}{U_{dc}}\right)$ to 0.1 and 0.9 and the power factor angle to $\dfrac{\pi}{12}$ and $\dfrac{5\pi}{12}$, respectively. According to the simulation results shown in Fig. 6 and Fig. 7, it can be seen that the improved VSVM method can suppress the CMV from $\dfrac{\pm U_{dc}}{3}$ (±200 V) to $\dfrac{\pm U_{dc}}{6}$ (±100 V) in a full range, which effectively controls the amplitude of the CMV. Also, by observing the voltage values of $C_1$ and $C_2$ in a stable state, it can be known that the NPVO is further suppressed. In the modulation cycle, the traditional method and the improved method only involve five switching states in each subsector, and the switch sequence changes one level at a time, so the switching loss can be roughly considered to be the same. To verify this view, taking $m = 0.9$ and $\varphi = \dfrac{\pi}{12}$ as an example, the switching loss under traditional and improved modulation methods was simulated, and the simulation results were shown in Fig. 8. By observing Fig. 9, it can be found that the switching loss waveforms of the two modulation methods are basically consistent, which verifies the previous theoretical analysis. By analyzing the total harmonics distortion (THD) of the two modulation methods, it can be found that the THD produced by the improved VSVM method is slightly larger than that produced by the traditional VSVM method.

It can be observed that when $m = 0.9$, the CMV under the improved VSVM method proposed in this paper presents an obvious periodic change. Here's an explanation for this change. When $m = 0.9$, the running trajectory of $U_{\text{ref}}$ is shown as the red dash line in Fig. 9.

The amplification sector shown in the figure above is taken as an example. When $U_{\text{ref}}$ is located in the region surrounded by the blue dash line and the green dash line, namely I–3, I–5, II–3, VI–5, the vector sequence and the CMV are shown in Table 5.

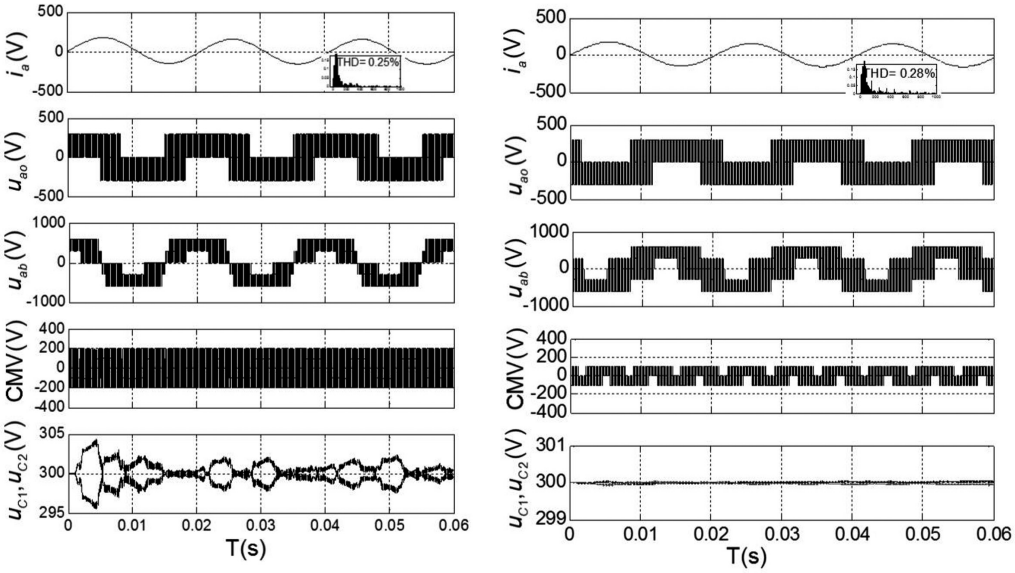



(a) $\varphi = \dfrac{5\pi}{12}$ traditional (b) $\varphi = \dfrac{5\pi}{12}$ improved

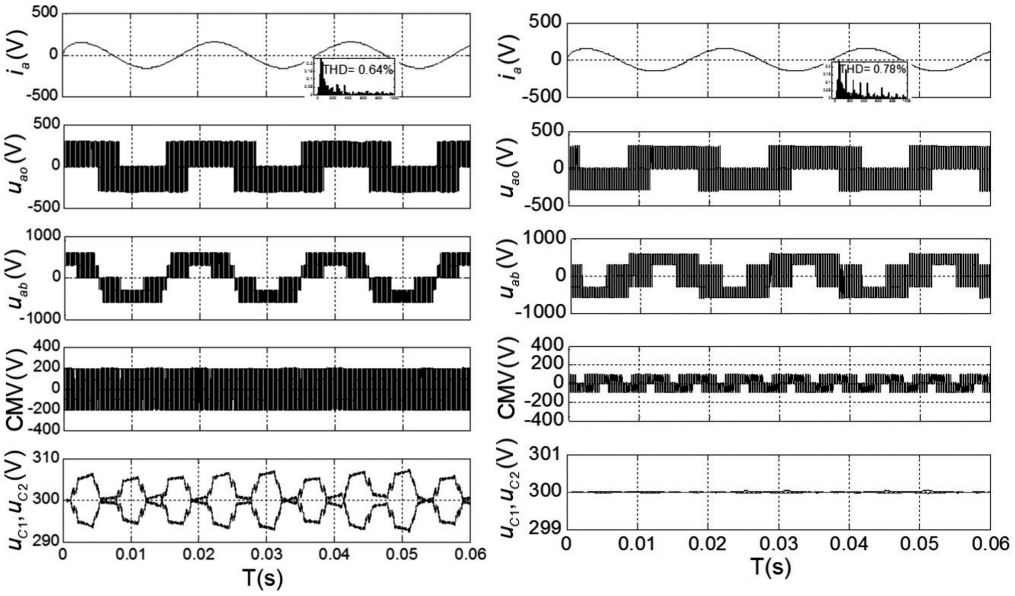



(c) $\varphi = \dfrac{\pi}{12}$ traditional (d) $\varphi = \dfrac{\pi}{12}$ improved

Fig. 6. Simulation waveform when modulation index $m = 0.1$

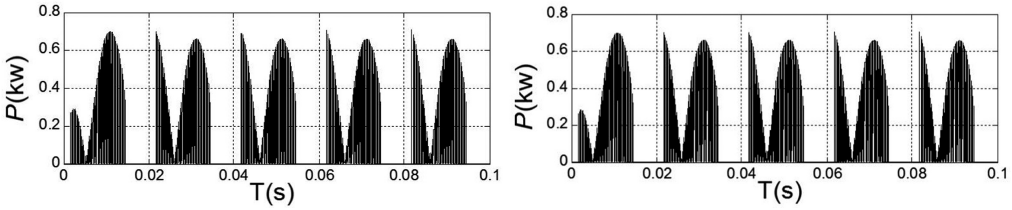



(a) $\varphi = \dfrac{5\pi}{12}$ traditional (b) $\varphi = \dfrac{5\pi}{12}$ improved



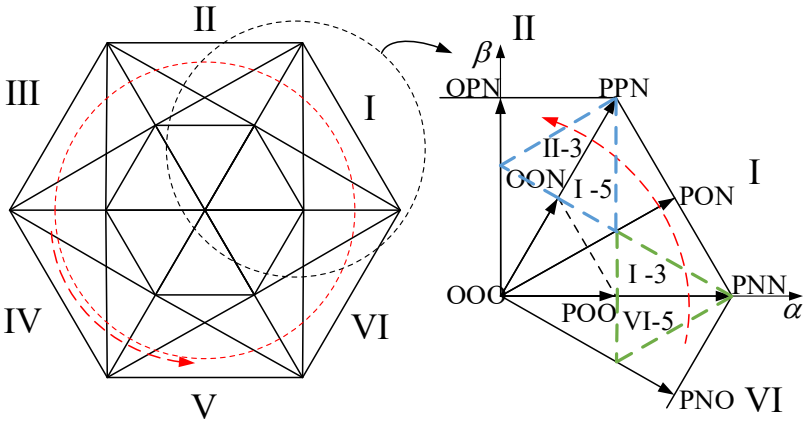

(c) $\varphi = \dfrac{\pi}{12}$ traditional (d) $\varphi = \dfrac{\pi}{12}$ improved

Fig. 7. Simulation waveform when modulation index $m = 0.9$




(a) $\varphi = \frac{\pi}{12}$ traditional (b) $\varphi = \frac{\pi}{12}$ improved

Fig. 8. The simulation waveform of switching loss when modulation index $m = 0.9$




(a) (b)

Fig. 9. The running trajectory of $U_{\text{ref}}$ when the modulation index $m = 0.9$

Table 5. Analysis of CMV under the improved VSVM when the modulation index $m = 0.9$

| Color | Subsector | Vector sequence | CMV |
|---|---|---|---|
| blue | I – 5 | OPN→PPN→PON→POO→PNO→POO→PON→PPN→OPN | $(0, U_{dc}/6)$ |
| | I – 3 | NPO→OPO→OPN→PPN→PNO→PPN→OPN→OPO→NPO | |
| green | I – 3 | OPN→OON→PON→PNN→PNO→PNN→PON→OON→OPN | $(-U_{dc}/6, 0)$ |
| | I – 5 | PON→PNN→PNO→ONO→ONP→ONO→PNO→PNN→PON | |

When $U_{\text{ref}}$ is located in the 4 subsector of each large sector, the CMV generated is in the range of $(-U_{dc}/6,\ U_{dc}/6)$. Therefore, when the modulation index is 0.9, the CMV of the improved VSVM changes according to the law of $(0,\ 100) - (-100,\ 100) - (-100,\ 0) - (-100,\ 100) - (0,\ 100)\ldots$, presenting the periodic change as shown in the Fig. 11, in which the blue dash line and the green dash line in Fig. 10 correspond to regions X and Y, respectively.

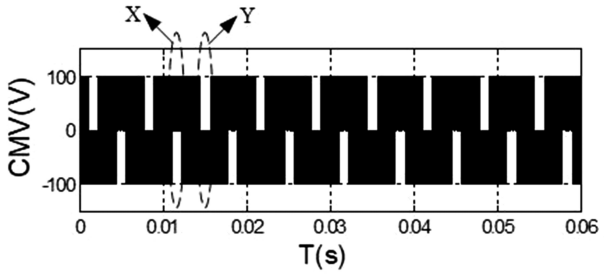
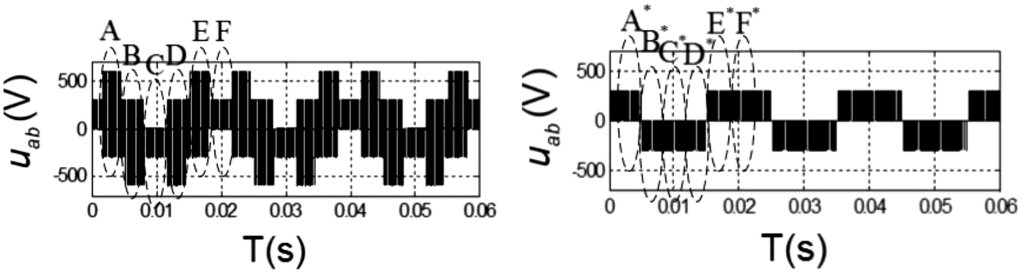



Fig. 10. CMV waveform of the improved VSVM when the modulation index $m = 0.9$

By observing Fig. 6 and Fig. 7, it can also be found that under the modulation of the traditional VSVM method and improved VSVM method, the waveform of the line voltage $u_{ab}$ is greatly different. When $m = 0.1$, $U_{\text{ref}}$ will only be located in 1 subsector of each sector (I to VI) in a modulation period. In the modulation process of the improved VSVM method, when $U_{\text{ref}}$ is located in the region I – 1, NPO, OPO, OOO, OON, and PON are selected to synthesize $U_{\text{ref}}$. According to the switching function in Equation (1), the basic vector can be defined as (−1, 1, 0), (0, 1, 0), (0, 0, 0), (0, 0, –1), (1, 0, –1). Then $S_a - S_b$ of these 5 switching functions are $-2(-U_{dc})$, $-1(-U_{dc}/2)$, 0(0), 0(0), $(1U_{dc}/2)$, respectively, which means that the range of the line voltage $u_{ab}$ when modulating in this subsector is $(-U_{dc},\ U_{dc}/2)$. The analysis is similar in other subsectors. When $m = 0.1$, the range of $u_{ab}$ within each modulation sector is shown in Table 6, and the simulation waveform is shown in Fig. 11.




(a) Improved VSVM (b) Traditional VSVM

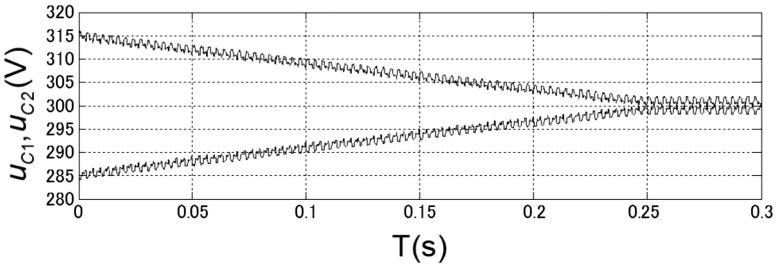
Fig. 11. The diagram of $u_{ab}$ when $m = 0.1$

To further verify the ability of the improved VSVM method to balance the NPV, take $m = 0.9$ and $\varphi = \dfrac{\pi}{12}$ as an example, and set the initial voltage values of $C_1$ and $C_2$ as $U_{C_1} = 315$ V and $U_{C_2} = 285$ V, respectively, for simulation. According to the simulation results shown in Fig. 12, it can be found that it takes about 0.25 s for the NPV to reach equilibrium under the traditional method modulation. However, with the improved method, the NPV balance only takes 0.06 s.

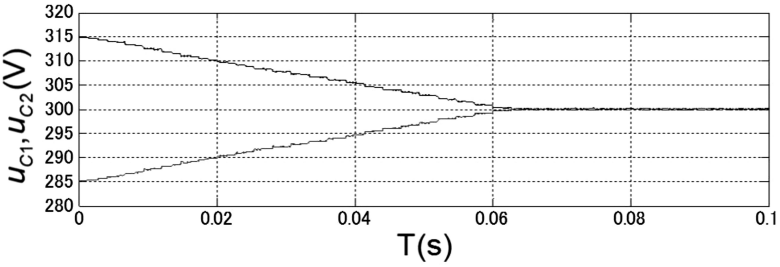
The simulation is established in four extreme environments, the modulation index $m$ is 0.1 and 0.9 respectively, and the power factor angle $\varphi$ is $\dfrac{\pi}{12}$ and $\dfrac{5\pi}{12}$, respectively. The phase current,

Table 6. $u_{ab}$ in these two modulation methods when $m = 0.1$

| Subsector | Improved | Traditional |
|---|---|---|
| I – 1 (A, A*) | $(-U_{dc}/2, U_{dc})$ | $(0, U_{dc}/2)$ |
| I – 1 (B, B*) | $(-U_{dc}, U_{dc}/2)$ | $(-U_{dc}/2, 0)$ |
| I – 1 (C, C*) | $(-U_{dc}/2, 0)$ | $(-U_{dc}/2, 0)$ |
| I – 1 (D, D*) | $(-U_{dc}, U_{dc}/2)$ | $(-U_{dc}/2, 0)$ |
| I – 1 (E, E*) | $(-U_{dc}/2, U_{dc})$ | $(0, U_{dc}/2)$ |
| I – 1 (F, F*) | $(0, U_{dc}/2)$ | $(0, U_{dc}/2)$ |




(a) The NPV of traditional VSVM




(b) The NPV of improved VSVM

Fig. 12. Simulation waveform of the NPV

phase voltage, line voltage, CMV, and NP voltage of the NPC three-level inverter are compared under the control of the two methods. The simulation results show that the improved VSVM method can reduce the CMV and NPVO.

## 6. Conclusions

An improved VSVM is proposed for the CMV and NPVO of NPC three-level inverters in this paper. By selecting the basic vector with a low CMV, virtual vectors are constructed, so that the CMV is effectively suppressed, and it is limited from $\frac{\pm U_{dc}}{3}$ to $\frac{\pm U_{dc}}{6}$. On the premise of ensuring

that the average neutral point current is 0 in the modulation process, and considering the influence of the NPVO on the space vector, a new virtual vector is constructed. It is verified that the virtual vector will not deviate due to the NPVO, and the error caused by the synthetic reference voltage vector is avoided. Besides, to eliminate the influence of non-ideal factors, such as switching delay and insertion of dead-time, a vector conversion method for the improved VSVM proposed is analyzed and designed, which further reduces the NPVO. The effectiveness of the improved VSVM for reducing the NPVO and CMV is verified by simulation.

## Acknowledgements

This paper was supported by the Harbin Applied Technology Research and Development Project (No. 2017RAXXJ075).

## References

[1] Zhang X., Wu X., Geng C., Ping X., Chen S., Zhang H., *An Improved Simplified PWM for Three-Level Neutral Point Clamped Inverter Based on Two-Level Common-Mode Voltage Reduction PWM*, IEEE Trans. Power Electronics, vol. 35, no. 10, pp. 11143–11154 (2020).

[2] Kaniewski J.Z., *Power flow controller based on bipolar direct PWM AC/AC converter operation with active load*, Archives of Electrical Engineering, vol. 68, no. 2, pp. 341–356 (2019).

[3] Beniwal N., Townsend C., Farivar G., Pou J., Ceballos S., Tafti H., *Band-Limited Three-Level Modulation for Balancing Capacitor Voltages in Neutral-Point-Clamped Converters*, IEEE Trans. Power Electronics, vol. 35, no. 9, pp. 9737–9752 (2020).

[4] Pham K., Nguyen N., *A Reduced Common-Mode-Voltage Pulsewidth Modulation Method With Output Harmonic Distortion Minimization for Three-Level Neutral-Point-Clamped Inverters*, IEEE Trans. Power Electronics, vol. 35, no. 7, pp. 6944–6962 (2020).

[5] Li C., Yang T., Kulsangcharoen P., Lo Calzo G., Bozhko S., Gerada C., Wheeler P., *A Modified Neutral-Point Balancing Space Vector Modulation for Three-Level Neutral Point Clamped Converters in High Speed Drives*, IEEE Trans. Ind. Electronics, vol. 66, no. 2, pp. 910–921 (2019).

[6] Jordi Z., Josep P., Salvador C., *A Comprehensive Study of a Hybrid Modulation Technique for the Neutral-Point-Clamped Converter*, IEEE Trans. Ind. Electronics, vol. 56, no. 2, pp. 294–304 (2009).

[7] Nguyen T.K.T., Nguyen N.-V., Prasad N.R., *Eliminated common mode voltage pulse width modulation to reduce output current ripple for multilevel inverters*, IEEE Trans. Power Electronics, vol. 31, no. 8, pp. 5952–5966 (2016).

[8] Lee J.S., Lee K.B., *Time-Offset Injection Method for Neutral-Point AC Ripple Voltage Reduction in a Three-Level Inverter*, IEEE Trans. Power Electronics, vol. 31, no. 3, pp. 1931–1941 (2016).

[9] McGrath B.P., Holmes D.G., Meynard T., *Reduced PWM harmonic distortion for multilevel inverters operating over a wide modulation range*, IEEE Trans. Power Electronics, vol. 21, no. 4, pp. 941–949 (2006).

[10] Chen J., He Y., Hasan S.U., Liu J., *A comprehensive study on equivalent modulation waveforms of the SVM sequence for three-level inverters*, IEEE Trans. Power Electronics, vol. 30, no. 12, pp. 7149–7158 (2015).

[11] Choi U.M., Lee J.S., Lee K.B., *New modulation strategy to balance the neutral-point voltage for three-level neutral-clamped inverter systems*, IEEE Trans. Energy Conversion, vol. 29, no. 1, pp. 91–100 (2014).

[12] Choi U.M., Lee K.B., Blaabjerg F., *Method to minimize the low frequency neutral-point voltage oscillations with time-offset injection for neutral-point-clamped inverters*, IEEE Trans. Ind. Appl., vol. 51, no. 2, pp. 1678–1691 (2015).

[13] Busquets-Monge S., Bordonau J., Boroyevich D., Somavilla S., *The nearest three virtual space vector PWM – A modulation for the comprehensive neutral-point balancing in the three-level NPC inverter*, IEEE Power Electron. Lett., vol. 2, no. 1, pp. 11–15 (2004).

[14] Xiang C.Q., Shu C., Han D., *Improved Virtual Space Vector Modulation for Three-Level Neutral-Point-Clamped Converter with Feedback of Neutral-Point Voltage*, IEEE Trans. Power Electronics, vol. 33, no. 6, pp. 5452–5464 (2018).

[15] Mukherjee S., Giri S., Banerjee S., *An Improved Adjustable Modulation Strategy for Three-Level NPC Inverters Considering Dynamic Loading Applications*, IEEE Trans. Ind. Electronics, vol. 65, no. 10, pp. 3915–3925 (2018).

[16] Yonglong Zhang, Yuejun An, Guangyu Wang, Xiangling Kong, *Multi motor neural PID relative coupling speed synchronous control*, Archives of Electrical Engineering, vol. 69, no. 1, pp. 57–68 (2020).

[17] Peng S., Zhang G., Qin C., Zhou Z., Gu X., Xia C., *MPTC of NP-clamped three-level inverter-fed permanent-magnet synchronous motor system for NP potential imbalance suppression*, IET Electric Power Applications, vol. 14, no. 4, pp. 658–667 (2020).

[18] Qin C., Zhang C., Chen A., Xing X., *A space vector modulation scheme of the quasi-Z-source three-level T-type inverter for common-mode voltage reduction*, vol. 65, iss. 10, pp. 8340–8350 (2018).

[19] Pham K., Nguyen N., *A Reduced Common-Mode-Voltage Pulsewidth Modulation Method with Output Harmonic Distortion Minimization for Three-Level Neutral-Point-Clamped Inverters*, IEEE Trans. Ind. Electronics, vol. 35, no. 7, pp. 6944–6962 (2020).

[20] Xu X., Zheng Z., Wang K., Yang B., Li Y., *A Comprehensive Study of Common Mode Voltage Reduction and Neutral Point Potential Balance for a Back-to-Back Three-Level NPC Converter*, IEEE Trans. Power Electronics, vol. 35, no. 8, pp. 7910–7920 (2020).

[21] Jiang W., Wang P., Ma M., *A Novel Virtual Space Vector Modulation with Reduced Common-Mode Voltage and Eliminated Neutral Point Voltage Oscillation for Neutral Point Clamped Three-Level Inverter*, IEEE Trans. Ind. Electronics, vol. 67, no. 2, pp. 884–894 (2020).