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NTC THERMISTOR NONLINEARITY COMPENSATION USING WHEATSTONE BRIDGE AND NOVEL DUAL-STAGE SINGLE-FLASH PIECEWISE-LINEAR ADC

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Abstract

NTC thermistors are frequently used low in cost temperature sensors which provide some of the most desirable sensing features. However, due to the nonlinear static transfer function their sensitivity decreases with temperature increase, causing lower measurement accuracy in some regions of the measurement range. This paper proposes a method for NTC thermistor nonlinearity compensation using a Wheatstone bridge and a novel dual-stage single-flash piecewise-linear ADC. Both conversion stages are performed using the same flash ADC of a novel design based on a reduced number of comparators employed. In this manner, simpler design, lower production costs, higher compactness and lower power consumption of the linearizing ADC, are achieved. The proposed linearizing method is tested on the Vishay NTCLE413E2103F520L thermistor, in the range from 0°C to 100°C, and the obtained results confirmed the effectiveness of the method in measurement accuracy improvement: when the flash ADC of 10-bit resolution is employed the accuracy obtained is $7.4747 \cdot 10^{-5}$°C.

Keywords: comparator count, dual-stage linearization, flash ADC, NTC thermistor, measurement accuracy, Wheatstone bridge.

1. Introduction

NTC thermistors are non-linear temperature-dependent semi-conductive resistive sensors which are characterized by high accuracy and reliability, quick response and small dimensions. Their resistance decreases exponentially with an increase in temperature, *i.e.* they are resistors with a negative temperature coefficient. At the ambient temperature, their resistance varies from several kΩ to about 40 MΩ [1]. NTC sensors are mostly used in the range between −50°C and 200°C [1].

In comparison with metallic resistive temperature sensors, NTC thermistors have smaller size, higher sensitivity to temperature changes, higher resistance (readings are less affected by the resistance of the connecting wires), *etc*. For example, NTC thermistors have about ten times higher sensitivity in comparison with platinum resistive thermometers [2]. However, their sensitivity decreases with the temperature increase. For this reason, NTC thermistors are used for

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measurements in a narrower temperature ranges that are usually met in the fields of medicine, biology, meteorology, air conditioning, *etc*.

An NTC thermistor static transfer function $R(T)$ is very non-linear, which can be easily observed from Fig. 1. This figure presents static transfer function $R(T)$ and the sensitivity $S(T)$ of the Vishay NTCLE413E2103F520L thermistor [3], for the temperature range between 0°C and 100°C.

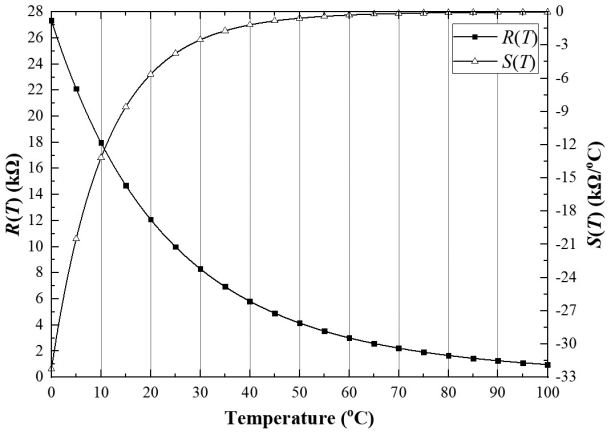

Fig. 1. Static transfer function $R(T)$ and sensitivity $S(T)$ of the Vishay NTCLE413E2103F520L thermistor.

The static transfer function $R(T)$ of this sensor, modelled with the Steinhart–Hart equation [4], is as follows:

$$R(T) = R_{25°\mathrm{C}} \cdot \exp\left(\mathrm{A} + \frac{\mathrm{B}}{T} + \frac{\mathrm{C}}{T^2} + \frac{\mathrm{D}}{T^3}\right), \tag{1}$$

where T is the measured temperature in [K], $R_{25°\mathrm{C}} = 10$ kΩ is the thermistor resistance at 25°C, and A = −12.89228328, B = 4245.148, C = −87493 and D = −9588114 are the Steinhart–Hart coefficients of the Vishay NTCLE413E2103F520L thermistor. The following equation gives the sensitivity dependence on the measured temperature:

$$S(T) = \frac{\mathrm{d}R(T)}{\mathrm{d}T} = -R(T) \cdot \left(\frac{\mathrm{B}}{T^2} + \frac{2\mathrm{C}}{T^3} + \frac{3\mathrm{D}}{T^4}\right). \tag{2}$$

Due to nonlinearity of the static transfer function, the sensitivity $S(T)$ of the NTC thermistor varies throughout the measurement range, *i.e*. its absolute value decreases with the temperature increase [1]. The goal of the linearization is to transform the nonlinear transfer function (dependence of the measured value on the input parameter) to a linear one and keep the sensitivity constant throughout the whole measurement range.

1.1. NTC thermistor linearization circuits

The common temperature measuring circuits based on NTC thermistors, called thermistor thermometers (also thermistor interfacing circuits), are usually derived in the form of a resistive voltage divider [5–7] or a Wheatstone bridge [1, 5, 6, 8, 9]. By using components of particular, pre-calculated values, these circuits perform compensation of thermistor nonlinearity over a narrow temperature range. However, the output of a thermistor thermometer circuit is a pseudo-linear

voltage [2, 5, 7], meaning that an additional linearization circuit is needed so higher measurement accuracy can be achieved. For this purpose, different linearizing schemes based on a 7555 timer [10], combination of a logarithmic amplifier, a differential amplifier and an analog divider [11], op-amp based inverting amplifier [12] were proposed. These linearization methods are known as analog, while there are digital linearization methods (such as *look-up table* (LUT)), and in recent years mixed-signal linearization methods have also been developed [13]. The mixed-signal linearization methods are performed by circuits which are known as nonlinear *analog-to-digital converters* (ADCs) [7, 9, 14–22]. The advantage of the nonlinear ADC application for sensor linearization is reflected in the fact that the same circuit performs two functions at the same time, *i.e.* sensor nonlinearity compensation and digitalization of the measurement result are performed simultaneously. In other words, shorter signal processing time is achieved in a cost effective and energy efficient manner. Moreover, the measurement result in the digital form becomes linearly dependent on the measured parameter.

Different architectures of nonlinear ADCs used for sensor linearization are proposed [7, 9, 15–22], providing the possibility for different sensor types to be linearized (NTC thermistors, resistive displacement sensors, magneto-resistive sensors, optical rotary encoders, humidity sensors, *etc.*). In [16], an NTC thermistor and an additional fixed resistor are used to determine input currents for a logarithmic amplifier, while its output voltage is brought to the input of a linearizing dual-slope ADC. As a result, the nonlinearity was reduced to ±0.2%. In [9], a dual-slope ADC was used to linearize the output of the Wheatstone bridge in the quarter-bridge configuration (one resistive sensor is employed) and in the half-bridge configuration (two resistive sensors are employed). By testing the dual-slope ADC with the quarter-bridge configuration, the nonlinearity error was found to be ±0.14% at worst. However, when a dual-slope ADC is in use, the compromise between low consumption and low sampling rate, need to be accepted.

In most cases, nonlinear ADCs have dual-stage architecture, where one stage performs linearization (its transfer function is the piecewise-linear approximation of the function inverse to the voltage generated by the sensor interfacing circuit), while the other stage reduces the quantization error introduced in the first stage. For this reason, these ADCs are often called dual-stage *piecewise-linear* (PWL) ADCs. A great number of dual-stage PWL ADCs have flash ADCs at both stages. The flash ADC is the fastest converter, but at the cost of higher complexity and power consumption which originate from a large number of employed preamplifiers and comparators, and it is known that operational amplifiers are great power consumers [18, 19, 21, 23, 24]. There are solutions for a dual-stage ADC which employ a flash ADC in the first stage, while the second stage of conversion is performed using an ADC of another type, such as a *successive approximation* (SAR) ADC [21]. In this particular case [21], the combination of flash and SAR ADC has lower power consumption in comparison with flash ADCs being employed at both stages. However, this ADC design has a longer signal processing time. There are other ways to reduce the complexity and power consumption of a dual-stage PWL ADC based on flash architecture and keep the processing time short [18, 19, 23, 24]. So far, several design modifications of the flash-based dual-stage PWL ADC have been proposed in order to reduce the number of employed comparators. One way is for both stages to be performed by the same flash ADC [18, 19] and another way is to reduce the number of comparators within one stage [22, 23]. In this paper, a novel design of the flash-based dual-stage PWL ADC, which combines both of the previously mentioned design modifications, is proposed. If a conventional design of the flash-based dual-stage PWL ADC can be named a *dual-stage dual-flash* (DSDF), then the ADC proposed in this paper should be named a *dual-stage single-flash* (DSSF) ADC. In the remainder of the paper the complete designing procedure of the proposed linearizing circuit (Wheatstone bridge thermistor thermometer and the DSSF PWL ADC) will be described.

2. The proposed linearizing circuit

In this paper, linearization of the Vishay NTC thermistor NTCLE413E2103F520L, is performed. Linearization is performed in the range between 0°C and 100°C, using a Wheatstone bridge and a DSSF PWL ADC with a flash ADC of compact design. The bridge output voltage, $V_1 - V_2$, is still nonlinear and has negative values, which is why it is fed to the input of a differential amplifier with the gain of –1 (see Fig. 2) before it is fed to the linearizing ADC. The amplifier output voltage $U(T) = -(V_1 - V_2)$ is S-shaped and has one inflection point [5, 7], where the temperature of the inflection point can be selected to reshape the voltage signal. It is important to note that the linearity of $U(T)$ is expressed most around the inflection point. In this way, the choice of the inflection point can influence the temperature range in which the linearity is the highest, even when only a Wheatstone bridge is used for linearization. Further linearization of $U(T)$ is performed in a DSSF PWL ADC, *i.e.* in its first stage with the transfer function which is the piecewise-linear approximation of the function inverse to the voltage $U(T)$.

2.1. Wheatstone bridge thermistor thermometer

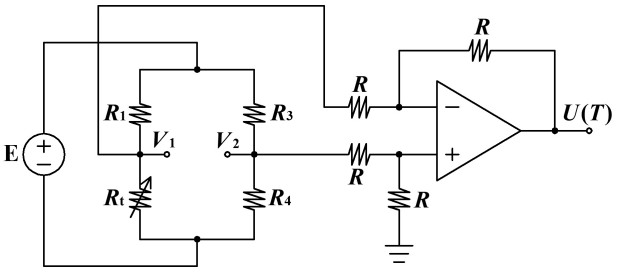

Fig. 2. Thermistor thermometer based on a Wheatstone bridge and a differential amplifier with the gain of –1.

The following calculations are needed in order to determine the values of the Wheatstone bridge parameters R_1, R_3, R_4 and E:

– The permissible operating current is the maximal current allowed through the NTC thermistor which will not cause the self-heating error higher than $\Delta T = 0.05$°C:

$$I_t = \sqrt{\frac{C_\mathrm{d} \cdot \Delta T}{(R_t)_\mathrm{min}}} = 0.418 \text{ mA}, \tag{3}$$

where $C_\mathrm{d} = 3$ mW/°C is the dissipation constant, and $(R_t)_\mathrm{min} = R_t(105°\mathrm{C}) = 858.33\ \Omega$ is the minimal thermistor resistance, which corresponds to the maximal temperature from the measurement range (for the specific thermistor the measurement range is from −40°C to 105°C).

– The value of resistor R_1 is obtained from the linearizing condition of the Wheatstone bridge, *i.e.* from $U''(T) = 0$ [2], and depends on the inflection point temperature T_{ip}:

$$R_1\left(T_{ip}\right) = R_t\left(T_{ip}\right) \cdot \frac{\beta\ [\mathrm{K}] - 2 \cdot T_{ip}\ [\mathrm{K}]}{\beta\ [\mathrm{K}] + 2 \cdot T_{ip}\ [\mathrm{K}]}, \tag{4}$$

where $\beta = \beta_{0/100} = 3399$ K is the thermistor material constant taken for the range between 0°C and 100°C, because thermistor linearization is performed in this specific range.

– From Fig. 2, the supply voltage E, which also depends on the selected inflection point temperature, can be expressed with:

$$E\left(T_{ip}\right) = I_t\left(R_1\left(T_{ip}\right) + R_t\left(T_{ip}\right)\right). \tag{5}$$

– The values of resistors R_3 and R_4 are derived from the bridge balancing condition for the temperature $T_{\min} = 0°\text{C}$ [8], *i.e.* when the following equality stands $U(T_{\min}, T_{ip}) = 0$ V. This condition is expressed with the following equation:

$$U\left(T_{\min}, T_{ip}\right) = 0\text{ V} = E\left(T_{ip}\right)\cdot\left(\frac{R_t(T_{\min})}{R_1(T_{ip}) + R_t(T_{\min})} - \frac{R_4}{R_3 + R_4}\right), \tag{6}$$

from where it finally follows:

$$\frac{R_3}{R_4} = \frac{R_1\left(T_{ip}\right)}{R_t\left(T_{\min}\right)}. \tag{7}$$

The values of resistors R_3 and R_4 are selected from E192 series of standard resistances (tolerance is 0.5%) defined by the IEC 60063:2015 standard [25], while condition (7) is satisfied. As the ratio (7) depends on the temperature of the inflection point T_{ip}, in Table 1 are given E192 standard values for R_1, R_3 and R_4, and the values of the supply voltage E, for three inflection points: 25°C, 50°C and 75°C.

Table 1. Wheatstone bridge parameters, linear approximation function and $U(T)$ percentage nonlinearity error NE [%] before linearization, for three different inflection points.

Inflection point temperature T_{ip} [°C]	**R_1 [Ω]**	**E [V]**	**R_3 [Ω]**	**R_4 [Ω]**	**Linear approximation function**	**NE [%]**
25°C	7590	3.53	383	1380	$U_{25°\text{C}}(T)$ [V] = $2.5935051 \cdot 10^{-6} + 0.0236156 \cdot T$ [°C]	14.5451
50°C	2840	1.55	135	1300	$U_{50°\text{C}}(T)$ [V] = $2.345775 \cdot 10^{-6} + 0.0100827 \cdot T$ [°C]	5.4690
75°C	1270	0.89	176	3790	$U_{75°\text{C}}(T)$ [V] = $8.735211 \cdot 10^{-7} + 0.0046414 \cdot T$ [°C]	14.2299

The nonlinearity error is specified for sensors with a transfer function which can be approximated by a straight line $y = a + bx$ [26]. Thus, nonlinearity is the maximal deviation of a real transfer function from a linear approximation function [27]. These approximation lines are given in Table 1, for each of the three considered inflection points. When a value of nonlinearity is given, it must always be emphasized in relation to which linear function that value is defined. One way to choose a linear approximation function is to use the endpoints of a real transfer function, *i.e.* to determine the sensor output for the minimal and maximal value of the sensor input, and then to draw a straight line between these two points. It can be seen from Fig. 3 that the nonlinearity error is the lowest near the endpoints, as well as near the inflection point.

For certain sensor applications, there can be a section of the measurement range which is of greater importance, so it is desirable to lower down the nonlinearity error as much as possible in that segment. This can be achieved by setting the inflection point in the middle of the segment of interest. Finally, the percentage nonlinearity error NE [%] is expressed as follows:

$$NE\text{ [\%]} = \frac{(\Delta U)_{\max}}{V_{\max}}\cdot 100\%, \tag{8}$$

where $(\Delta U)_{\max}$ represents the maximal deviation of the real transfer function from the approximation line (see Fig. 3), and $V_{\max} = (U(T))_{\max}$ is the maximal value, *i.e.* the full span of voltage $U(T)$ [17, 26]. In Table 1 are also given percentage nonlinearity errors NE [%] calculated for three inflection points.

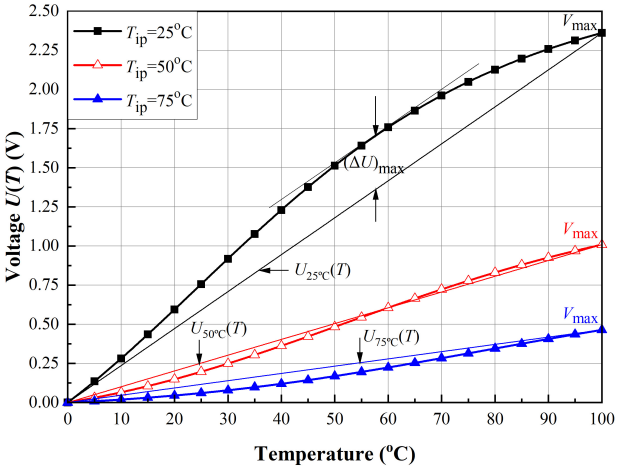

Fig. 3. Output voltage $U(T)$ before linearization and its linear approximation for three inflection points.

2.2. Designing principles of a dual-stage piecewise-linear ADC

The most representative feature of a dual-stage PWL ADC used for sensor linearization is that the first stage of conversion is conducted by a non-uniform ADC with a transfer function (quantization function) composed of linear segments of unequal width bounded by so-called break voltages [18, 20, 22]. These linear segments approximate the ideal first-stage ADC transfer function which is inverse to the input signal, *i.e.* inverse to the output voltage of the sensor interface circuit $U(T)$. The second stage is performed by a uniform ADC with its input range uniformly divided into cells of equal width.

Fig. 4 represents the ideal monotonically rising transfer function (continual black line) of the 4-bit dual-stage PWL ADC approximated by the linear segments of different width (red lines) bounded by non-uniformly distributed break voltages (red squares). For the particular case, each

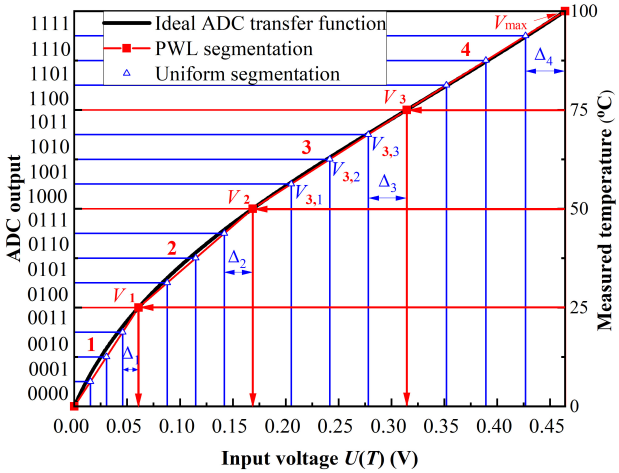

Fig. 4. Ideal transfer function of a dual-stage PWL ADC (black line); PWL approximation (red lines) with the break voltages (red squares) and uniform cell boundaries (blue triangles).

stage of A/D conversion has the resolution of $N = 2$ bits, meaning that there are 4 non-uniform segments, each consisting of 4 uniform cells. These very low resolutions are taken just for the simplicity of explanation. The values of break voltages are obtained by dividing the temperature range from $T_{\min} = 0°\text{C}$ to $T_{\max} = 100°\text{C}$ (right axes in Fig. 4) into 4 linear segments of equal width and by projecting their endpoints (for 25°C, 50°C and 75°C) on the voltage axes (voltages V_1, V_2 and V_3 in Fig. 4). In general, the break voltages can be determined as follows:

$$V_i = U(T_i), \quad T_i = T_{\min} + i \cdot \frac{T_{\max} - T_{\min}}{2^N}, \quad i = 1, \ldots, 2^N - 1. \tag{9}$$

For example, the third segment is bounded by V_2 and V_3, and within these boundaries equally wide cells are uniformly distributed. Cell boundaries are marked with $V_{k,j}$ ($V_{3,1}$, $V_{3,2}$ and $V_{3,3}$ for the third segment), where k represents the segment number and j represents the ordinal number of a cell boundary within the k-th segment. The cell boundaries (blue triangles) can be derived in the following manner:

$$V_{k,j} = V_{k\text{L}} + j \cdot \frac{V_{k\text{H}} - V_{k\text{L}}}{2^N} = V_{k\text{L}} + j \cdot \Delta_k, \quad k = 1, \ldots, 2^N, \quad j = 1, \ldots, 2^N - 1, \tag{10}$$

where $V_{k\text{L}}$ represents the lower segment boundary, $V_{k\text{H}}$ is the higher segment boundary, and Δ_k is the cell width in the k-th segment (Δ_1, Δ_2, Δ_3 and Δ_4 in Fig. 4). The width of the cells is constant throughout the segment, however, due to different widths of linear segments, cell widths are different between segments as well. As one can notice, this method for designing the dual-stage PWL ADC is not complex and does not require application of a microcontroller or any other kind of processing power. At the end of conversion, the belonging cell of the input voltage sample is determined and represented with the corresponding 4-bit digital code (left axes in the Fig. 4).

2.3. Proposed DSSF PWL ADC design

It is well known that an n-bit flash ADC of the conventional design employs $2^n - 1$ comparators. Accordingly, a dual-stage ADC with two flash ADCs of different resolution needs $2^{N1} - 1 + 2^{N2} - 1$ comparators, where N_1 and N_2 are the resolutions of the first and the second stage, respectively. The dual-stage ADC proposed in this paper has two conversion stages of the same resolution N, *i.e.* the total resolution is $2N$, while the number of employed comparators is $2^{(N-2)} + 1$. In this manner, the ADC with a more compact design and lower power consumption is obtained.

As an example, an 8-bit DSSF PWL ADC will be examined (see Fig. 5). In other words, a 4-bit flash ADC ($N = 4$) of modified design is used. The number of break voltages is $2^4 - 1 = 15$, *i.e.* from V_1 to V_{15}. These voltages are obtained using the resistive voltage divider network composed of resistors R_1 to R_{16} with mutually different resistances. Break voltages are derived from voltage V_{ref} which is equal to the maximal ADC input voltage $V_{\max} = (U(T))_{\max}$. The whole conversion process is controlled by synchronization signals S_i generated by the timing generator. The conversion is executed as follows: after taking a sample V_{in} of input voltage $U(T)$ (started by signal S_1), the sample is fed to the input of comparator C1 which determines whether the voltage sample belongs to the sub-range below or above the central break voltage, which is in this case V_8 (in the middle between V_1 and V_{15}). The C1 comparator output bit is D_3' (MSB bit of the final result), and if $D_3' = 1$ sample is above V_8, and if $D_3' = 0$ sample is below V_8. This bit controls a 2 to 1 analog multiplexer (AMUX) with input values V_{12} and V_4 which are actually central break voltages in the upper and lower sub-range (in relation to V_8) of the ADC input range, respectively. In other words, break voltages V_8, V_{12} and V_4 divide the ADC input range into four different sub-ranges. When $D_3' = 1$, the AMUX output is V_{12}, while for $D_3' = 0$ the output is V_4. In this

manner, the reference voltage of comparator C2, which determines the next bit D'_2, is obtained. D'_3 and D'_2 determine the outputs of three 4 to 1 AMUXs whose inputs are break voltages from the corresponding sub-ranges. The output voltages of three 4 to 1 AMUXs are reference voltages of comparators C3, C4 and C5. The comparators' outputs represent a thermometer code converted by the 2-bit priority encoder into two bits D'_1 and D'_0. After the first 4 bits $D'_3 - D'_0$ are fed into the register (controlled by signal S_2), the second stage of conversion follows (started by signal S_3).

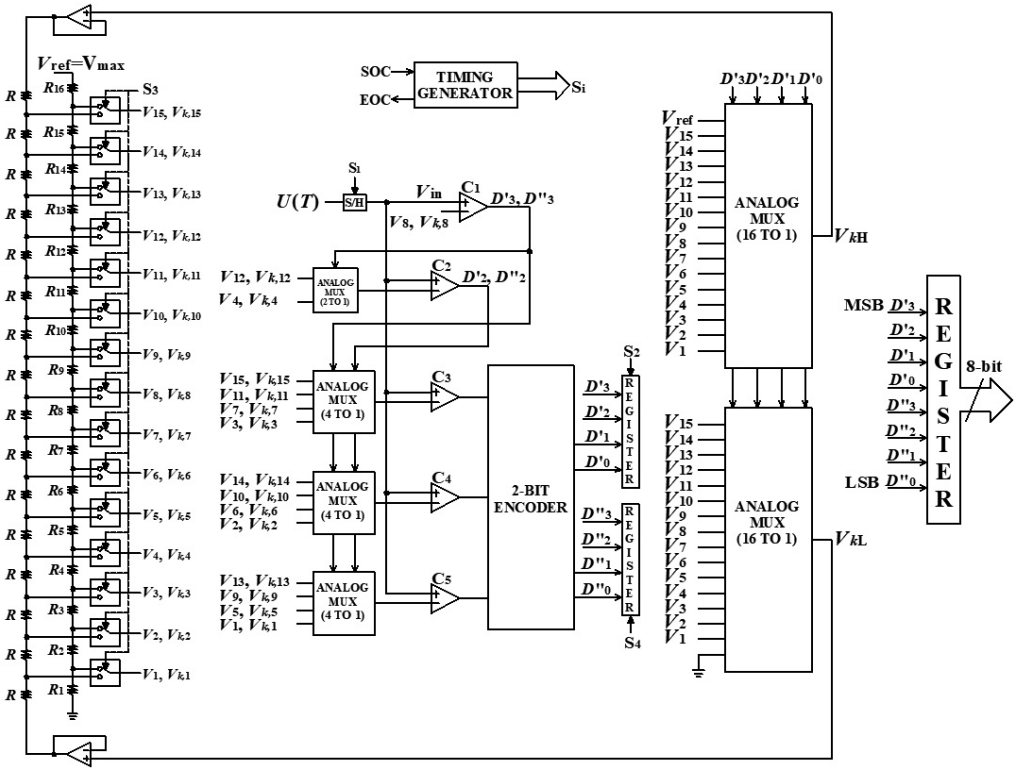

Fig. 5. The design of the proposed DSSF PWL ADC with 8-bit resolution.

The output bits of the first stage of conversion define the k-th non-uniform segment to which the current input sample V_{in} belongs. Additionally, the first-stage bits control the outputs of two 16 to 1 AMUXs. The outputs of these AMUXs are the boundaries $V_{k\text{L}}$ (lower) and $V_{k\text{H}}$ (higher) of the k-th non-uniform segment and, at the same time, boundaries of the input range of the second stage of conversion. The second stage of conversion is executed in exactly the same way as the first stage, the difference being that the conversion is performed within the boundaries of the k-th segment to which the current sample belongs. Synchronization signal S_3 controls the switches which select the appropriate resistive voltage divider network used for the generation of cell boundaries $V_{k,j}$ ($k = 1, \ldots, 2^N$ and $j = 1, \ldots, 2^N - 1$). Unlike the first stage, at the second stage of conversion the resistive voltage divider network consisting of resistors of mutually equal resistances R, is used. The corresponding cell to which the current sample belongs is now determined and encoded with 4 bits, D''_3-D''_0. After feeding these 4 bits into the register (directed by signal S4), the final 8-bit ADC output code is obtained.

3. Results and discussion

In order to highlight the advantages of the proposed DSSF PWL ADC with $2N$-bit resolution, it is compared to the *dual-stage dual-flash* (DSDF) PWL ADC of the same total resolution ($N_1 + N_2 = 2N$). The working principles of the proposed DSSF PWL ADC and DSDF PWL ADC, and their effectiveness in the linearization of the output voltage of the Wheatstone bridge with the Vishay NTCLE413E2103F520L thermistor are investigated using LabVIEW simulation software.

The front panel of a LabVIEW *virtual instrument* (VI) used for the simulation of the complete measurement system, from the NTC thermistor input to the ADC output, is presented in Fig. 6. At the very beginning of the simulation, it is necessary to set the values of resolutions N_1 and N_2, run the instrument, and then press the START button. To simulate a DSDF PWL ADC, the chosen resolutions N_1 and N_2 must be different, while to simulate DSSF PWL ADC, resolutions N_1 and N_2 need to be equal. The voltage at the output of the differential amplifier $U(T)$ is generated within the VI. Voltage samples are obtained for the set of input temperatures selected from the range between 0°C and 100°C with a certain step. The thermistor transfer function is simulated as well, since it affects the voltage $U(T)$. A linear approximation function of the voltage $U(T)$ (given in Table 1) is simulated within the VI as well as the ideal transfer function of the proposed ADC, which is an inverse function of voltage $U(T)$ (left side in Fig. 6). Additionally, the value of percentage nonlinearity error NE [%] of the voltage $U(T)$ before linearization is calculated (also given in Table 1). As a next step, the values of break voltages are generated and then used in the simulation of the first stage of A/D conversion where the comparisons between break voltages and input voltage sample are performed. As a result, the belonging segment of the current input voltage sample and its digital representation are determined. After determining the segment, *i.e.* its lower and higher boundary, the second stage of conversion follows where the ordinal number of the uniform cell to which the current sample belongs is determined and converted into the digital format. This procedure is repeated for each sample of input voltage $U(T)$. After the conversion is completed, the obtained digital code words ($N_1 + N_2$ bits long) are converted back to (measured) temperature values and compared to the corresponding values of

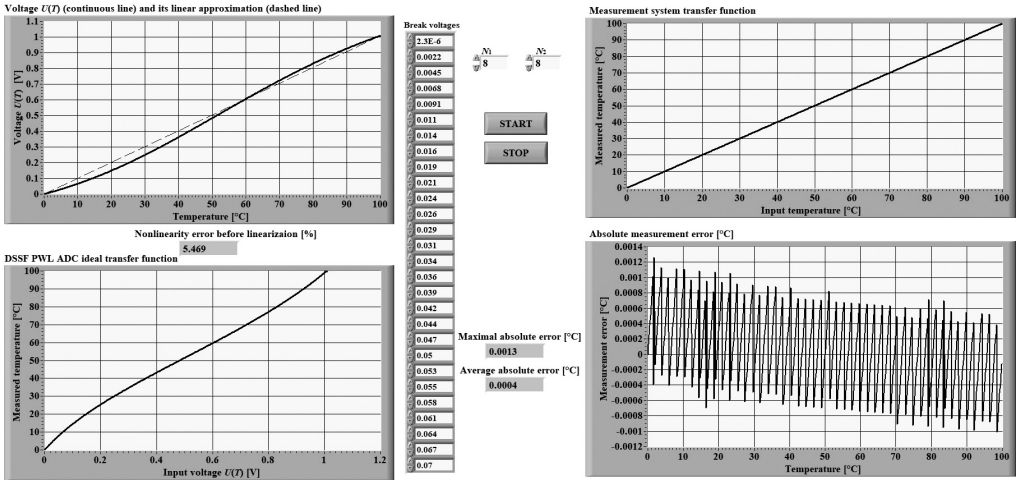

Fig. 6. Front panel of the virtual instrument used for the simulation of the proposed DSSF PWL ADC and DSDF PWL ADC.

input temperature. The difference between these values represents the measurement error. The absolute measurement error as a function of input temperature for the entire measurement range, and the transfer function of the entire measurement system are presented in Fig. 6. Also, the maximal absolute error $\Delta T_{\max}$ [°C] and the average absolute error in the whole measurement range ΔT_{avr} [°C] are calculated and given below in Tables 2 to 4, for three different inflection points of voltage $U(T)$.

Table 2. Maximal absolute error $\Delta T_{\max}$ [°C] and average absolute error ΔT_{avr} [°C] of temperature measurement after linearization for T_{ip} = 25°C.

Inflection point at T_{ip} = 25°C							
Dual-stage dual-flash PWL ADC				**Dual-stage single-flash PWL ADC**			
N_1	N_2	$\Delta T_{\max}$ [°C]	ΔT_{avr} [°C]	N	N	$\Delta T_{\max}$ [°C]	ΔT_{avr} [°C]
4	8	$1.275 \cdot 10^{-1}$	$4.87 \cdot 10^{-2}$	6	6	$2.16 \cdot 10^{-2}$	$6.8 \cdot 10^{-3}$
4	12	$1.196 \cdot 10^{-1}$	$4.87 \cdot 10^{-2}$	8	8	$1.2 \cdot 10^{-3}$	$4 \cdot 10^{-4}$
6	10	$8.1 \cdot 10^{-3}$	$3.1 \cdot 10^{-3}$				
4	16	$1.189 \cdot 10^{-1}$	$4.87 \cdot 10^{-2}$	10	10	$7.0795 \cdot 10^{-5}$	$2.6134 \cdot 10^{-5}$
6	14	$7.5 \cdot 10^{-3}$	$3 \cdot 10^{-3}$				
8	12	$5 \cdot 10^{-4}$	$2 \cdot 10^{-4}$				

Table 3. Maximal absolute error $\Delta T_{\max}$ [°C] and average absolute error ΔT_{avr} [°C] of temperature measurement after linearization for T_{ip} = 50°C.

Inflection point at T_{ip} = 50°C							
Dual-stage dual-flash PWL ADC				**Dual-stage single-flash PWL ADC**			
N_1	N_2	$\Delta T_{\max}$ [°C]	ΔT_{avr} [°C]	N	N	$\Delta T_{\max}$ [°C]	ΔT_{avr} [°C]
4	8	$1.427 \cdot 10^{-1}$	$4.1 \cdot 10^{-2}$	6	6	$2.16 \cdot 10^{-2}$	$6.6 \cdot 10^{-3}$
4	12	$1.35 \cdot 10^{-1}$	$4.07 \cdot 10^{-2}$	8	8	$1.3 \cdot 10^{-3}$	$4 \cdot 10^{-4}$
6	10	$9.3 \cdot 10^{-3}$	$2.6 \cdot 10^{-3}$				
4	16	$1.35 \cdot 10^{-1}$	$4.07 \cdot 10^{-2}$	10	10	$7.4747 \cdot 10^{-5}$	$2.5497 \cdot 10^{-5}$
6	14	$8.8 \cdot 10^{-3}$	$2.6 \cdot 10^{-3}$				
8	12	$6 \cdot 10^{-4}$	$2 \cdot 10^{-4}$				

Table 4. Maximal absolute error $\Delta T_{\max}$ [°C] and average absolute error ΔT_{avr} [°C] of temperature measurement after linearization for T_{ip} = 75°C.

Inflection point at T_{ip} = 75°C							
Dual-stage dual-flash PWL ADC				**Dual-stage single-flash PWL ADC**			
N_1	N_2	$\Delta T_{\max}$ [°C]	ΔT_{avr} [°C]	N	N	$\Delta T_{\max}$ [°C]	ΔT_{avr} [°C]
4	8	$1.765 \cdot 10^{-1}$	$4.69 \cdot 10^{-2}$	6	6	$2.2 \cdot 10^{-2}$	$6.9 \cdot 10^{-3}$
4	12	$1.579 \cdot 10^{-1}$	$4.64 \cdot 10^{-2}$	8	8	$1.3 \cdot 10^{-3}$	$4 \cdot 10^{-4}$
6	10	$1.04 \cdot 10^{-2}$	$2.9 \cdot 10^{-3}$				
4	16	$1.580 \cdot 10^{-1}$	$4.64 \cdot 10^{-2}$	10	10	$7.7153 \cdot 10^{-5}$	$2.6043 \cdot 10^{-5}$
6	14	$1.01 \cdot 10^{-2}$	$2.9 \cdot 10^{-3}$				
8	12	$7 \cdot 10^{-4}$	$2 \cdot 10^{-4}$				

The simulations were conducted for three inflection points 25°C, 50°C and 75°C, and for ADC resolutions of 12, 16, and 20 bits. For example, for the inflection point at 50°C (see Table 3), and the total resolution of 20 bits, the maximal absolute error for DSSF PWL ADC is $7.4747 \cdot 10^{-5}$°C which is almost 8 times lower in comparison with $6 \cdot 10^{-4}$°C which is the maximal absolute error obtained for the case when $N_1 = 8$ bits and $N_2 = 12$ bits. The ratio between the errors goes up to 1800 when the 20-bit DSSF PWL ADC is compared to the DSDF PWL ADC with $N_1 = 4$ bits and $N_2 = 16$ bits. The measurement accuracy of 0.5°C, given in the datasheet of the particular thermistor [3], can be improved by $6.7 \cdot 10^3$ times by using the proposed 20-bit linearizing ADC. From Tables 2 to 4, it can be observed that the average measurement error is approximately 3 times lower in comparison with the maximal absolute error, for all considered cases. Additionally, the percentage nonlinearity error NE [%] of the ADC digital output has the same numerical value as the maximal absolute error $\Delta T_{\max}$ according to (8), since the temperature range (full span) is 100°C.

If the results from Tables 2 to 4 are mutually compared, *i.e.* if the results related to three inflection points are mutually compared for the same resolutions, one can notice that errors $\Delta T_{\max}$ and ΔT_{avr} are not significantly different. What is important, when a specific inflection point is used, is that the measurement error near the inflection point is significantly smaller compared to the rest of the measurement range. This can be observed from Fig. 7, where the diagrams of the measurement error for three inflection points and DSDF PWL ADC with $N_1 = 8$ bits and $N_2 = 12$ bits, are given.

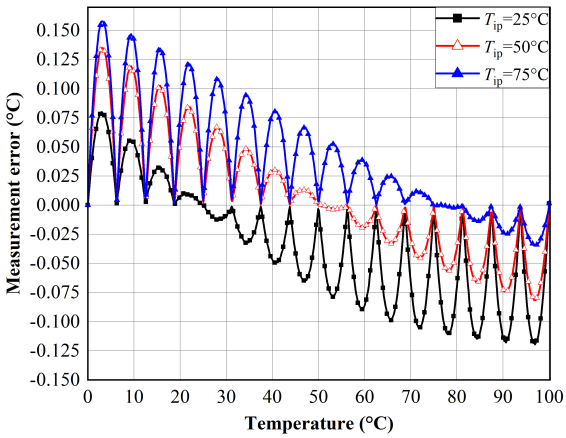

Fig. 7. Measurement error for three inflection points and a DSDF PWL ADC with $N_1 = 8$ bits and $N_2 = 12$ bits.

Since the linearization is performed in the first stage of conversion, its resolution has the greatest impact on nonlinearity compensation. However, the second stage of conversion reduces quantization noise generated during the first stage of conversion. When both stages have the same resolution, as is the case with the proposed ADC, the nonlinearity compensation is more effective when compared to the case when the first stage has a lower resolution, as in the DSDF PWL ADC. However, the residual error still persists because of the high quantization error. In other words, the resolution of the second conversion stage needs to be higher than that of the first stage in order to eliminate the quantization error from the first conversion stage. For this reason, the DSDF PWL ADC has a significantly lower quantization noise level contained in the overall measurement error, but the effect of the nonlinearity compensation is not as good as with the

DSSF PWL ADC of the same total resolution. The previous statements can be easily proved by comparing results from Fig. 7 with those from Figs. 8 to 10. It is easily observed from Figs. 8 to 10 that the measurement error is smaller around the inflection point, even in the presence of high levels of quantization noise. Additionally, the transfer function of the first stage of the DSSF PWL ADC is not the best PWL approximation, *i.e.* the approximation error is not minimized and this error is also contained in the residual measurement error after linearization.

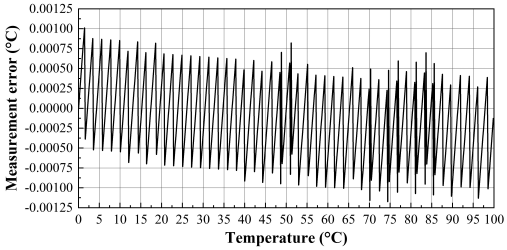

Fig. 8. Measurement error for $T_{ip} = 25°\text{C}$, $N = 8$ bits.

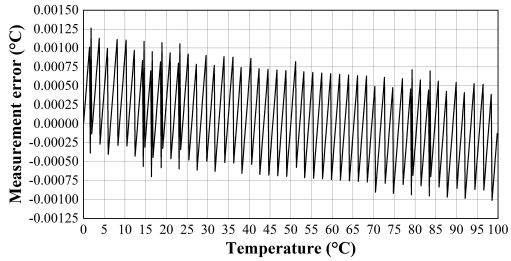

Fig. 9. Measurement error for $T_{ip} = 50°\text{C}$, $N = 8$ bits.

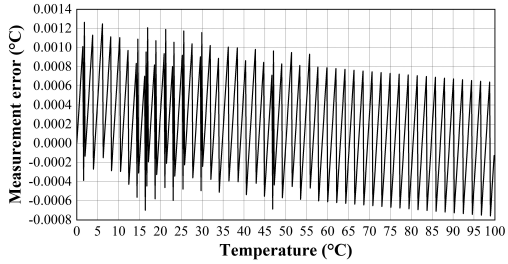

Fig. 10. Measurement error for $T_{ip} = 75°\text{C}$, $N = 8$ bits.

Another very important advantage of the proposed design is its compactness and energy efficiency due to the significantly lower number of employed comparators. The comparison between two discussed designs in terms of the number of comparators employed is given in Table 5. For example, for the 10-bit flash ADC of the proposed design, *i.e.* for the 20-bit DSSF PWL ADC, total comparator count equals to 257, while for the same overall resolution and a DSDF PWL ADC with $N_1 = 4$ bits and $N_2 = 16$ bits, the comparator count equals to 65550, which

Table 5. Comparator count comparison between DSDF and DSSF PWL ADCs of the same total resolution.

Comparator count						**Comparator count ratio**
Dual-stage dual-flash PWL ADC			**Dual-stage single-flash PWL ADC**			
N_1	N_2	$2^{N1} - 1 + 2^{N2} - 1$	N	N	$2^{(N-2)} + 1$	
4	8	15 + 255 = 270	6	6	17	15.88
4	12	15 + 4095 = 4110	8	8	65	63.23
6	10	63 + 1023 = 1086				16.71
4	16	15 + 65535 = 65550	10	10	257	255.06
6	14	63 + 16383 = 16446				64
8	12	255 + 4095 = 4350				16.93

is 255 times more. The obtained numbers show that the proposed design compensates the well-known disadvantages of flash ADCs, such as high design complexity and power consumption, while short conversion cycle due to parallelism of design is kept.

4. Conclusions and summary

In this paper, linearization of an NTC thermistor is performed using a Wheatstone bridge and a dual-stage piecewise-linear ADC of a newly-proposed design. The output of the Wheatstone bridge is quasi-linear *S*-shaped voltage which is further linearized with the ADC of the proposed design. The proposed ADC has been named the dual-stage single-flash PWL ADC since both conversion stages are performed by the same flash ADC. In addition, the design of the employed flash ADC has been made more compact and cost-effective by reducing the number of employed comparators. The proposed ADC has been used for the Vishay NTCLE413E2103F520L thermistor linearization in the range from 0°C to 100°C, and with the resolution of 20 bits (a 10-bit flash ADC of compact design is used) the maximal absolute error of $7.0795 \cdot 10^{-5}$°C has been obtained. In addition to performing two signal processing functions simultaneously, *i.e.* linearization and A/D conversion, the proposed ADC is compact, cost-effective and with lower power consumption in comparison with a dual-stage dual-flash PWL ADC of the conventional design and the same total resolution. The proposed linearization method can be performed without any kind of processing power or memory, but still achieves high quality results in sensor nonlinearity compensation. The aforementioned advantages of the proposed linearizing ADC can result in its wider application in linearization of different types of sensors, such as resistive displacement sensors, magneto-resistive sensor bridges, optical rotary encoders, humidity sensors, *etc.*

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