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A control method of fault current in MT-HVDC grid based on current limiter and circuit breaker

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Abstract: In order to realize selective isolation of fault lines in multi-terminal high voltage DC (MT-HVDC) grids, it is necessary to ensure that the sound lines can still transmit power normally after the grounding fault occurs in a DC power network. If the fault line needs to be cut before the converter is blocked, a DC circuit breaker (DCCB) with large switching capacity is often required. At present, the extreme fault over-current and the high cost of DCCBs have become the prominent contradiction in MT-HVDC projects. Reducing the breaking stress of power electronic devices of the circuit breaker and controlling its cutting-off time are the major difficulties in this research field. In this paper, a topology of a hybrid DCCB with an inductive current limiting device is proposed. By analyzing its working principle, the calculation method of key parameters is given, and a four-terminal HVDC grid is built in a PSCAD/EMTDC platform for fault simulation. The results show that compared with the traditional circuit breaker, this topology can effectively limit the rising speed and maximum current of fault current when the system fails, and quickly remove the fault line, so as to meet the suppression requirement of the HVDC system for fault current.

Key words: bipolar short circuit, fault current limiting, hybrid DC circuit breaker, ulti-terminal HVDC grid

1. Introduction

With the development of large-scale access of distributed renewable energy, the construction of a new urban distribution network, island power supply and remote area power supply, the difficulty of large-scale collection and delivery of renewable energy needs to be solved urgently. Presently,

the high voltage DC (HVDC) power grid is a research hotspot in the field of power electronics technology, which provides a solid backing for the increasing DC load and the improvement of energy storage technology. The HVDC system based on a voltage source converter (VSC) has become the main trend of DC power grid development due to its advantages of faster power decoupling control, less risk of commutation failure and no need of large capacity reactive power compensation devices. In 2003, German professor R. Marquardt proposed a topological structure based on a modular multilevel converter (MMC) [1]. By virtue of its advantages of good expansibility, low harmonic content and low loss, an MMC has become the first choice of converter station topology for a new generation of HVDC transmission systems.

Flexible DC transmission technology is changing to different topological structures. Since China has a vast territory, new energy bases and load centers are far apart, reasonable allocation of resources and asynchronous networking of multiple AC systems are the major requirements for building a strong smart grid. In 2020, the newly-built Zhangbei ±500 kV/3000 MW four-terminal flexible DC power grid demonstration project has been officially put into operation, which is also the first DC power grid project in the world to realize a wind power interconnection.

An MT-HVDC power grid is a low-inertia system. Once a short circuit fault occurs on the DC side, the initial fault current will rise to the order of several kA in a few milliseconds, threatening the stable operation of the whole system [2]. The fast and effective isolation of DC fault requires an accurate calculation method of fault transient current analysis and an effective over-current suppression strategy. Some achievements have been made in the fault current suppression technology of MTDC power grids.

In references [3] and [4], a "double thyristor" structure is proposed at the outlet of the converter submodule to force the fault current fed by the converter station to decay freely after the converter station is locked, and a damping module is added to accelerate the decay speed of the fault current; In reference [5], a fault current suppression scheme is proposed, in which an inductive fault current limiter is connected in series with a circuit breaker at both ends of a DC line, and the theoretical calculation method of the current limiting inductance is given; In references [6] and [7], it is proposed to install a superconducting current limiter in a multi-terminal HVDC transmission system, which has achieved a good fault current suppression effect; In reference [8], a fault handling strategy based on the coordination of a resistive superconducting current limiter and hybrid DC circuit breaker is proposed; In reference [9], considering both the maximum breaking current requirement of a CB and the cost of a fault current limiter, the optimal configuration of a capacitive fault current limiter is achieved by using a genetic algorithm; In reference [10], a particle swarm optimization (PSO) algorithm is improved, and the improved algorithm is used to optimize the configuration of a UHV fault current limiter; In reference [11], the global optimal configuration of a current limiting reactor is realized by setting constraints and adopting a "teaching and learning" optimization algorithm.

To sum up, the advantages of references [3] and [4] are that the attenuation speed of fault current is accelerated, and the harm of fault current to the system can be effectively reduced, but the cost is high and the suppression process is complex; In reference [5], this topology can reduce the effectiveness of energy absorption of arresters, thus reducing the difficulty of making arresters, but it can not effectively suppress the fault current; Although the superconducting current limiters mentioned in references [6] and [7] can suppress the fault current to a certain extent, they are not widely used; The application of the technology mentioned in reference [8] in

the actual high voltage flexible direct power grid is still in the research and development stage, and the cost and reliability need to be considered; The main contribution of references [9, 10] and [11] is to improve the optimization algorithm, but the accuracy and application environment of its mathematical model are very limited.

Based on this, this paper proposes a fault current control and protection strategy based on the combination of a fault current limiter and a high voltage DC circuit breaker, so that the flexible DC power grid can quickly isolate faults in the case of a short circuit. This paper first analyzes the fault current after the fault occurs, and introduces the principle of DC power grid fault protection. On this basis, a new circuit breaker topology is proposed, and its parameter design is deduced through theoretical calculation. Finally, the feasibility of this scheme is verified by simulation. Compared with other fault current control methods, this topology has the advantage of low cost, only adding a fault current limiter can achieve the purpose of greatly suppressing the fault current, and the suppression process is simple. Secondly, compared with the superconducting current limiter, this control method is more suitable for large-scale promotion and application. To sum up, the fault current limiting control strategy proposed in this paper reduces the manufacturing cost of DC circuit breakers, improves the engineering feasibility, and limits the rising rate of fault current to a great extent, so as to increase the fault detection redundancy time, reduce the probability of protection malfunctions, and improve the safety and reliability of the system. In a PSCAD/EMTDC simulation platform, the proposed scheme is configured in the four-terminal DC power grid model to verify its effectiveness.

2. Fault status analysis on DC lines

2.1. Introduction to MMC-HVDC transmission system

Compared with VSC-based DC transmission systems, an HVDC grid based on a MMC has higher transmission flexibility and power supply reliability. But it also requires a DCCB to isolate and remove faults, and extremely stringent requirements for relay protection. A four-terminal HVDC grid is shown in Fig. 1. There are a total of four converter stations in a bipolar half-bridge MMC structure in the system, which is connected by four DC transmission lines $L_{1(2,3,4)}$ to form a DC network. The positive and negative poles of the line are shown in the form of a single line diagram. The converter stations all adopt the half-bridge MMC topology, among which MMC1 and MMC4 are the rectifier stations, MMC2 and MMC3 are the inverters. R_1~R_8 represent the voltage and current measuring points at the end of the line, and hey are also the installation places for line protection and a DCCB. Both sides of the circuit are equipped with hybrid HVDC circuit breakers CB1~CB8 and flat wave reactors L_{S1}~L_{S8}.

When a short circuit fault occurs, the fault current cannot be blocked by blocking an insulated gate bipolar transistor (IGBT) because there are anti-parallel diodes in a submodule (SM). If only the circuit breaker on the AC side is broken after about 100 ms, the fault current will rise rapidly for the low-damping DC transmission network. After the converter station is locked up, the AC system will feed current to the fault point through the reverse parallel diode, which will continuously feed a huge fault current to the fault point. In addition, the reinvestment of the converter station requires the SM capacitor pre-charging and other operations, which may be not conducive to the quick recovery of transient faults. Therefore, it is necessary to set up line

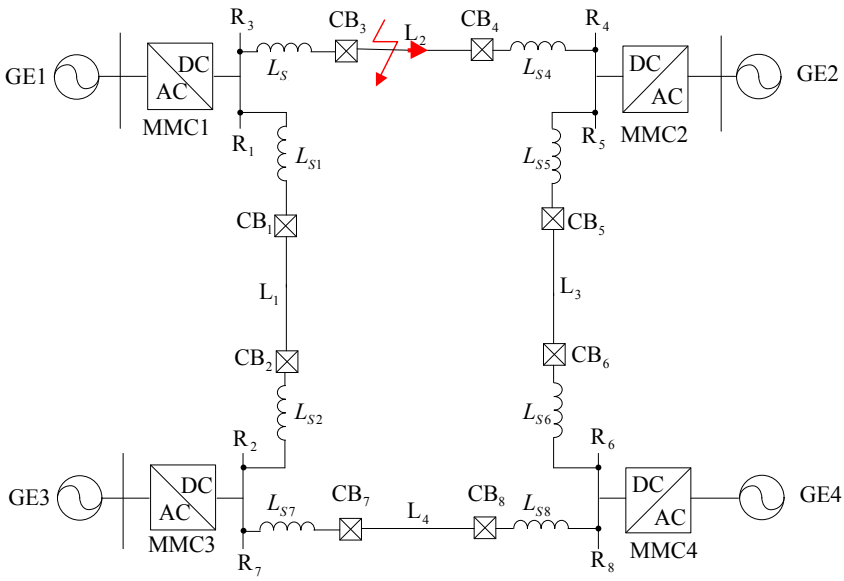


Fig. 1. Topology of four-terminal HVDC power grid

protection to monitor the occurrence of faults before the converter station is locked, so as to limit the rise of fault current.

2.2. Current analysis of bipolar short circuit fault on DC side based on MMC

There are three types of transmission line faults in a MTDC power grid: a disconnection fault, single pole grounding fault and double pole short circuit fault. A disconnection fault refers to a type of fault in which the DC transmission line is disconnected by external factors. When the system has a disconnection fault, the power transmission at both ends is interrupted. If the system is working in rectification mode, the DC voltage will gradually oscillate and rise, and the valve equipment severe overvoltage will occur, and the converter station must be locked immediately to ensure system safety. From the perspective of the impact on the system, the bipolar short circuit fault is the most serious [12]. In this paper, the detection and location of DC fault will be analyzed by taking the bipolar short circuit fault as an example. In the bipolar short circuit fault current path shown in Fig. 2, each MMC bridge arm contains N sub-modules and series reactor L_0, each phase unit contains two upper and lower bridge arms, and each SM contains two IGBTs, VD1, VD2, two antiparallel diodes and an energy-storage capacitor, C_0.

At the initial stage of the short circuit fault, the DC voltage drops rapidly. At this point, the fault current on the line is mainly composed of the capacitor discharge of the SM and the AC side power supply feed [13], as is illustrated in Fig. 2. Since the vector sum of the AC short-circuit current at the top and bottom of the valve is zero, the discharge current of the capacitance of the SM is only considered when the current is calculated.

On the DC side, the discharge process can be equivalent to the second-order circuit shown in Fig. 3. L_{eq}, R_{eq}, C_{eq}, respectively, represent the equivalent inductance, resistance and capacitance

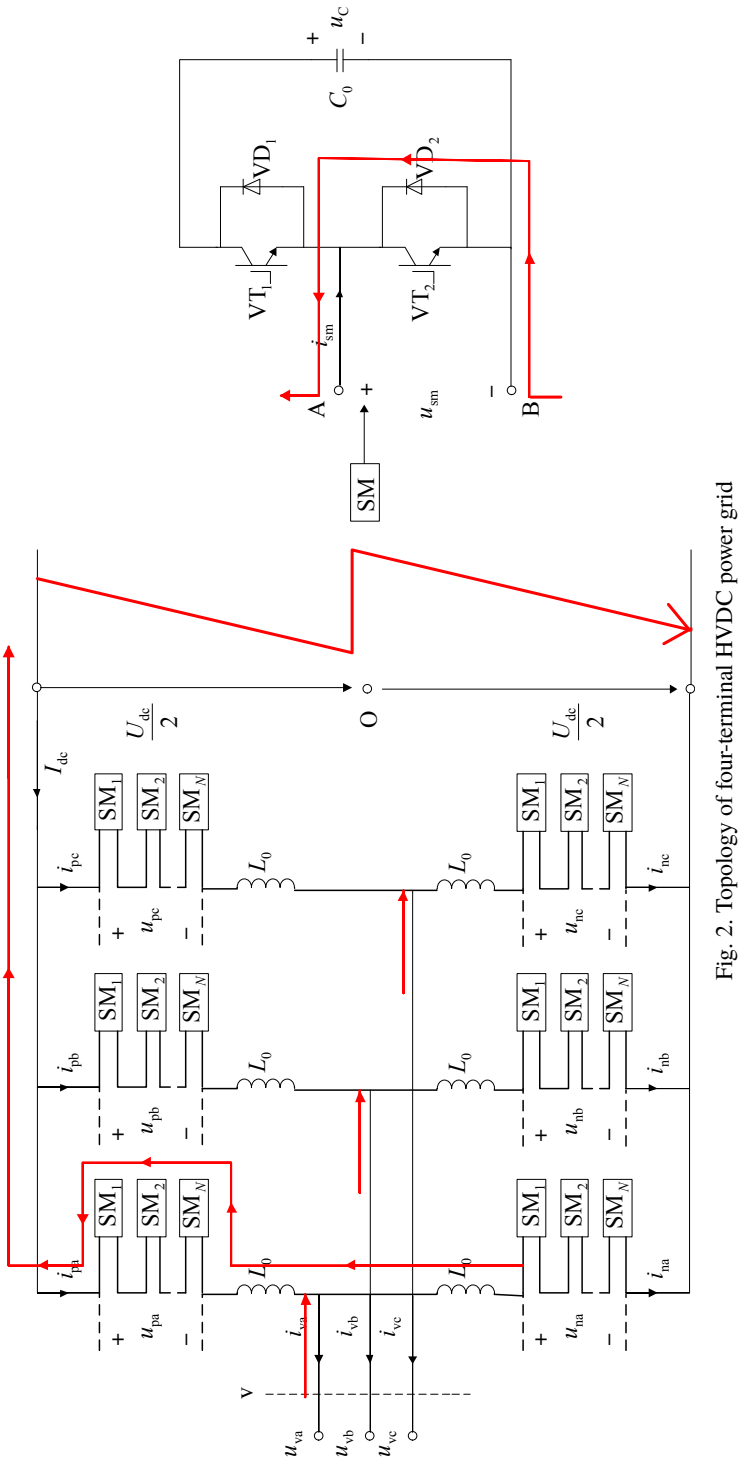


Fig. 2. Topology of four-terminal HVDC power grid

of the converter station. Since the small capacitance of the overhead line is negligible, r_l and l_l are used to represent the resistance and inductance of the line per unit length respectively, and x is the distance from the fault point to the converter station.

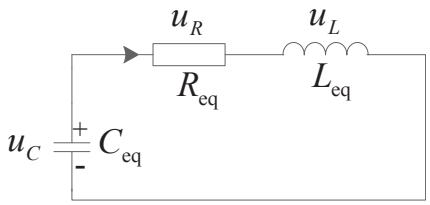


Fig. 3. Equivalent second-order circuit of converter

According to the analysis,

$$\begin{cases} C_{eq} = \dfrac{6C}{N} \\ L_{eq} = \dfrac{2}{3}L_{s1} + 2L_{s2} + 2xl_0 \\ R_{eq} = \dfrac{2}{3}R_1 + 2xr_0 + R_f \end{cases}, \tag{1}$$

where: L_{s1} and L_{s2} are the bridge arm reactor and the smoothing reactor, respectively; R_1 and R_f are the bridge arm resistance and the fault loop transition resistance; N represents the number of SMs put into each bridge arm at the same time.

The transient process of this stage can be represented by Eq. (2):

$$L_{eq}C_{eq}\frac{d^2u_c}{dt^2} + R_{eq}C_{eq}\frac{du_c}{dt} + u_c = 0. \tag{2}$$

It can be seen from the above equation that the discharge of the SM is in a second-order under-damped oscillation process, and the fault current on the DC side will decay exponentially. Therefore, it is necessary to set a current limiter to accelerate the current attenuation speed.

3. Protection strategy and current limiting control on DC side

3.1. Principle of DC grid fault protection

Each protected area of the flexible DC grid is not completely independent, and proper coordination is required. Meanwhile, there should be no dead zone between the protected areas to provide complete protection for all operating equipment [14]. The conventional flexible HVDC system is focused mainly on the rapidity and sensitivity of fault detection and fault identification, the MTDC system also takes into account the recognition of fault lines, and due to the complexity of faults in the flexible DC power grid, higher requirements are put forward for the rapidity, sensitivity and selectivity of fault detection and recognition. The configuration principle of flexible DC grid protection is shown in Fig. 4.

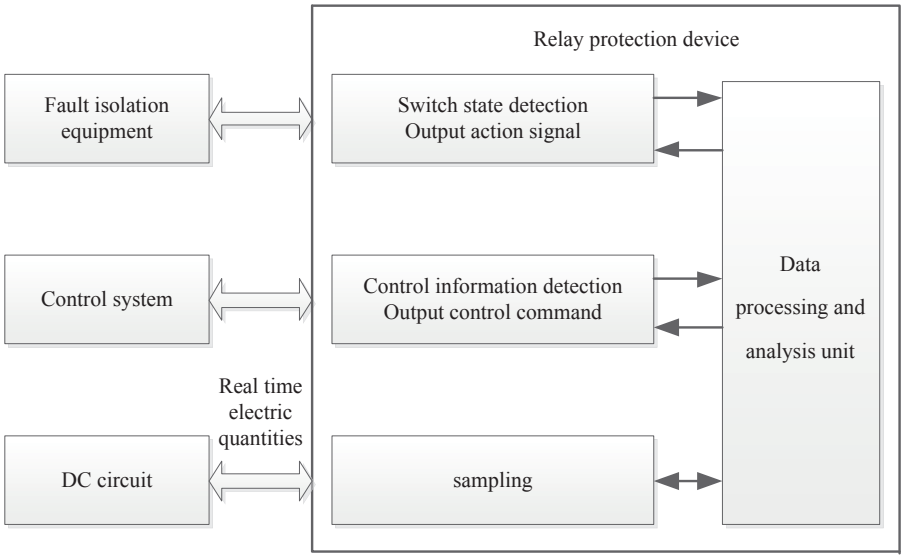


Fig. 4. Principle of flexible DC grid protection configuration

Presently, DC line fault detection and identification methods mainly include:

1. Fault detection based on a single terminal: fault identification and location are carried out by detecting the amplitude change or incremental change rate of voltage/current on the DC line, with fast action speed, generally used as the main protection of the line.
2. Communication-based pilot protection: the current differential protection needs to use the communication channel to detect the difference flow at both ends of the line for fault discrimination, but a lot of data transmission processing will affect the speed of the protection action [15]. The directional pilot protection can be used as the backup protection of the line by identifying the current direction at both ends of the component and relying on the communication system.
3. Traveling wave protection: the high-frequency characteristics of transient traveling waves, such as amplitude, polarity, duration, are extracted and analyzed by a corresponding mathematical method to detect and locate the fault. However, with the attenuation of electrical quantity, the sensitivity of protection becomes worse.

3.2. Fault current control strategy based on current limiter and circuit breaker

3.2.1. Design of a new DCCB topology

Hybrid DC circuit breakers are mainly composed of three parts: the main breaker (MB), a load commutation switch (LCS), and ultra-fast switch (UFD). When running in a steady state, the MB is turned off, an LCS and UFD are closed, and DC current flows through normal flow components. When the DC line fails, the LCS is first applied with a turn-off signal, and the current is transferred to the fault current breaking component. Secondly, the UFD is disconnected, and after 2 ms of interruption delay, the turn off signal is applied to the MB. At the moment of MB disconnection,

the arresters of each section are connected to the fault line, and the current oscillation through the fault line is attenuated to zero [16, 17]. The circuit breaker topology is shown in Fig. 5.

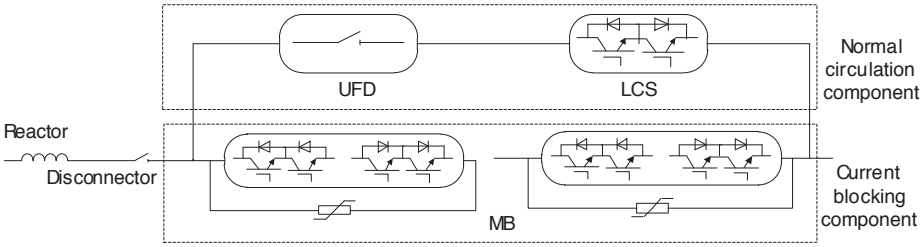


Fig. 5. Topology of hybrid DCCB

DCCBs with large switching capacity are necessary to ensure reliable operation under various extreme fault overflows. Extreme fault over-current and high cost of DCCBs have become a prominent contradiction in MT-HVDC systems [18]. The solution to this contradiction is to set a certain current-limiting device on the line, control the short-circuit current at a low level, and then remove the fault by the DCCB. However, the principle of the DC line fault protection proposed above is mostly based on the value or rate of change of different electric capacity of the line as the criterion. If the current limiter is not configured properly, the protection characteristic quantity will be destroyed, leading to failure identification, thus extending the protection time and damaging the safe operation of the system.

To solve above problems, a novel fault current control method based on the current-limiting device and DCCB is proposed in this chapter. The topology, the new type of hybrid DCCB with inductive current-limiting circuit is shown in Fig. 6. The inductive current-limiting device L-BTA is composed of current-limiting inductance and energy dissipation branches. The energy dissipation branch consists of a controllable bidirectional thyristor, T_r, and an energy absorption resistance, R_r.

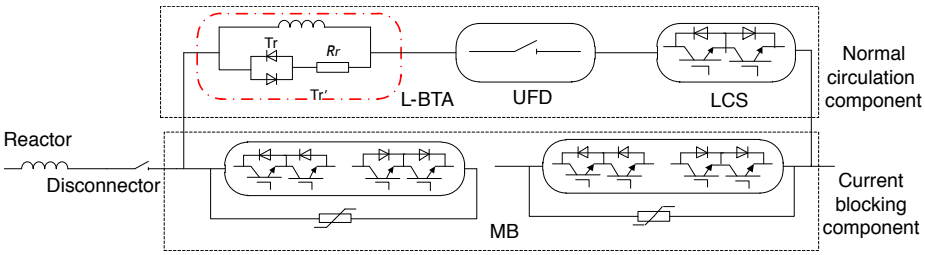


Fig. 6. Topology of DCCB with inductive current limiting circuit

Different working stages of the DCCB with the above topology circuit breaker are analyzed as follows:

1. Fault detection stage: the grid current flows through the main branch, and the fault current shows a monotonously increasing trend. Since the number of mechanical switches is small and its conduction loss is insignificant, the on-state loss is small [19]. The circuit breaker

can be tantamount to an inductor, the value of which depends on its switching capacity and the current change rate it can withstand.

2. Current transfer stage: when the main switch of the circuit breaker is turn on, T_r and T_r' trigger the conduction. Due to the addition of a current-limiting device to the circuit, the fault current decreases first and then increases. The values of inductance and resistance in the current-limiting device need to make sure that the fault current cannot exceed the cut-off capacity of the circuit breaker.
3. Energy absorption stage: energy absorption resistance and the metal oxide arrester (MOA) in energy absorption branches jointly release energy of fault current, and the fault current shows a monotonously decreasing trend.

When L-BTA cooperates with a DC circuit breaker to cut off fault current, the current flow path after DC circuit breaker acts as shown in Fig. 7.

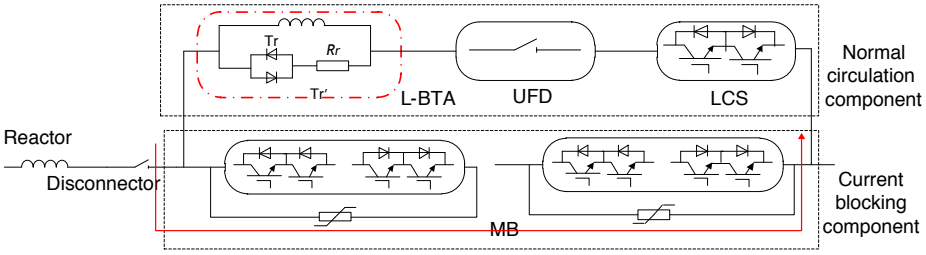


Fig. 7. The current flow path after DC circuit breaker act

3.2.2. Parameters design of new circuit breaker

Circuit breaker parameters are determined by the DC side fault current. When researching the DC side line current of the converter station, the AC side can be regarded as a DC power source under normal operation of the converter station. In the case of fault, only the fault current of the capacitor discharge stage should be analyzed without considering the AC side [20]. The fault current comes to its peak value in the capacitor discharge stage, while the circuit breaker generally acts before the peak value of the current. Therefore, this paper only examines the fault current in the capacitor discharge stage.

After adding the current-limiting device, the fault current rises slowly, and the capacitor voltage does not drop much within 2 ms after fault detection. Therefore, the DC voltage source can be used to approximately replace the capacitor for calculation, and the simplified fault current is shown in Eq. (3):

$$I_{dc}(t) = \frac{U_{dc}}{R_L} - \frac{U_{dc} - I_{dN}R_L}{R_L} e^{-\frac{R_L}{L'}(t-t_0)}, \tag{3}$$

where: U_{dc}, I_{dN} are the nominal voltage and nominal current on the DC side, respectively; R_L is the line resistance; L' is the sum of current-limiting inductance L_s and the line inductance.

Due to parameter requirements of DCCBs: the maximum fault current shall not exceed the circuit breaker's breaking current. The fault current rise rate shall not exceed the maximum current change rate that the circuit breaker can withstand. According to the parameters of ABB DCCBs [21], the constraint conditions can be obtained:

$$I_{dc}(t_1) < 9 \text{ kA}, \tag{4}$$

$$\frac{\mathrm{d}I_{\mathrm{dc}}}{\mathrm{d}t} < 3.5 \text{ kA/ms}, \tag{5}$$

$$t_1 = t_0 + t_{\mathrm{f}}, \tag{6}$$

where t_{f} is the fault detection time.

Similarly, during the current transfer stage (starting from time t_1), the line current is

$$I_{\mathrm{dc}}(t) = \\ = \frac{I(t_1)R_{\mathrm{r}}L_{\mathrm{r}}^2 + I(t_1)R_{\mathrm{r}}L_{\mathrm{S}}L_{\mathrm{r}} + U_C(t_1)L_{\mathrm{r}}^2}{\dfrac{R_{\mathrm{r}}\,(L_{\mathrm{S}}+L_{\mathrm{r}})^2 + U_C(t_1)L_{\mathrm{r}}^2(t-t_1)}{L_{\mathrm{S}}+L_{\mathrm{r}}} + L_{\mathrm{r}}\dfrac{I(t_1)L_{\mathrm{S}}L_{\mathrm{r}} - L_{\mathrm{r}}U_C(t_1) + I(t_1)L_{\mathrm{r}}R}{R_{\mathrm{r}}\,(L_{\mathrm{S}}+L_{\mathrm{r}})^2}e^{\frac{R_{\mathrm{r}}(L_{\mathrm{S}}+L_{\mathrm{r}})}{L_{\mathrm{S}}+L_{\mathrm{r}}}(t-t_1)}}. \tag{7}$$

Considering the circuit breaker capacity and the time when the current reaches the minimum, the constraint conditions of the current transfer stage are shown below:

$$I_{\mathrm{dc}}(t_2) < 9 \text{ kA}, \tag{8}$$

$$\frac{\mathrm{d}I'_{\mathrm{dc}}}{\mathrm{d}t} < 3.5 \text{ kA/ms}, \tag{9}$$

$$t_{\min} < t_1, \tag{10}$$

where $t_{\min}$ is the moment when the current reaches its minimum value.

At the same $t_{\min}$, there are many different combinations of the values of resistance R_{r} and inductor L_{r}. Therefore, the design of parameters is flexible, and the parameters can be chosen according to the actual situation.

When designing parameters of current-limiting devices, R_{r}, $t_{\min}$ are firstly determined, and then L_{r} is calculated. Observe the peak current $I_{(t2)}$ at t_2, if it is much larger than the breaking capacity or much smaller than the peak current $I_{(t1)}$ at t_1, adjusted the value of R_{r}, $t_{\min}$ according to the situation. If it is a little bigger or less than $I_{(t1)}$, L_{r} can be adjusted.

4. Simulation and analysis

4.1. Fault current control strategy based on current limiter and circuit breaker

In order to verify the working effect of the proposed L-BTA current-limiting DCCB, a simulation model of a four-terminal HVDC power grid was built on a PSCAD/EMTDC simulation platform. The topology, connection mode, circuit breaker configuration and fault location are shown in Fig. 1. Converter stations 1, 3 and 4 adopt constant active power control and constant reactive power control, while converter station 2 adopts constant DC voltage and constant reactive power control [22]. Considering that the DC reactor used in the project is generally 150 mH, and the limiting current demand of a 500 kV DC power grid [23], 200 mH is selected in this paper. The SM capacitor voltage balance control method used in the simulation is the MMC capacitor voltage balance method based on the load regulation of the energy harvesting power supply [24]. In this method, a low-voltage additional circuit is paralleled to the output side of the energy harvesting power supply to make the power load adjustable. The additional circuit is composed of

a resistor and MOSFET (metal oxide semiconductor field effect transformer) in series. An external control signal with fixed frequency is used to control the MOSFET, which can adjust the input current and load power of the power supply and indirectly change the capacitor voltage system of the MMC submodule. Basic parameters are presented in Table 1; DC circuit breaker parameter settings are shown in Table 2.

Table 1. Parameters of four-terminal HVDC grid

System parameters		**Value**	**Unit**
Line length	L_{12}	208	km
	L_{23}	180	km
	L_{34}	205	km
	L_{41}	50	km
Active power of converter station	Station 1	800	MW
	Station 2	1000	MW
	Station 3	1200	MW
	Station 4	500	MW
DC line voltage		±500	kV
Number of SMs on bridge arm		100	/
SM capacitance		1000	μF
Smooth wave reactor		100	mH

Table 2. DC circuit breaker parameters

Branch	**Parameter**	**Value**
Main branch	Stray inductance of main branch L_{ZS1}/μH	1.7
	Fast mechanical switch stray inductance L_{ZS2}/μH	20.8
	Fast mechanical switch stray capacitance C_{ZS2}/pF	0.005×10^{-3}
	Fast mechanical switch parallel equivalent resistance R_0/Ω	550
	Fast mechanical switch parallel equivalent capacitance C_0/pF	500
Transfer branch	Capacitance C_{a1}/pF	23.3
	Diode parallel resistance R_{ZY1}/Ω	16
	Parallel resistance across the capacitor R_{ZY2}/MΩ	3
	RCD branch stray inductance L_{ZS3}/μH	2.1
	IGBT series loop stray inductance L_{ZS4}/μH	3

4.2. MOV value of DC circuit breaker

A metal oxide varistor (MOV) is paralleled on the DC circuit breaker port to absorb the great energy during the shutdown process. If the MOV value is larger, the over-voltage level between the circuit breaker ports and other locations of the DC power grid will be higher, and the external insulation requirements of the equipment will be higher, which will lead to the cost increase; If the MOV value is small, the over-voltage level is small, but the discharge current and energy consumption of the arrester are very high, the multi column arrester method is needed, and the cost will be increased, so a compromise configuration scheme must be adopted. This paper compares the rated voltage of a DC circuit breaker MOV with different values. The comparison data include DC pole line over-voltage, DC circuit breaker fracture over-voltage, arrester energy consumption, etc. The parameter configuration of the arrester is shown in Table 3, and the comparison calculation results of MOV rated voltage are shown in Table 4.

Table 3. Parameters of arrester

Equipment	**Name of arrester**	**Rated voltage/ kV**
Connecting transformer valve side	AV	592
Bridge arm reactor valve side	LV	592
DC bus	CBH	631
DC pole	DL	631
DC neutral bus	CBN1/CBN2	219

Table 4. Calculating comparison on various DC breaker MOV rated voltages

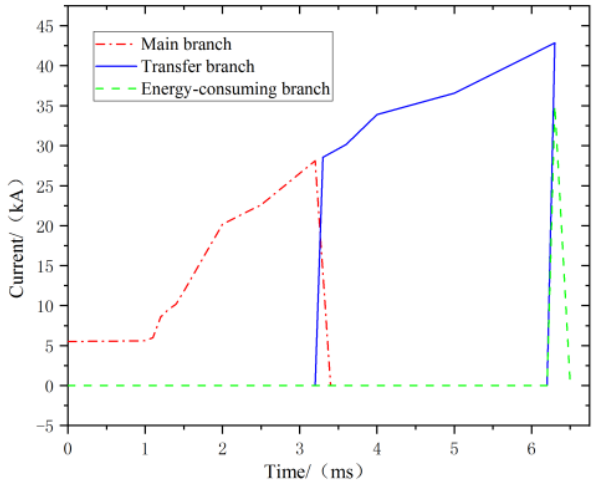
MOV rated voltage / kV	**DC circuit breaker break over-voltage / kV**	**MOV energy consumption (MJ)/ Recommended columns / kV**	**DC pole line over-voltage / kV**
520	777	6.9/4	910
535	800	6.6/4	915
550	820	6.2/4	918

After repeated comparison and calculation, the rated voltage of the DC circuit breaker MOV in this paper is 550 kV, which makes the DC circuit breaker break over-voltage basically at a level of 1.6 pu, and the reference value of the DC voltage is equal to 515 kV.

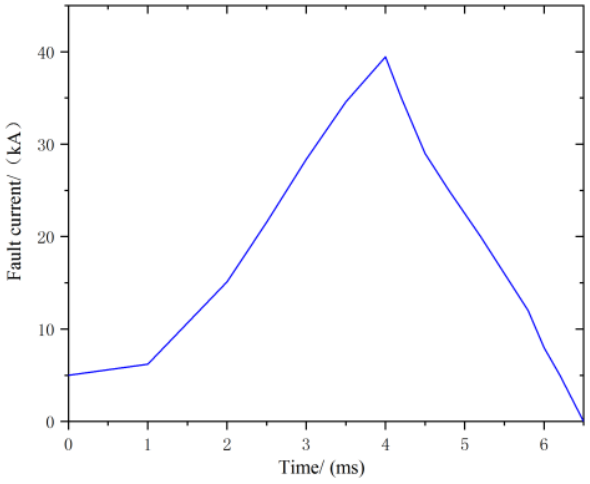
4.3. Current limiting performance analysis

The simulation of the system with an L-BTA current limiting device and without L-BTA current limiting device is carried out. A bipolar short circuit fault with a transition resistance of 50 Ω is set at 18 km away from MMC1 end on line L_2. In the single-ended DC equivalent

system, the fault occurrence time is set to 1.0 s. After 3 ms, the DC circuit breaker starts to operate, the main branch current drops to 0 instantaneously, and the fault current flows through the transfer branch; after another 3 ms, the transfer branch current drops. When it reaches 0, the current of the energy-consuming branch rises instantaneously, and drops to 0 after about 0.5 ms. The current is completely consumed, and the DC circuit breaker completes the breaking process. The current changes of each branch are shown in Fig. 8(a). The fault current on the MMC1 side is shown in Fig. 8(b). It can be seen that since 1.006 s, after the current in the DC circuit breaker is transferred to the energy-consuming branch, the line current begins to decrease and decreases to 0 at 1.0065 s. The power transmission is interrupted.



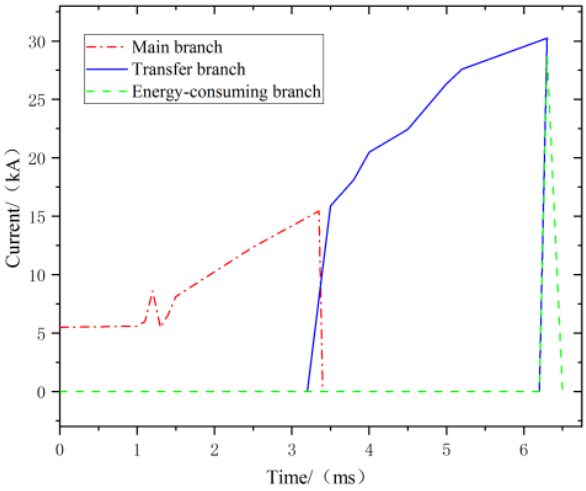
(a) Current of each branch of the circuit breaker



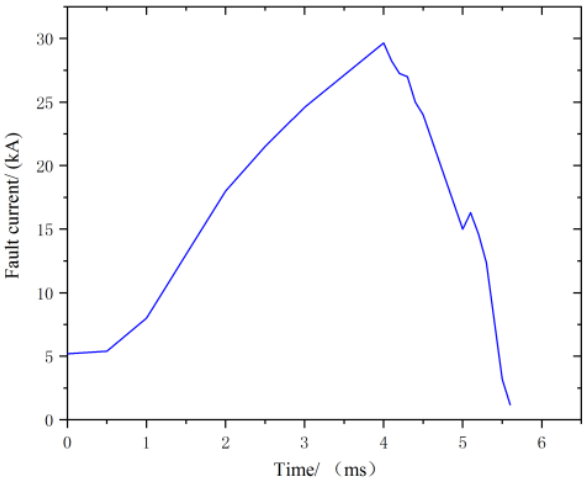
(b) Fault current on MMC1 side

Fig. 8. Current condition of DCCB without L-BTA

The change of system current after installing an L-BTA current limiting device on the HVDC circuit breaker is shown in Fig. 9. Compared with Fig. 9, the peak value of fault current is 39.863 kA before the current limiting device is installed, but after the current limiting device is installed, the peak value of fault current is 29.647 kA. The fault current is significantly reduced, and the current of the main branch and transfer branch of the circuit breaker is also significantly reduced, that is, the breaking current of the circuit breaker is reduced, and the manufacturing cost of the circuit breaker is reduced. In addition, after the installation of the current limiting device, the time for the fault current to be reduced to zero is greatly shortened, which optimizes the rapidity of line protection.



(a) Current of each branch of the circuit breaker



(b) Fault current on MMC1 side

Fig. 9. Current condition of DCCB with L-BTA

To sum up, the coordination strategy of the L-BTA current limiter, DCCB and overcurrent protection proposed in this paper can effectively limit fault current, avoid circuit interruption caused by blocking before switching the converter and circuit breaker, and improve the stability of the DC transmission system.

5. Conclusion

Due to the particularity of the flexible HVDC grid's own structure, its faults are characterized by large current peak and rapid fault development, which is easy to cause the damage of converter devices and threaten the safe and stable operation of the system [25]. This paper presents a topology of a high-voltage DCCB with an inductance current limiting device. The faulty process is divided into sections by an equivalent model, and the current limiting and cut-off processes are analyzed respectively. The current-limiting performance of this topology is verified by a four-terminal HVDC power network model. We can craw the following conclusions:

1. By using inductance and bidirectional controllable thyristors, the flexible switch between steady-state low reactance and transient high current limit reactance can be realized through the design of topology structure and control strategy. On the basis of the DCCB's basic function of breaking current, the function of limiting the development of fault current is realized.
2. It can be seen from the simulation results in the paper that the maximum fault current of the system without a current limiting device can be developed to more than 8 kA, while under the action of the current limiting device, the maximum is 5 kA, which reduces the manufacturing cost of the DCCB and improves the engineering feasibility. At the same time, the increasing rate of fault current is limited to a certain extent, so as to increase the redundancy time of fault detection, reduce the chance of false operation of protection, and improve the security and reliability of the system.
3. Equipment with power flow control or voltage conversion capability will become a key research direction in the future; an integrated gate commutated thyristor (IGCT) is expected to replace part of an IGBT to become the key power electronic device of new generation DC systems.

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