jet INTL JOURNAL OF ELECTRONICS AND TELECOMMUNICATIONS, 2021, VOL. 67, NO. 4, PP. 705-710
Manuscript received July 9, 2021; revised November, 2021 DOI:10.24425/ijet.2021.137866

Logarithmic ADC with Accumulation of Charge and Impulse Feedback – Analysis and Modeling

Zynoviy Mychuda, Lesya Mychuda, Uliana Antoniv, and Adam Szcześniak

***Abstract*—This article is a presentation of the analysis of new class of logarithmic analog-to-digital converter (LADC) with accumulation of charge and impulse feedback. Development of mathematical models of errors, quantitative assessment of these errors taking into account modern components and assessing the accuracy of logarithmic analog-to-digital converter (LADC) with accumulation of charge and impulse feedback were presented. (Logarithmic ADC with accumulation of charge and impulse feedback – analysis and modeling).**

***Keywords* —Analog-to-digital converter, analysis, construction, charge accumulation, logarithm, modeling, impulse feedback**

I. Introduction

ANALOG-to-digital converters (ADC) are the most important link in the modern digital systems used in the various areas of human activity, because they link these systems with real objects whose information from sensors is almost always (more than 90 %) given in analog form. The accuracy and speed of these systems depend in the first place on the characteristics and parameters used in ADC. From many ADC special attention is paid to ADC with logarithmic characteristic of conversion [1-20].

Logarithmic converters are indispensable for systems working in a wide range of input signals of 80 dB or more.

Use of logarithmic conversion provides for an effective solution to a number of important tasks, such as: compression of dynamic range of input signals, ensuring constant relative error of conversion, linearization of conversion characteristics and carrying out logarithmic arithmetic operation, in which multiplication, division or raising to a power is reduced to the basic operations of addition, subtraction, multiplication and division by constant factors. The last of these advantages is probably the most important, because it causes a significant increase in the speed of computerized systems, which is the most important for control systems of real-time such as control systems of manufacturing process and robot motion, telecommunications, aero navigations, cosmic and others in which delay in processing must be minimized.

This article was developed as part of the international cooperation concluded between the University of Technology in Kielce and the University of Technology in Lviv.

Zynoviy Mychuda, Lesya Mychuda and Uliana Antoniv are with Lviv Polytechnic National University, Department of the Computer-assisted Systems of Automation, Ukraine (e-mail: Zynovii.R.Mychuda@lpnu.ua, Lesia.Z.Mychuda@lpnu.ua, Uliana.S.Antoniv@lpnu.ua).

Adam Szcześniak is with University of Technology In Kielce, Department of Mechatronics and Machine Building, Poland (e-mail: a.szczesniak@tu.kielce.pl).

A. Objective and scope of work

The aim of this article is development of mathematical models of errors, quantitative assessment of these errors taking into account modern components and assessing the accuracy of logarithmic analog-to-digital converter (LADC) with accumulation of charge and impulse feedback.

II. Modeling Influence of Parasitic Capacitancies in the LADC with Charge Accumulation and Impulse Feedback

To facilitate modeling let us draw simplified functional diagram of LADC with charge accumulation and impulse feedback which is shown in fig. 1, where: U_{in} - input voltage, U_{Y0} to U_{Y2}– control voltage, SW0 to SW2 – analog switches, EC – output "End of conversion".

Since actual switches have different on and off times, then during work of LADC there may be cases when one of the switches for example SW0 still did not turn on and second SW1 had turned on. This will lead to the loss of the load on accumulative capacitor and reduction of accuracy. Duration time of these breaks should be long enough to allow switches to turn on or off. Thus in each step of conversion of LADC with charge accumulation and impulse feedback there will be two phases (F1-F2), and each of them will determine appearance of LADC model:

F1) discharging of accumulative capacitor which occurs when switches SW0, SW2 are turned on and switch SW1 is turned on;

F2) break: switches SW0, SW1 are turned off and switch SW2 is turned on.Taking into account a simplified functional diagram of LADC with charge accumulation and impulse feedback (fig.1), we can note that non-ideal components will be revealed by influence of interelectrode parasitic capacitances and leakage currents.

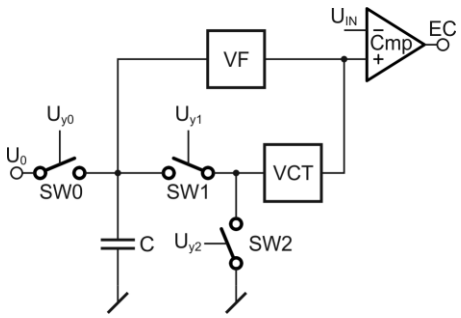

Figure 1. Simplified functional diagram of LADC with charge accumulation and impulse feedback

Influence of interelectrode parasitic capacitances comes down to the influence of parasitic capacitances of interelectrode analog switches, input capacitance of voltage follower and input capacitance of voltage-current converter VCT.

Taking into account construction and special work of LADC with accumulation of charge and impulse feedback (fig.1) we conclude:

1) interelectrode parasitic capacitances of analog switches cause sudden change of charge of accumulative capacitor;

2) In the discharge phase (during switch SW1 is turned on) control voltage is passed trough interelectrode capacitances gate-source (C_{GS1}) and gate-drain (C_{GD1}) of switch SW1 on the accumulative capacitor (C), and gate-drain (C_{GD1}) parasitic capacitance collects parasitic charge which value is proportional to sum of control voltage and voltage measured on the accumulative capacitor;

3) In pause phase (during switch SW1 turned off) parasitic charge, which is accumulated on capacity C_{GD1} when control voltage U_y acts , pass on accumulative capacitor C , changing voltage level on it.

So, the interelectrode parasitic capacitances in LADC with charge accumulation and impulse feedback cause following effects: immediate change of capacitance of accumulative capacitor; leakage of control voltage; passing parasitic charge.

Apart from parasitic capacitances errors of conversion of LADC with charge accumulation and impulse feedback cause leakage currents of components such as accumulative capacitor, analog switches (SW0 - SW2) and input current of voltage follower.

We will conduct analysis of influence of these all factors on work of LADC with charge accumulation and impulse feedback.

Based on functional diagram fig. 1 let us define model of LADC with charge accumulation and impulse feedback (fig. 2), which takes into account interelectrode parasitic capacitances of components. Numbers in indexes of parasitic capacitances gate-drain (C_{gd}) , gate-source (C_{gs}) and drain-source (C_{ds}) indicate number of the switch to which corresponding capacitance belong. Input capacitance of voltage follower is marked as C_{in} and output capacitance of VCT as C_{out}.

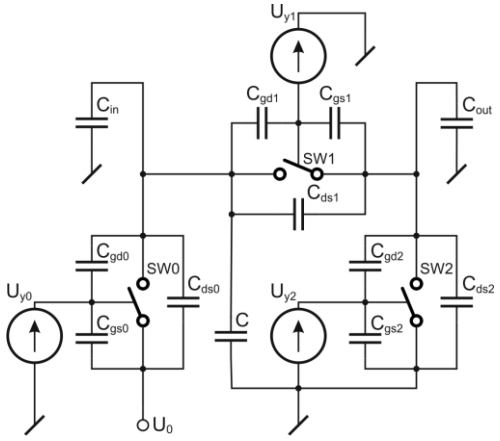

Figure 2. Model of LADC with charge accumulation and impulse feedback which takes into account interelectrode parasitic capacitances

Transmit coefficient of voltage follower VF does not depend on the value of capacitance leakage because there is no potential difference between input and output of VF, which is made on OA and its voltage transmit coefficient is equal to one.

A. Instantaneous change of accumulative capacitor.

Logarithm base ξ_{i0} in LADC with charge accumulation and impulse feedback depends on value of conversion coefficient of VCT, stability time of discharge when switch SW1 is turned on and capacity of accumulative capacitor. Taking into account connections of capacitances on the basis of equivalence theorem of electrostatic systems [13] under the assumption of equality of appropriate capacitances of switches, i.e.

$$C_{gs1} = C_{gs2} = C_{gs0} = C_{gs}$$

$$C_{gd1} = C_{gd2} = C_{gd0} = C_{gd}\,,\; C_{ds1} = C_{ds2} = C_{ds0} = C_{ds}$$

Formula for calculating basis of logarithm has form

$$\xi = \frac{1 - Y \cdot t / 2(C + 3C_{gd} + C_{gs} + 2C_{ds} + C_{in} + C_{out})}{1 + Y \cdot t / 2(C + 3C_{gd} + C_{gs} + 2C_{ds} + C_{in} + C_{out})} \qquad (1)$$

Substituting value of logarithm base in the formula for the description of characteristic of conversion of LADC we define error ($\Delta N_{i\delta}$) of output code from instantaneous change of capacitance of accumulative capacitor caused by interelectrode parasitic capacitances of components on i-th tact of conversion

$$\Delta N_{id} = \left(\frac{1}{\ln \xi} - \frac{1}{\ln \xi_{id}} \right) \cdot \ln \frac{U_{in}}{U_O}$$

Absolute error of voltage on accumulative capacitor from instantaneous change of capacitance of accumulative capacitor has value on N-tact of conversion

$$\Delta U_{Nd} = (\xi^N - \xi_{id}^N) \cdot U_o \qquad (2)$$

The results of the calculations are shown in fig. 3, which shows that absolute error from instantaneous change of capacitance of accumulative capacitor by interelectrode parasitic capacitances decreases together with decrease of parasitic capacitances and at their values of no more than 4pF absolute error is less than 4.1 μV .

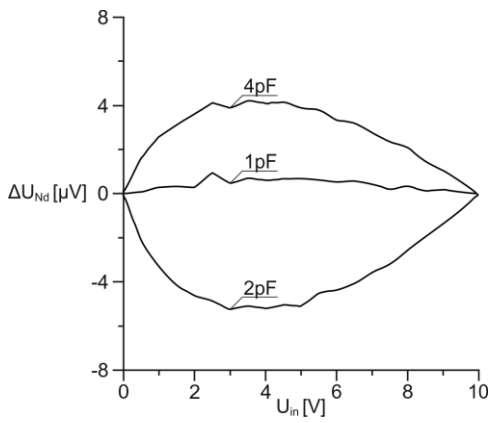

Figure 3. Absolute error of voltage on accumulative capacitor measured from instantaneous change of capacitance C

B. Leakage of control voltage.

Let us consider a change in voltage on the accumulative capacitor from leakage of control voltage through parasitic capacitances of switch SW1.

Using superposition principle and omitting resistance of switch SW1 in the on state, we receive model of LADC with feedback, which takes into account leakage of control voltage (fig. 4). In fig. 4 marked

$$C_{1e} = C_{gs} + C_{gd}\,; \quad C_{2e} = C + 2C_{gd} + 2C_{gs} + C_{in} + C_{out}\,.$$

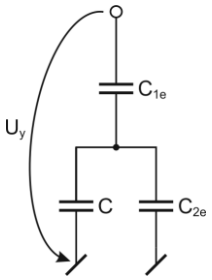

Figure 4. Model of LADC with charge accumulation and impulse feedback which takes into account effect of control voltage leakage

As you can see, fig. 4 shows diagram of capacitive voltage divider. Control voltage U_y is divided by the divider and gives an increase of voltage on the accumulative capacitor (ΔU).

$$\Delta U = \frac{C_{gs} + C_{gd}}{C + 3C_{gd} + C_{gs} + 2C_{gs} + C_{in} + C_{out}} \cdot U_y \qquad (3)$$

Let us consider process of charge collecting, taking into account an increase in voltage on accumulative capacitor from leakage of control voltage through interelectrode parasitic capacitances from switch SW1 .

After first clock impulse (first tact) voltage on accumulative capacitor from leakage of control voltage will have value of

$$U_{1y} = \xi U_0 - \Delta U\,,$$

where ΔU - increase of voltage on accumulative capacitor from leakage of control voltage.

After second clock impulse (second tact) voltage on accumulative capacitor will be equal to

$$U_{2y} = \xi U_{1y} - \Delta U \quad \text{or}$$

$$U_{2y} = \xi^2 U_0 - \xi\Delta U - \Delta U =$$

$$= \xi^2 U_0 - (\xi + 1)\cdot\Delta U$$

After third clock voltage on accumulative capacitor will be equal to

$$U_{3y} = \xi U_{2y} - \Delta U \quad \text{or}$$

$$U_{3y} = \xi^3 U_0 - \xi(\xi + 1)\cdot\Delta U - \Delta U =$$

$$= \xi^3 U_0 - (\xi^2 + \xi + 1)\cdot\Delta U$$

Similarly, we find voltage on accumulative capacitor, taking into consideration leakage of control voltage and after next N clock impulses

$$U_{Ny} = \xi^N U_0 - (\xi^{N-1} + \xi^{N-2} + \ldots +$$

$$+ \xi^2 + \xi + 1)\cdot\Delta U$$

or by using a known formula for sum of terms of geometrical progression

$$U_{Ny} = \xi^N U_0 - \frac{1-\xi^N}{1-\xi}\cdot\Delta U \qquad (4)$$

First term on the right side of above formula is the value of voltage on accumulative capacitor after collecting N clock impulses taking into consideration error from instantaneous changes of capacitance of accumulative capacitor and second term – absolute error of the voltage (ΔU_{Ny}), caused by the effect of leakage of control voltage

$$\Delta U_{Ny} = \frac{1-\xi^N}{1-\xi}\cdot\Delta U \qquad (5)$$

Fig. 5 presents a graph of error from leakage of control voltage. It shows that this error is negative and that increase of absolute value with increasing interelectrode parasitic capacitance (C_P) is equal to -1 mV for C_p = 1 pF, -2mV for C_p = 2 pF and -4 mV for C_p = 4 pF.

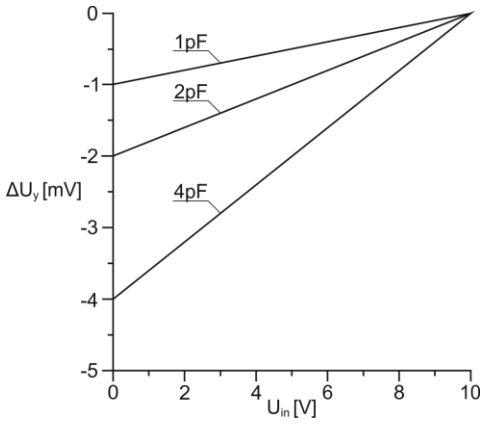

Figure 5. Absolute error of voltage on accumulative capacitor from leakage of control voltage

C. Transfer of parasitic charge.

As mentioned above, when switch SW1 turns off parasitic charge, which accumulated on interelectrode parasitic capacitance gate-drain of switch SW1 (in time when control voltage is on its gate) transfers itself on accumulative capacitor.

We formulated model of LADC with charge accumulation an impulse feedback (fig.6), which takes into account influence of carrying parasitic charge. Using this model, we can define voltage on accumulative capacitor after carrying parasitic charge, collected on capacitance gate-drain C_{gd1} key SW1. It is important to remember that transferring charge takes place after turning off switch SW1.

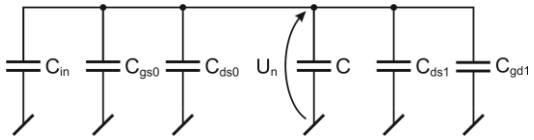

Figure 6. Model of LADC with charge accumulation and impulse feedback, which takes into account the effect of carrying parasitic capacitance of switch during discharge

Parasitic charge gathered on capacitance C_{gd1} at the end of the first clock impulse is equal to

$$Q_{n1} = (U_y + U_{1y}) \cdot C_{gd1}$$

At the same time summary charges of capacitors

$$Q_1 = Q_{c1} + Q_{n1},$$

where $Q_{c1} = C_1 \cdot U_{1y}$;

$$C_1 = (C_{ds1} + C_{gd0} + C_{ds0} + C + C_{in}).$$

so

$$Q_1 = (C + C_{gd0} + 2C_{ds} + C_{in}) \cdot U_{1y} + (U_y + U_{1y}) \cdot C_{gd}.$$

On the other hand summary charge

$$Q_1 = (C + 2C_{gd} + 2C_{ds} + C_{in}) \cdot U_1 .$$

Equalizing the right parts of the last two equations for summary charge let us define voltage on accumulative capacitor after first clock impulse, taking into account effects of transferring parasitic charge and leakage of control voltage.

$$U_1 = U_{1y} + kU_y \quad \text{or} \quad U_1 = \xi U_0 - \Delta U + kU_y ,$$

where

$$k = \frac{C_{gd}}{C + 2C_{gd} + 2C_{ds} + C_{in}} \tag{6}$$

U_{1y} - defined above, voltage value on accumulative capacitor after first clock impulse with taking into consideration effect of control voltage leakage

$$(\ U_{1y} = \xi U_0 - \Delta U\ ).$$

Similarly, we find voltage on accumulative capacitor and after next clock impulses.

On second tact of conversion in the time of discharge, when switch SW1 is turned on, voltage on accumulative capacitor (with taking into consideration charge carrying in previous clock impulse and transfer of control voltage)

$$U_{2y} = \xi U_1 - \Delta U \quad \text{or} \quad U_{2y} = \xi^2 U_0 - (\xi + 1) \cdot \Delta U + \xi k U_y$$

After second clock impulse (switch SW1 turned off) voltage on accumulative capacitor

$$U_2 = U_{2y} + kU_y \quad \text{or} \quad U_2 = \xi^2 U_0 - (\xi + 1) \cdot \Delta U + (\xi + 1) \cdot kU_y$$

Similarly, in the third tact of conversion during discharging, when switch SW1 is turned on, voltage on accumulative capacitor

$$U_{3y} = \xi U_{2y} - \Delta U \quad \text{or}$$

$$U_{3y} = \xi^3 U_0 - (\xi^2 + \xi + 1) \cdot \Delta U + (\xi + 1) \xi k U_y$$

and after turning off switch SW1 voltage on accumulative capacitor

$$U_3 = U_{3y} + kU_y \quad \text{or}$$

$$U_3 = \xi^3 U_0 - (\xi^2 + \xi + 1) \cdot \Delta U + (\xi^2 + \xi + 1) \cdot kU_y$$

In the end, after N-th tact of conversion when switch SW1 is turned off, voltage on accumulative capacitor (with taking into consideration charge carrying and transfer of control voltage) will be equal to

$$U_N = \xi^N U_0 - (\xi^{N-1} + \xi^{N-2} + \ldots + \xi^2 + \xi + 1) \cdot \Delta U + (\xi^{N-1} + \xi^{N-2} + \ldots + \xi^2 + \xi + 1) \cdot kU_y \quad \text{or}$$

$$U_N = \xi^N U_0 - \frac{1 - \xi^N}{1 - \xi} \cdot \Delta U + \frac{1 - \xi^N}{1 - \xi} \cdot kU_y \tag{7}$$

On the right side of the equation (7) first term is the value of voltage on accumulative capacitor, taking into account error from the immediate changes of capacitance of accumulative capacitor, second – absolute error ΔU_{Ny} from leakage of control voltage, third – absolute error ΔU_{Nq} from carrying parasitic charge of switch SW1 during discharging

$$\Delta U_{Nq} = \frac{1 - \xi^N}{1 - \xi} \cdot kU_y \tag{8}$$

Calculated graphs of absolute error ΔU_{Nq} from carrying parasitic charge of switch SW1 during discharge are shown in fig. 6, which shows, that error ΔU_{Nq} is positive and amounts 0.5 mV when C_p = 1 pF , 1 mV when C_p = 2 pF and 2 mV when C_p = 4 pF.

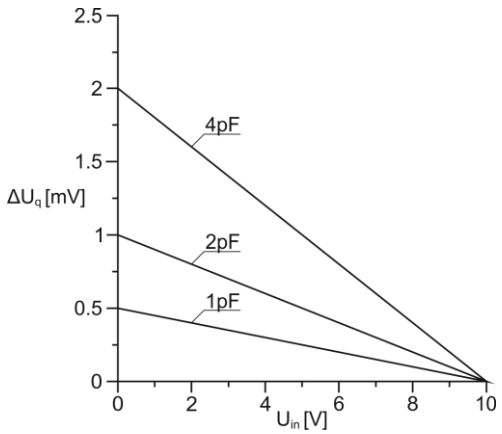

Figure 6. Absolute error of voltage on accumulative capacitor from carrying out parasitic charge during discharging of the switch

Resulting summative absolute error (ΔU_{Nc}), caused by an impact of interelectrode parasitic capacitance, will be equal to

$$\Delta U_{Nc} = (\xi^N - \xi_{id}^N) \cdot \mathrm{U}_0 + \frac{1 - \xi^N}{1 - \xi} \cdot (kU - \Delta U) \tag{9}$$

The results of the calculations of summative absolute error (ΔU_{Nc}) are shown in fig.7, which shows that this error ΔU_{Nc} is negative and amounts -0.5 mV when C_p = 1 pF, -1 mV for C_p = 2 pF and -2 mV for C_p = 4 pF.

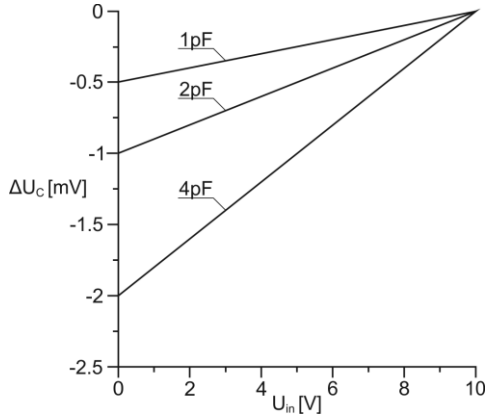

Figure 7. Summative absolute error from influence of interelectrode parasitic capacitances of components

III. An evaluation of accuracy of LADC with charge accumulation an impulse feedback.

Error of LADC, as also error of any other measurement or conversion system, consists of methodological and instrumental errors.

As it is well known, methodological error of ADC is quantization error (δ_m), and instrumental error (δ_i) is error which occurs due to non-ideal components of ADC.

We define methodological and instrumental errors, using methods by which we can find the resulting (summation) error of LADC.

Adding errors will consider presence of correlation between particular errors and will organize them to corresponding groups by correlation coefficient. The sum of two errors, including correlation is defined according to the formula

$$\delta_{12} = \sqrt{\delta_1^2 \pm 2\kappa\delta_1\delta_2 + \delta_2^2}$$

where δ_1 and δ_2 correspondingly first and second error

κ - correlation coefficient, which is equal to zero when there is no correlation between errors and one when there is strong correlation.

It should also be borne in mind, that in order to determine resulting error (summative) one should use together nominal errors as separate components.

Summation error of LADC (δ_{SUM}) is equal to sum of instrumental and methodological errors, which are not correlated with each other. In relation to this correlation coefficient takes value of zero ($\kappa = 0$) and summation error of LADC is defined by an equation

$$\delta_{SUM} = \sqrt{\delta_i^2 + \delta_m^2} \tag{10}$$

Relative error of quantization (δ_m) of LADC depends on choice of base value of logarithm ξ and is constant over the entire range of input signals. Its value can be found by an equation

$$\delta_m = \frac{1-\xi}{\zeta} \cdot 100\% \tag{11}$$

So δ_m = 0.35 % at ξ = 0,9965522 (N = 2000) and δ_m = 0.1 % at ξ = 0,9990009 (N = 9214).

Instrumental error of LADC is determined by non-ideal components, and in particular by the influence of interelectrode parasitic capacitances and leakage currents.

At the same time, error from: voltage polarization of VF, VCT, Cmp, deviation from nominal value of capacitance of accumulative capacitor and VCT resistors is omitted. VCT resistors set value of logarithm base, these components are compensated by adjusting LADC.

Evaluation of instrumental errors of various LADC we will make with use of high-quality components, including OAs of small input currents, for example OA K1409, for which input currents are less than 50pA, and analog switches, for example switch K590, in the best of these interelectrode parasitic capacity is not higher than 2pF and leakage currents smaller than 100pA.

Instrumental error of LADC is equal to (because its components are not correlated with each other, the correlation coefficient $\kappa = 0$)

$$\delta_i = \sqrt{\delta_C^2 + \delta_{IL}^2} \tag{12}$$

where: δ_C - relative error of parasitic capacitances C_p, δ_{IL} - relative error of leakage currents.

Research of LADC was carried out for range of input signals from 1mV to 10V. In this context, taking into account input signals specified above, nominal error of LADC from influence of interelectrode parasitic capacitances does not exceed 0.01% (with $C_p \leq 2$ pF), and leakage current less than 0,0016%. Since this last error is much smaller, instrumental error of LADC actually is defined as error from the impact of interelectrode parasitic capacitances, i.e. $\delta_i \approx \delta_c \leq 0{,}01\%$.

By setting error of quantization at 0,1%, summative error of described LADC with charge accumulation and impulse feedback will be obtained according to formula (10): $\delta_{SUM} \approx 0{,}1\%$.

IV. Conclusions

On the basis of conducted research of LADC with charge accumulation and impulse feedback, it can be concluded that:

1. Impact of interelectrode parasitic capacitances of switches, VF and VCT on process of conversion is caused by: instantaneous change of capacitance of accumulative capacitor, leakage of control voltage and transfer of parasitic charge of gate of switch SW1 during discharge.
2. Instrumental error from the impact of interelectrode parasitic capacitance of the components of LADC with charge accumulation and impulse feedback does not exceed 0.01 % at C_p = 2 pF (0.005% at C_p = 1pF) and is much smaller than in LADC with charge redistribution and LADC with charge accumulation on active and passive capacitor cells.
3. Summation error of LADC is practically totally determined by value of quantization error for values 0.1 % or more.
4. In instrumental error of LADC, there is dominant error from the influence of interelectrode parasitic capacitances of the components.

REFERENCES

[1] S. Purighalla, B. Maundy, "84-dB Range Logarithmic Digital-to-Analog Converter in CMOS 0.18-µm Technology," *IEEE Transactions on Circuits and Systems II: Express Briefs*, 58 (2011), no.5, pp. 279-283

[2] J. Lee, J. Kang, S. Park, J. Seo, J. Anders, J. Guilherme, M. P. Flynn, "A 2.5 mW 80 dB DR 36 dB SNDR 22 MS/s Logarithmic Pipeline ADC," *IEEE Journal Of Solid-State Circuits*, 44 (2009), no.10, pp. 2755-2765

[3] B. Maundy, D. Westwick, S. Gift, "On a class of pseudo-logarithmic amplifiers suitable for use with digitally switched resistors," *Int. J. of Circuit Theory and Applications*, vol. 36 (2008), no.1, pp. 81–108

[4] B. Maundy, D. Westwick, S. Gift, (2007) "A useful pseudo-logarithmic circuit," *Microelectronics International*, Vol. 24 Iss: 2, pp.35 - 45

[5] M. Alirieza, L. Jing and J. Dileepan, ¨Digital Pixel Sensor Array with Logarithmic Delta-Sigma Architecture," *Sensors*, 13(8), pp. 10765-10782, August 2013

[6] J. Guilherme, J. Vital, Jose Franca, "A True Logarithmic Analog-to-Digital Pipeline Convener with 1.5bitistage and Digital Correction," *Proc. IEEE International Conference on Electronics Circuits and Systems*, pp. 393-396, Malta 2001

[7] G. Bucci, M. Faccio, C. Landi, "The performance test of a piece-linear A/D converter," *IEEE Instrumentation and Measurement Technology Conference*, St. Paul USA May 1998, pp.1223.1228

[8] J. Guilherme, J. Vital, J. Franca, "A CMOS Logarithmic Pipeline *A/D* Converter with a Dynamic Range of 80 dB," *IEEE Electronics, Circuits and Systems, 2002. 9th International Conference on,* (2002), no.3/02, pp. 193-196

[9] J. Sit and R. Sarpeshkar, "A Micropower Logarithmic A/D With Offset and Temperature Compensation," *IEEE J. Solid-State Circuits*, 39 (2004), nr. 2, pp. 308-319

[10] J. Mahattanakul, "Logarithmic data converter suitable for hearing aid applications," *Electronic Letters*, 41 (2005), no.7, pp. 31-32

[11] S. Sirimasakul, A. Thanachayanont, W. Jeamsaksiri, "Low-Power Current-Mode Logarithmic Pipeline Analog-to-Digital Converter for ISFET based pH Sensor," *IEEE ISCIT*, 2009, no.6/09, pp. 1340-1343

[12] M. Santosa, N. Hortaa, J. Guilherme, "A survey on nonlinear analog-to-digital converters," *Integration, the VLSI Journal,* Volume 47, Issue 1, pp. 12–22, January 2014

[13] Z.R. Mychuda, "Logarithmic Analog-To-Digital Converters – ADC of the Future," Prostir, Lviv, Ukraine 2002, pp. 242

[14] A. Szcześniak, Z Myczuda, "A method of charge accumulation in the logarithmic analog-to-digital converter with a successive approximation," *Electrical Review*, 86 (2010), no.10, pp. 336-340

[15] A. Szcześniak, U. Antoniw, Ł. Myczuda, Z. Myczuda, „Logarytmiczne przetworniki analogowo-cyfrowe z nagromadzeniem ładunku i impulsowym sprzężeniem zwrotnym," *Electrical Review*, R. 89 no. 8/2013, pp. 277 – 281

[16] A. Szcześniak, Z. Myczuda, „Analiza prądów upływu logarytmicznego przetwornika analogowo-cyfrowego z sukcesywną aproksymacją," *Electrical Review,* 88 (2012), no. 5a, pp. 247-250

[17] J.H. Moon, D. Y. Kim, M. K. Song, Patent No. KR20110064514A, "Logarithmic Single-Slope Analog Digital Convertor, Image Sensor Device And Thermometer Using The Same, And Method For Logarithmic Single-Slope Analog Digital Converting,"

[18] J. Gorisse, F. A. Cathelin, A. Kaiser, E. Kerherve Patent No. EP2360838A1, "Method for logarithmic analog-to-digital conversion of an analog input signal and corresponding apparatus,"

[19] R. Offen Patent No. DE102008007207A1 "Logarithmierender Analog-Digital Wandler,"

[20] H. Suzunaga Patent No. US20080054163A1, "Logarithmic-compression analog-digital conversion circuit and semiconductor photosensor device,"