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Topology analysis and parameter design of three-level multi-input DC/DC converter based on multi-source access

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Abstract: A three-level multi-input DC/DC converter is proposed to solve the problems of complex interface circuit structure and high economic cost for multi-source access to the joint power supply distribution system. In this structure, multiple dc sources are integrated into a three-level DC/DC converter. In comparison with the two-stage counterpart, two active switches and boost diodes are eliminated, while two blocking diodes are added to block the reverse current from the dc-link capacitors. In addition, when the input inductors work in the discontinuous conduction mode, power sharing among different input sources can be achieved by properly selecting the inductance value. The working principle of the converter is analyzed by introducing nine working modes in detail and deriving the steady-state relationship expressions. The parameter range of the element is determined and the design process of a group of dynamic parameter values is shown. Finally, the power electronics real-time simulation platform is built based on StarSim HIL and the corresponding experimental waveforms are given to verify the topology and analysis.

Key words: multi-input converter; parameter design; power sharing; three-level; topology analysis



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1. Introduction

Recently, with the continuous development and application of renewable energy in distribution systems, the research of new energy technology is becoming a hotspot [1, 2]. However, most new energy sources are greatly limited by climate conditions, with intermittent and fluctuating power generation, unstable and discontinuous power supply, and other problems. Therefore, in order to solve the above problems, many scholars have proposed multi-source access to the joint power supply distribution system [3, 4]. Among them, the traditional multi-source access distribution system is that multiple input sources are connected to the dc bus through their respective single input DC/DC converters. It has the disadvantage of having a large number of converters in the system, which causes a high cost [5, 6]. In order to simplify the circuit structure and improve the device utilization, a multi-input DC converter (MIC) is used to replace the original multiple single-input DC converters to realize multi-source complementarity, which is of great significance to promoting the grid connection of new energy [7].

The MIC topologies are divided into non-isolated and isolated. The traditional non-isolated MIC can realize simultaneous or time-sharing power supply, which has a simple structure but can't achieve a high gain [8, 9]. A non-isolated high gain MIC topology is proposed in [10], which can achieve high gains and continuous input source current and adopt input sources with different voltage and current characteristics, but its input sources are not easy to expand. There is no isolation between input sources, lack of security protection, and circulation problem exists. An isolated MIC has advantages in isolation protection and avoiding leakage and circulating current, with high circuit safety, flexible distribution of input sources, and high-power density [11, 12]. An isolated multiport DC/DC converter based on a high-frequency transformer is proposed in [13]. The converter can be extended to n inputs, and its power can flow in both directions. However, by increasing the input source, the number of transformer windings and the complexity of their control also increase. An isolated MIC topology is proposed in [14], which has a small number of structural components, but the voltage stress of switches is large, and the system loss increases.

The switches of the two-level converter have high voltage stress and high requirements for device withstand voltage, which is not conducive to improving the system power density and reducing system cost [15–17]. Compared with the two-level converter, the voltage withstand value of the three-level converter is half of the output voltage. The switching loss is reduced, the overall efficiency is improved, and it is easy to modularize, parallelize, and expand. It is suitable for power generation systems with various voltage levels and powers [18, 19]. A double input half-bridge three-level converter is proposed in [20]. Compared with the double input full-bridge converter, the half-bridge three-level unit reduces the voltage utilization of the high-voltage input source and makes the duty cycle of the two units evenly distributed. It is suitable for situations where the voltage amplitude of the two input sources are greatly different. The three-level unit can also reduce the withstand voltage value of the switches, and the two freewheeling diodes also reduce the voltage stress of the switches. However, the topology has a large number of components, a high economic cost, and complex expansion.

In order to solve the above problems, a three-level multi-input DC/DC converter based on multi-source access is proposed in this paper. The specific arrangement is as follows: section 2 analyzes the topological structure and its working principle; section 3 deduces the expression of

the input-output relationship; section 4 determines the range of relevant parameters according to the phase-shifting control principle of the converter; section 5 verifies the correctness of the above theoretical analysis through simulation and experiment; finally, section 6 summarizes the article.

2. Working principle

The topology of the three-level multi-input DC/DC converter proposed in this paper is shown in Fig. 1. V_{11} and V_{21} are the two input sources, respectively, $S_1, S_2, S_3,$ and S_4 are the power switches, $D_3, D_4, D_5,$ and D_6 are the rectifier diodes, L_0 is the filter inductance, C_0 is the filter capacitor, R is the load, and the turn ratio of the transformer is $1:N$. The boost inductor and four switches form two boost circuit structures, respectively. The secondary side rectifier can be a half-bridge or full-bridge structure for low-voltage or high-voltage output. This paper is based on the analysis of the input inductance in the discontinuous conduction mode (DCM) with two input sources. In order to simplify the analysis, the working principle of the converter is discussed based on the following assumptions:

1. The power switching devices are ideal and inductors, capacitors are ideal devices with negligible parasitic effects.
2. The transformer has no leakage inductance, and its power loss is not considered.

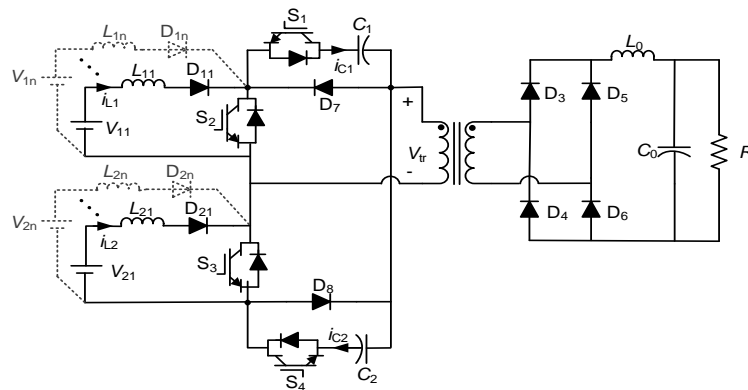


Fig. 1. Three-level multi-input DC/DC converter

The main working waveform of the converter is shown in Fig. 2. The switches S_2 – S_3 and S_1 – S_4 have 180° phase shifts with respect to each other. The duty cycle D_1 of intermediate switches S_2 and S_3 is greater than 0.5, which provides a freewheeling path for the current on the primary side of the transformer. When the converter works in DCM, its specific control scheme is when S_2 and S_3 are connected, respectively, the boost inductors are charged by different input sources and when S_2 or S_3 is closed, the energy in the inductance is transferred to the load. The excess or insufficient energy is absorbed or compensated by the capacitance. At the same time, the switching between S_1 and S_4 applies $V_{dc}/2, -V_{dc}/2,$ and zero voltage to the primary side of the transformer, respectively. The specific switching scheme is that S_1 is turned on immediately

after S_3 is turned off, and S_4 is turned on immediately when S_2 is turned off. At the moment when S_1 is on and S_3 is off, or the moment when S_2 and S_4 exchange switch status, the dead time shall be set to avoid a short circuit of capacitance due to the simultaneous conduction of the upper or lower three switches.

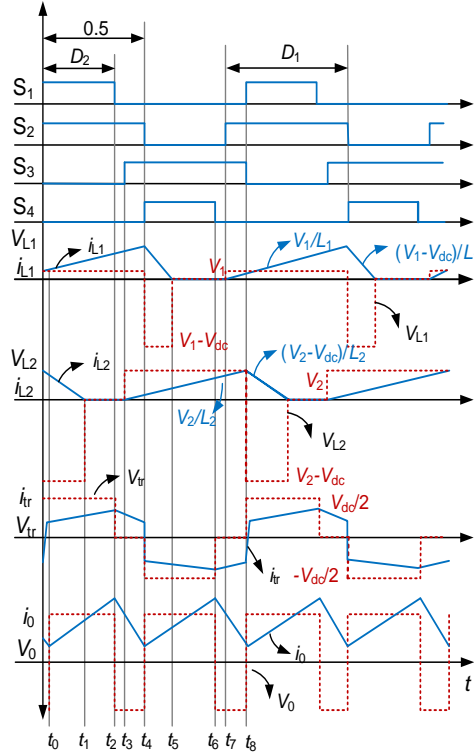


Fig. 2. The main working waveform of the converter

It can be divided into nine working modes in a switching cycle. The circuit structure of each working mode is shown in Fig. 3. The specific circuit working diagrams of different switching modes will be analyzed below.

Mode 1 [$t < t_0$]

As shown in Fig. 3(a), S_2 is on, and S_3 is off. The current of L_1 increases linearly under the action of V_1 , and the excess energy is charged to C_1 through the body diode of S_1 . Thus, S_1 can be turned on under zero voltage with proper time delay, the energy of L_2 is released to the load through the primary winding of the transformer, L_2 charges C_2 at the same time, and $-V_{dc}/2$ is applied to the primary side of the transformer.

Mode 2 [$t_0 < t < t_1$]

As shown in Fig. 3(b), when $t = t_0$, the current of the L_1 is equal to the current on the primary side of the transformer. At this moment, the energy in C_1 is discharged through the primary side load of the transformer, and the current of C_2 is equal to the current of L_2 .

Mode 3 [$t_1 < t < t_2$]

As shown in Fig. 3(c), when $t = t_1$, L_1 continues to store energy under the action of V_1 , S_1 and S_2 are turned on, the currents of L_2 and C_2 reach zero, and the load current is only provided by C_1 .

Mode 4 [$t_2 < t < t_3$]

As shown in Fig. 3(d), S_1 is turned off, S_2 is continuously on, D_7 is on, zero voltage is applied to the primary side of the transformer, the output voltage is $-V_0$, and i_{L0} decreases linearly.

Mode 5 [$t_3 < t < t_4$]

As shown in Fig. 3(e), when $t = t_3$, S_2 and S_3 are on, L_2 stores energy under the action of V_2 . The primary side current flows to the load through D_7 , the primary side voltage continues to be zero, and the output inductance current continues to decrease under the action of the output voltage.

Mode 6 [$t_4 < t < t_5$]

As shown in Fig. 3(f), when $t = t_4$, S_2 is turned off, S_4 is turned on, and the energy stored in L_1 is released into load and C_1 . C_2 discharges to the load, and the primary side of the transformer is applied to $V_{dc}/2$. L_2 continues to store energy under the action of V_2 .

Mode 7 [$t_5 < t < t_6$]

As shown in Fig. 3(g), when $t = t_5$, the energy stored in L_1 is completely transferred out, its current reaches zero at DCM, and the load current is only provided by C_2 .

Mode 8 [$t_6 < t < t_7$]

As shown in Fig. 3(h), S_4 is turned off, the primary side current flows to the load through D_8 , zero voltage is applied to the primary side of the transformer and the current in L_2 continues to increase.

Mode 9 [$t_7 < t < t_8$]

As shown in Fig. 3(i), when $t = t_7$, S_2 is on, while S_3 remains on, the primary side current continues to circulate in D_8 , and the currents of L_1 and L_2 increase linearly under the applied input voltage.

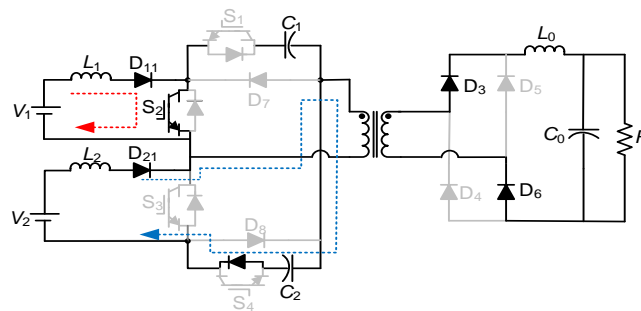
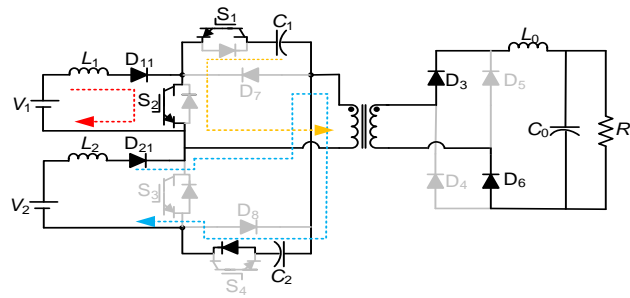
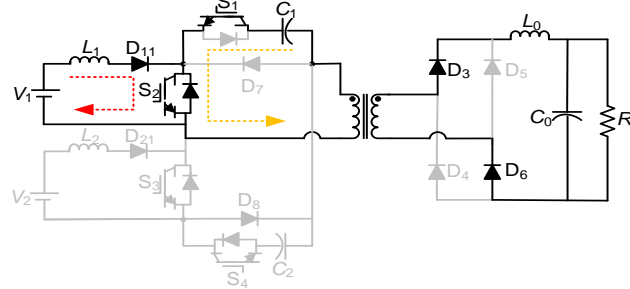
(a) Mode 1 [$t < t_0$]

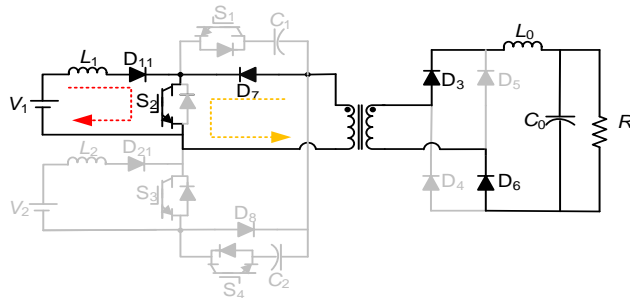
Fig. 3



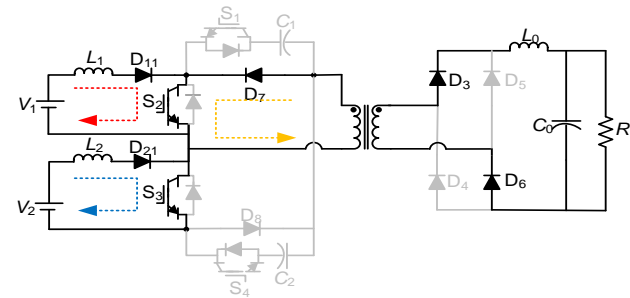
(b) Mode 2 [$t_0 < t < t_1$]



(c) Mode 3 [$t_1 < t < t_2$]

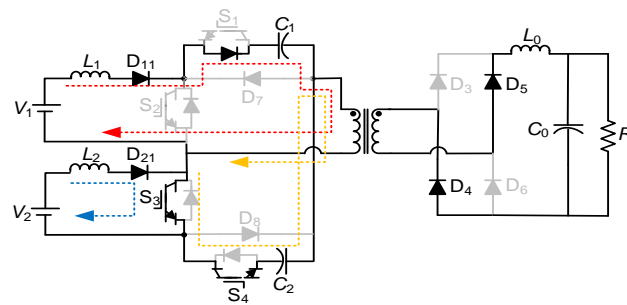


(d) Mode 4 [$t_2 < t < t_3$]

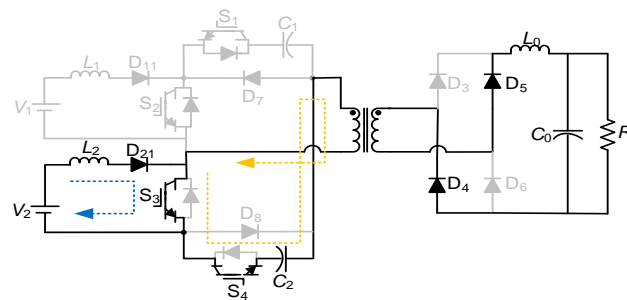


(e) Mode 5 [$t_3 < t < t_4$]

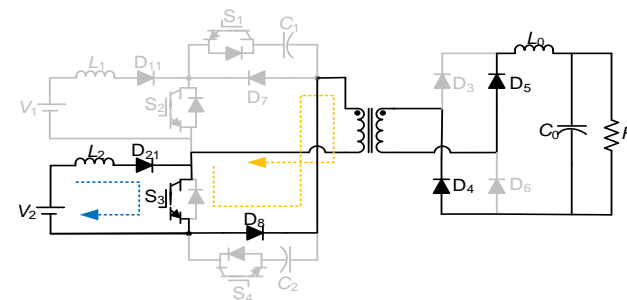
Fig. 3



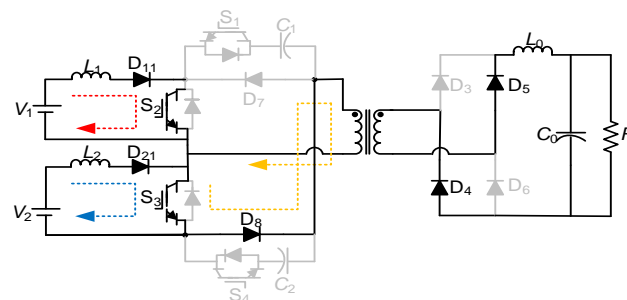
(f) Mode 6 [$t_4 < t < t_5$]



(g) Mode 7 [$t_5 < t < t_6$]



(h) Mode 8 [$t_6 < t < t_7$]



(i) Mode 9 [$t_7 < t < t_8$]

Fig. 3. Switching mode circuit diagram

3. Steady-state characteristic

3.1. Voltage expressions

The performance of the converter will be analyzed in detail below, which mainly includes the steady-state performance of each storage element (such as L_1 , L_2 , C_1 , and C_2). The currents flowing through the boost inductors L_1 and L_2 are i_{L1} and i_{L2} , respectively. In addition, the voltages passing through the capacitors C_1 and C_2 are V_{C1} and V_{C2} , respectively. In order to ensure that overshoot will not occur due to switching, it is necessary to consider switching between S_2 , S_3 and S_1 , S_4 to provide a proper freewheeling path and reversal of polarity. The relationship between D_1 and D_2 (the duty cycle of S_1 and S_4) is as follows:

$$D_1 = 1 - D_2 - D_B, \quad (1)$$

where D_B is the duty cycle of dead time.

For the transformer with a turn ratio of 1 : N , the following formula can be obtained:

$$V_{tr} = V_0/N, \quad (2)$$

$$I_{tr} = NI_0, \quad (3)$$

where V_{tr} is the primary side voltage and I_{tr} is the primary side current.

When the converter is in steady-state operation, in one cycle T , according to the volt second balance principle of L_1 and L_2 , the change value of the inductor current is zero. Applying volt second balance across L_1 , the following formula can be obtained:

$$V_1 D_1 + (1 - D_1)(V_1 - V_{tr} - V_{C1}) = 0, \quad (4)$$

$$V_{tr} = \frac{V_1}{(1 - D_1)} - V_{C1}. \quad (5)$$

Similarly, applying volt second balance across L_2 , the following formula can be obtained:

$$V_2 D_1 + (1 - D_1)(V_2 - V_{tr} - V_{C2}) = 0, \quad (6)$$

$$V_{tr} = \frac{V_2}{(1 - D_1)} - V_{C2}. \quad (7)$$

According to (5), it can be seen clearly when V_1 is powering the load, C_2 is discharging and C_1 is getting charged by i_{L1} . In addition, (6) clearly shows when V_2 is powering the load, C_1 is discharging and C_2 is getting charged by i_{L2} .

The relevant expressions of V_0 and D_1 can be obtained:

$$V_0 = N \times V_{tr} = \frac{N}{2} \left(\frac{V_1 + V_2}{(1 - D_1)} - (V_{C1} + V_{C2}) \right) = \frac{N(V_1 + V_2)}{4(1 - D_1)}, \quad (8)$$

$$D_1 = \left(1 - \frac{V_1}{(V_{tr} + V_{C1})} \right) = \left(1 - \left(\frac{V_2}{(V_{tr} + V_{C1})} \right) \right). \quad (9)$$

3.2. Current expressions

When the converter is in steady-state operation, in one cycle T , according to the ampere second balance principle of C_1 , the change value of capacitor voltage is zero, and the following formula can be obtained:

$$-D_2(I_{tr} - I_{L1}) + (1 - D_1)(I_{L2}) = 0, \quad (10)$$

$$I_{tr} = \frac{I_{L2}(D_2 + D_B)}{D_2} + I_{L1}. \quad (11)$$

Similarly, following the ampere second balance principle of C_2 , the relevant expressions are as follows:

$$-D_2(I_{tr} - I_{L2}) + (D_2 + D_B)(I_{L1}) = 0, \quad (12)$$

$$I_{tr} = \frac{I_{L1}(D_2 + D_B)}{D_2} + I_{L2}. \quad (13)$$

Finally, the relevant expressions of I_0 and D_2 can be obtained:

$$I_0 = \frac{I_{tr}}{n} = \frac{1}{2n} \left(\frac{(I_{L1} + I_{L2})(D_2 + D_B)}{D_2} + I_{L1} + I_{L2} \right), \quad (14)$$

$$D_2 = \left(\frac{D_B \times I_{L1}}{(I_{tr} - I_{L1} + I_{L2})} \right) = \left(\frac{D_B \times I_{L2}}{(I_{tr} - I_{L1} + I_{L2})} \right). \quad (15)$$

From (11) and (13), it can be seen that the control of two input currents can be realized by controlling the duty cycle of the switch so as to realize the maximum power tracking control. (5), (7), (11), and (13) clearly show that the input power in DCM and continuous conduction mode (CCM) is equal. According to the above analysis, the relationship between the output voltage and output current can be synthesized by the average value as shown in (8) and (14).

3.3. Comparative analysis

Table 1 shows the comparison of some characteristics between the proposed converter and the converters mentioned in references [14] and [20].

Table 1. Comparison between the proposed converter and some other converters

Variable name	Converter proposed in [14]	Converter proposed in [20]	Converter proposed in this paper
switching withstand voltage	V_{dc}	$V_{dc}/2$	$V_{dc}/2$
switches	4	8	4
diodes	6	8	8
inductors	4	1	3
capacitors	6	7	3

Table 1 shows some characteristics comparison between the proposed converter (represented by A in the following text) and the converters (represented by B and C, respectively in the following text) in references [14] and [20]. Although A has two more diodes compared with B, the withstand voltage value of A's switches is obviously lower than B's. As A has input inductance, the ripple value of input current will also be significantly lower than C. In addition, although the voltage withstand value of the switches of C is equal to that of A, the number of switches, diodes, inductors and capacitors is more than that of A, which increases the cost of the converter. Therefore, the converter proposed in this paper has more advantages in economic cost.

4. Parameters design

Proper component parameters are the precondition to ensure the normal operation of the converter. The condition of $D_1 \geq 0.5$ can be obtained from section 2 and the remained 0.5 is shared between D_2 and D_B which leaves a margin for the duty cycle D_1 . Then the value of each duty cycle can be determined according to the following formula:

$$D_B = 0.5 - D_{2,\max}, \quad (16)$$

where $D_{2,\max}$ is the maximum value of D_2 .

1) Determination of L_0 , D_2 , and D_B

The load side of the converter can operate in CCM or DCM. That is, the output inductance current can be continuous or discontinuous, or the converter can transit to DCM under light load conditions to reduce the size of the output inductance. The output inductance can be determined by the following formula:

$$L_0 \geq \frac{V_0^2(0.5 - D_{\min})}{2P_x f_s}, \quad (17)$$

where P_x is the minimum output power of the converter in CCM, and D_{\min} is the minimum duty cycle.

When the output inductance works in CCM, the following formula can be obtained:

$$D_{2,\max} = \frac{NV_0}{V_{dc,\min}}, \quad (18)$$

where N is the turn ratio of the transformer and $V_{dc,\min}$ is the minimum value of DC-link voltage.

The equivalent duty cycle in DCM can be written as:

$$D_2 = \sqrt{\frac{2L_0}{RT_s \left(\left(\frac{V_{dc}}{NV_0} - 1 \right)^2 - 1 \right)}}, \quad (19)$$

where T_s is the time period.

According to different operation modes, N can be found from (18) or (19). Once $D_{2,\max}$ and $V_{dc,\min}$ are determined, D_B can be obtained from (16).

2) Determination of the DCM boundary and DC-link voltage

The input sources are controlled by D_1 , and the voltage levels of the two input sources may be different. Only one input source would be able to operate in CCM, while the other input source would continue operating in DCM. If one of the input sources is switched to CCM, the inductive current will be continuously output, and $-V_{dc}$ will be forcibly applied to the other input source to keep the voltage of latter at the same level. Hence, latter continues to provide same amount of power in DCM while the remaining power will be provided by the input source operating in CCM. This operation could be considered for applications where the output power of photovoltaic power can be maximized to its limit value, and wind energy can provide the residual load power demand.

The operation modes shown in Fig. 3 are based on the analysis in DCM. The input inductance can be selected under any load, and the input inductance current reaches zero in D_2T_s . However, if the interval lasts longer, depending on the selected parameters and output power, there may be other operating modes not given in Fig. 3. Therefore, in order to define the boundary of CCM and DCM, it is necessary to analyze this working mode. After the operation interval 7, even if S_4 is closed under the influence of $V_{dc}/2$, L_2 will continue to charge C_2 through the diode of S_4 until D_8 is turned on. The voltage of the primary side of the transformer remains at zero since D_8 conducts. The relevant waveform is shown in Fig. 4.

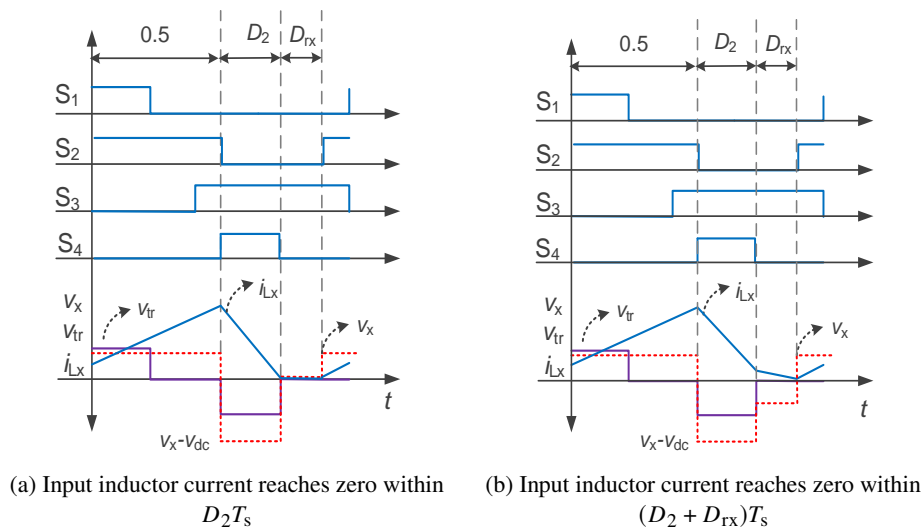


Fig. 4. DCM/CCM boundary sample diagram

There D_{rx} denotes the duty ratio of the time interval in which inductor current decreases from its peak value to zero when the boost switch is turned off. V_x provides input source voltage with higher output power and i_{Lx} represents inductive current.

In order to find the operating boundary point, it should be considered that the inductive current reaches zero at the end of the switching period. The critical DC-link voltage can be found by the

inductance voltage balance expression as follows:

$$V_x D_1 = (V_{dc,art} - V_x) D_2 + \left(\frac{V_{dc,art}}{2} - V_x \right) (1 - D_1 - D_2). \quad (20)$$

The lowest DC-link voltage that adopted for DCM operation can be expressed as:

$$V_{dc,art} = \frac{2V_x}{D_2 - D_1 + 1}. \quad (21)$$

For DCM, the following condition shall be met: $V_{dc,min} > V_{dc,art}$.

3) Determination of L_1 and L_2

For the converter studied in this paper, the duty cycle of S_2 and S_3 is the same, which is equal to D_1 . Therefore, the output power of each input source is proportional to the square of its input voltage and inversely proportional to the inductance. The total power P_0 of the input source can be expressed as:

$$P_0 = \eta \frac{V_{dc} D_1^2 T_s}{2} \sum_1^n \frac{V_n^2}{L_n (V_{dc} - V_n)}. \quad (22)$$

Therefore, power sharing can be realized by designing appropriate parameters for different input sources. According to (22), there are many schemes to determine L . The bottom boundaries for L_n based on $V_{n,min}$ and output power are defined as:

$$P_{max} = \eta \frac{V_{dc} D_{1,max}^2 T_s}{2} \sum_1^n \frac{V_{n,min}^2}{L_n (V_{dc} - V_{n,min})}. \quad (23)$$

The values of corresponding inductances can be determined according to different application requirements. Such as in PV generation systems, the corresponding inductances can be determined by the expected load distribution at the maximum power operation point.

In addition to finding all possible L_1 and L_2 combinations based on (23), the inductance parameters value can also be determined by the power ratio between input sources under the required input voltage. Under the maximum output power and minimum input voltage, the power ratio of the second input source to the first input source is represented by γ . Based on the selected γ , the inductive parameters value can be determined, as shown in Fig. 5.

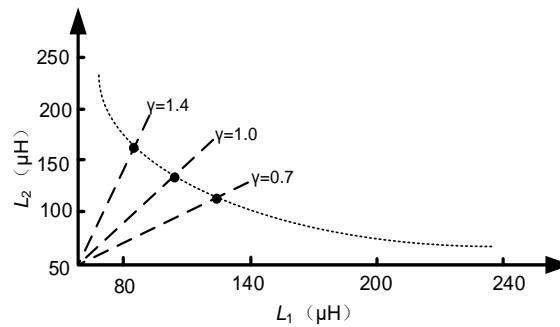
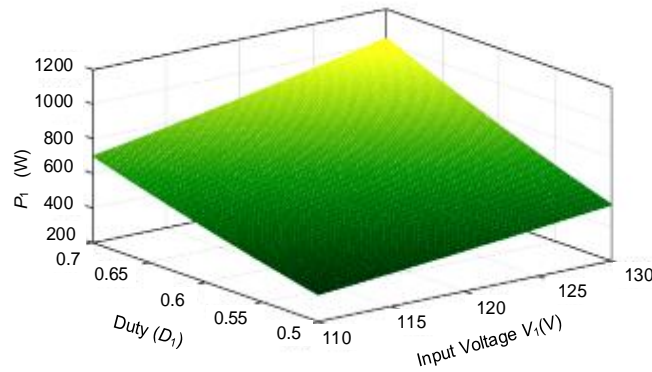


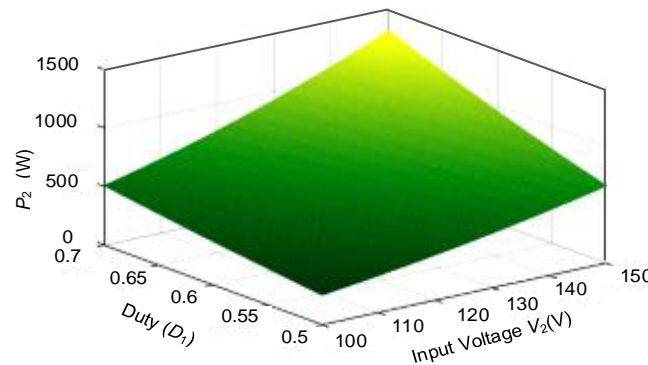
Fig. 5. Parameters curve variation diagram based on γ value ($V_1 = V_{1,min}$, $V_2 = V_{2,min}$)

The design process of a constant value load with a constant input voltage source is relatively simple. A set of design processes with dynamic parameter variables are shown below. The specific parameters are as follows: $V_{1,\min} = 110$ V, $V_{1,\max} = 130$ V, $V_{2,\min} = 100$ V, $V_{2,\max} = 150$ V, $V_0 = 200$ V, $f_S = 50$ kHz, $P_{\text{tot,max}} = 1.2$ kW. The duty cycle D_2 of a typical bridge isolation converter ranges from 0.25 to 0.48. Due to certain restrictions on the duty cycle of the proposed converter, it can be set that $D_{1,\max}$ is 0.7 and D_1 varies from 0.5 to 0.7. From (16), D_B is 0.2, $D_{2,\max}$ is 0.3. The critical DC-link voltage V_{dc} can be obtained from (21), and $V_{dc,\text{art}}$ is 500 V. Therefore, $V_{dc,\min}$ is determined as 500 V. According to (18), the transformer turn ratio is 0.75. In this study, the value of γ is 0.7, that is, when $V_1 = V_{1,\min}$, $V_2 = V_{2,\min}$, the output power of the second input source is 500 W, and the output power of the first input source under the maximum load is 700 W. The corresponding inductance parameter value can be determined from Fig. 5, that is, $L_1 = 108$ μH , $L_2 = 122$ μH .

According to the duty cycle D_1 and the dynamic variation range of input voltage of different input sources, the dynamic variation of the corresponding output power is shown in Fig. 6.



(a) $D_{1,\min} = 0.5$, $D_{1,\max} = 0.7$, $V_{1,\min} = 110$ V, $V_{1,\max} = 130$ V



(b) $D_{1,\min} = 0.5$, $D_{1,\max} = 0.7$, $V_{2,\min} = 100$ V, $V_{2,\max} = 150$ V

Fig. 6. Power dynamic changes of different input sources under DCM

As can be seen from Fig. 6, the first input source provides 700 W and the second input source provides 500 W to meet the load demand of its minimum input voltage. When the voltage of the input source reaches the maximum value, the power ratio reaches 1.23, so the choice of γ depends entirely on application requirements and can be adjusted flexibly.

When $V_1 = V_{1,\min}$, $V_2 = V_{2,\min}$, $V_{dc,\min} = 500$ V, $V_{dc,\max} = 800$ V, the relationship between the total power provided by the input source and the duty cycle and DC-link voltage is shown in Fig. 7.

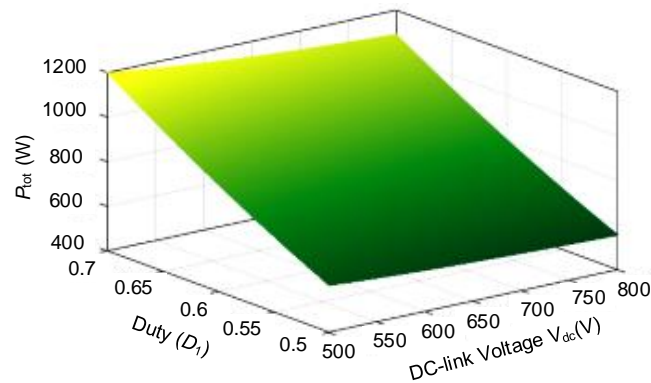


Fig. 7. Output power change dynamic diagram under DCM

Consistent with the theoretical analysis, when the output voltage is constant, the higher the DC-link voltage, the lower the output power. Therefore, the output power capability of the converter under different DC-link voltages can be evaluated, and the total output power can be adjusted for the given reference DC-link voltage. The above analysis only shows the design framework based on DCM. As mentioned earlier, one of the input sources can be switched to CCM and provides the remaining required power, which may be preferred in fuel cell applications.

5. Verification and analysis

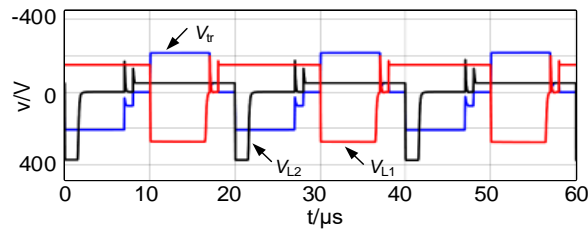
5.1. Simulation verification

In order to verify the working principle of the proposed converter, the converter with different parameters is simulated in MATLAB/Simulink. The first group of simulation is conducted for different input voltages with the same boost inductors, while the second group of simulation is conducted for the same input voltage with different boost inductors. D_1 is taken as 0.6, D_2 is taken as 0.35, and the switching frequency f_s is 50 kHz. The first group of specific simulation parameters are shown in Table 2.

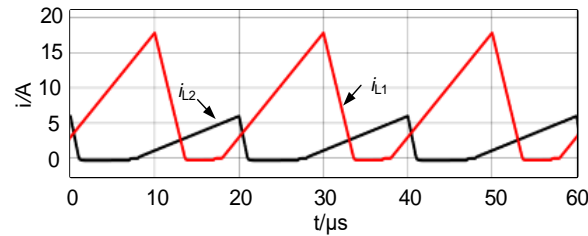
The first group simulates different input voltages with the same input inductance to obtain the voltage and current waveforms of the primary side of the transformer and various components, as shown in Fig. 8.

Table 2. The first group of simulation parameters

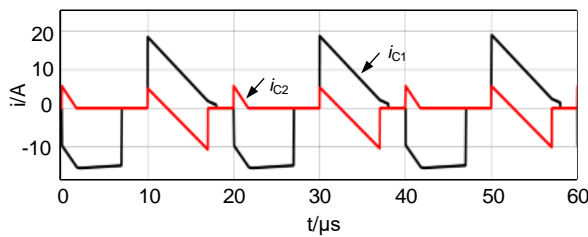
Parameters	Value
V_1	150 V
V_2	50 V
L_1/L_2	100 μ H
C_1/C_2	100 μ F
L_0	330 μ H
C_0	220 μ F
V_0	750 V



(a) Transformer primary side voltage and boost inductance voltage

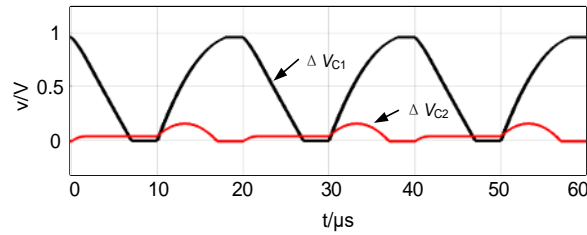


(b) Transformer primary side boost inductor current



(c) DC-link capacitance current

Fig. 8



(d) DC-link capacitance-voltage fluctuation

Fig. 8. Waveforms of $V_1 = 150$ V, $V_2 = 50$ V, $L_1 = L_2 = 100$ μ H

As can be seen from Fig. 8(a), even if the input voltage is different, the contribution of output power is the same under the same boost inductance. As can be seen from Fig. 8(b), $V_1 > V_2$, $L_1 = L_2$, the peak current of L_1 is 17.5 A, and the peak value of L_2 is 6 A, that is, $i_{L1, pk} > i_{L2, pk}$. As can be seen from Fig. 8(c), the charging and discharging currents of C_1 and C_2 are different, that is, $i_{C1} > i_{C2}$, which results in voltage fluctuation between the two DC-link, as shown in Fig. 8(d). For the proposed converter, it can be realized by adding the compensation signal to the duty cycle of S_1 and S_4 , which will extend or shorten its effective duty cycle and realize the capacitor voltage balance.

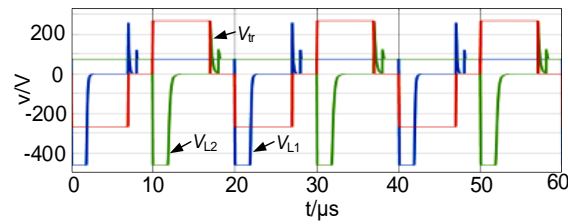
The second group of specific simulation parameters are shown in Table 3:

Table 3. The second group of simulation parameters

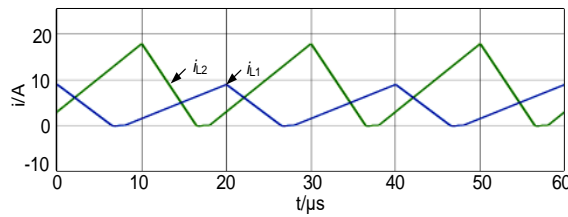
Parameters	Value
V_1/V_2	150 V
L_1	200 μ H
L_2	100 μ H
C_1/C_2	100 μ F
L_0	330 μ H
C_0	220 μ F
V_0	750 V

The second group simulates the same input voltage with different input inductances to obtain the voltage and current waveforms of the primary side of the transformer and various components, as shown in Fig. 9.

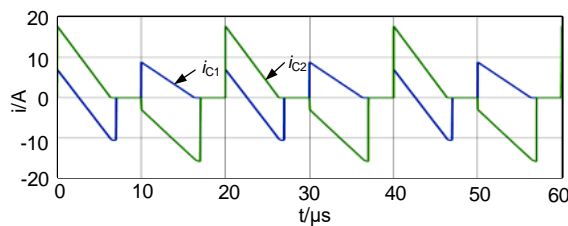
As can be seen from Fig. 9(a), even if the same voltage is applied to the boost inductor, the contribution of the corresponding output power is different due to the different inductance selected. As can be seen from Fig. 9(b), the peak current of L_1 is 9 A, and the peak value of L_2 is 17.5 A, that is, $i_{L1, pk} < i_{L2, pk}$. As can be seen from Fig. 9(c), due to the asymmetry of the input source, the capacitance current is different, and the charge-discharge current of C_1 is less than C_2 , resulting in the generation of capacitance voltage ripple.



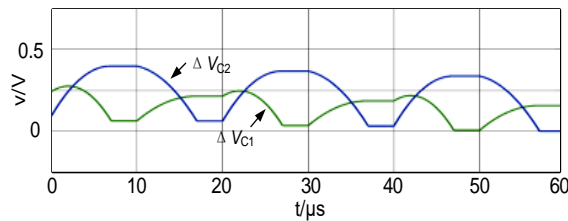
(a) Transformer primary side voltage and boost inductance voltage



(b) Transformer primary side boost inductor current



(c) DC-link capacitance current



(d) DC-link capacitance-voltage fluctuation

Fig. 9. Waveforms of $V_1 = V_2 = 150 \text{ V}$, $L_1 = 200 \text{ } \mu\text{H}$, $L_2 = 100 \text{ } \mu\text{H}$

The third group is to simulate and verify the dynamic change process of two input source voltage values. D_1 and D_2 are adjusted to 0.7 and 0.25. The parameters are as follows: $V_{1,\min} = 60 \text{ V}$, $V_{1,\max} = 70 \text{ V}$, $V_{2,\min} = 70 \text{ V}$, $V_{2,\max} = 110 \text{ V}$, $L_1 = L_2 = 87 \text{ } \mu\text{H}$, $C_1 = C_2 = 470 \text{ } \mu\text{F}$, $C_0 = 220 \text{ } \mu\text{F}$, $L_0 = 200 \text{ } \mu\text{H}$. The turn ratio N of the transformer winding is 1, and the switching frequency is 50 kHz. Under the same operating conditions, different input sources are simulated and verified, and the relevant voltage and current waveforms are obtained as follows.

As shown in Fig. 10, the two input source voltages are set to 70 V. It can be seen that two boost inductors provide a peak current of 9.5 A and share the required power of the load equally.

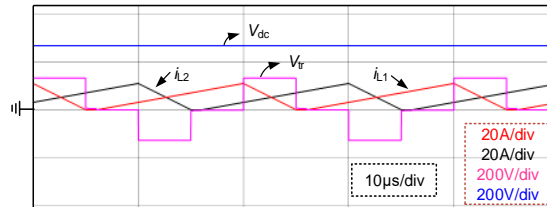


Fig. 10. Waveforms of $D_1 = 0.7, D_2 = 0.25, V_1 = 70 \text{ V}, V_2 = 70 \text{ V}$

As shown in Fig. 11, when the voltage of the second input source is set to 100 V, the peak current of inductor L_2 increases to 14.5 A. At the same time, it can be calculated that the power ratio of the second input source to the first input source becomes 2.15.

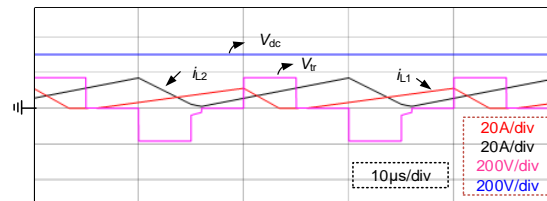


Fig. 11. Waveforms of $D_1 = 0.7, D_2 = 0.25, V_1 = 70 \text{ V}, V_2 = 100 \text{ V}$

As shown in Fig. 12, $V_1 = V_{1,\min} = 60 \text{ V}$ and $V_2 = V_{2,\min} = 110 \text{ V}$. The voltage waveforms of the primary side, DC-link of the transformer and the current waveform of the boost inductor are given. The peak current of inductor L_2 increases to 17.5 A, the peak current of inductor L_1 decreases to 7 A, and the calculated power ratio changes to 3.75. Above all, we can clearly see the difference between the power provided by different input sources.

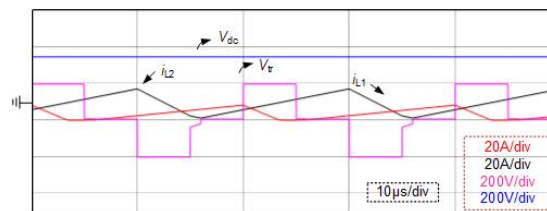


Fig. 12. Waveforms of $D_1 = 0.7, D_2 = 0.25, V_1 = 60 \text{ V}, V_2 = 110 \text{ V}$

5.2. Experimental verification

In order to verify the correctness of theoretical analysis and the feasibility of the proposed converter, we built a semi physical experiment platform as shown in Fig. 13. The real-time simulator forms a closed loop with the DUT through I/O signal or communication to test the

weak current control board (usually the DSP board), which is also called the simulation test of Hardware-In-the-Loop (HIL). The upper computer is on the left, the white box in the middle is Starsim HIL and the oscilloscope is on the right.

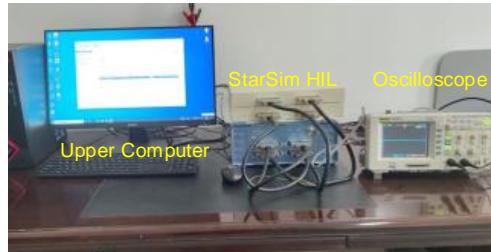


Fig. 13. Semi physical experiment platform

This paper mainly considers two different duty ratios. Figure 14 shows the experimental waveforms of the switch pulse with duty ratios $D_1 = 0.7$, $D_2 = 0.25$.

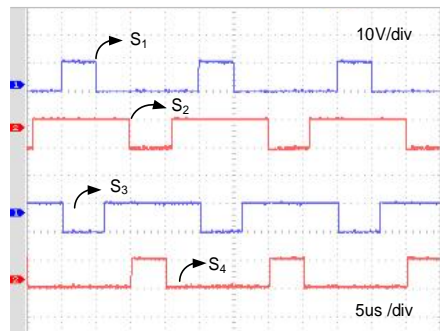


Fig. 14. Experimental waveforms of gate signals when $D_1 = 0.7$, $D_2 = 0.25$

The first set of experimental parameters is as follows: $L_1 = L_2 = 87 \mu\text{H}$, $V_1 = V_2 = 70 \text{ V}$, $D_1 = 0.6$, $D_2 = 0.35$, $f_s = 50 \text{ kHz}$, $C_1 = C_2 = 470 \mu\text{F}$, $C_0 = 220 \mu\text{F}$, $L_0 = 220 \mu\text{H}$. Figure 15 shows the waveforms of boost inductance current.

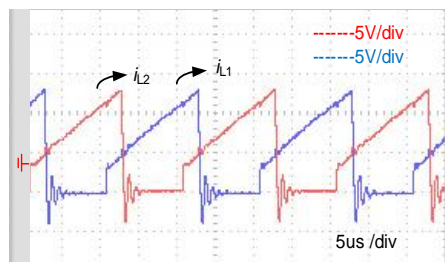


Fig. 15. Experimental waveforms of transformer primary side boost inductor current

As shown in Fig. 15, the two input source voltages are set to 70 V. It can be seen that the two boost inductors provide the same peak current 9.5 A and equally share the required power of the load. Additionally, the experimental value is slightly smaller than the theoretical value. The reason may be that the software simulation environment is ideal and the actual conduction loss of the inductor is not considered.

Figure 16 shows the experimental waveforms of boost inductance current. It can be seen that different switching modes of the light switch will cause the primary side of the transformer to bear three levels: $V_{dc}/2$, $-V_{dc}/2$ and zero.

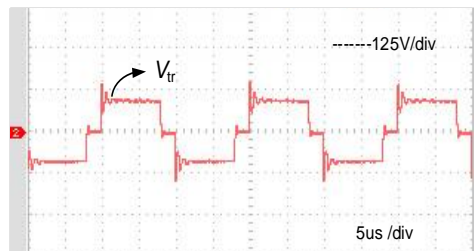


Fig. 16. Experimental waveform of transformer primary side voltage

The second set of experimental parameters is as follows: $L_1 = L_2 = 87 \mu\text{H}$, $V_1 = 70 \text{ V}$, $V_2 = 90 \text{ V}$, $D_1 = 0.7$, $D_2 = 0.25$, $f_s = 50 \text{ kHz}$, $C_1 = C_2 = 470 \mu\text{F}$, $C_0 = 220 \mu\text{F}$, $L_0 = 200 \mu\text{H}$. Figure 17 shows the waveforms of boost inductance current.

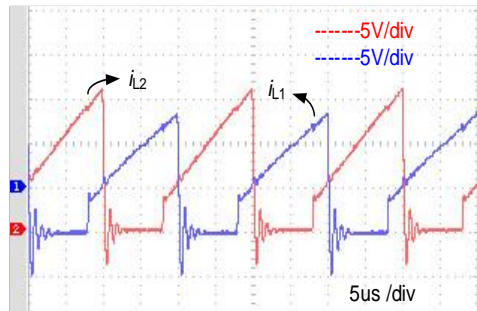


Fig. 17. Experimental waveforms of transformer primary side boost inductor current

As shown in Fig. 17, when the second input source voltage is set as 90 V, the peak current of inductor L_2 increases to 12.5 A. The voltage value at the original side of the transformer also changes, as shown in Fig. 18.

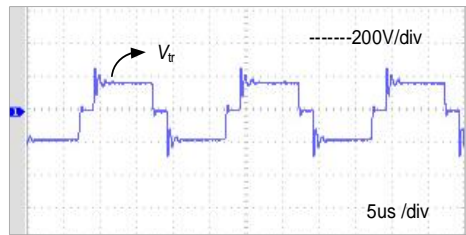


Fig. 18. Experimental waveform of transformer primary side voltage

6. Conclusion

In this study, a new multi-input DC/DC converter is proposed, which has the same number of active switches as the three-level isolated DC/DC converter, and does not need to introduce additional switching actions. The circuit analysis and design consideration have been provided in detail. With a proper selection of input inductors, autonomous load sharing can be achieved. To verify the operation of the converter, simulations of different parameters have been performed. A semi physical experiment platform has been built and tested under varying input voltages and duty cycles. The results prove the effective integrated operation of input sources with a three-level multi-input isolated DC/DC structure, by operating four switches in a phase-shifted manner without introducing control complexity. Compared with the MIC topology proposed in [14] and [20], the converter has the advantages of a simple structure, a small number of components, easy expansion, low voltage withstand value of the switch tube, and low cost of the interface circuit.

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