

On the design and linearization of transmitters for the LTE 450 base station

Dawid Rosołowski, Daniel Gryglewski, Wojciech Wojtasiak, Michał Kajczuk, and Jędrzej Klocek

Abstract—The paper presents the two transmitter analog paths of 10 W and 400 W peak output power developed for micro- and macro-cell LTE450 base stations, respectively. Each path contains a chain of amplifiers with a final stage designed in the Doherty architecture to improve total transmitter power efficiency. The paths were optimized for linearity and efficiency considering, i.e., an output power vs. input power course shape and tuning of the amplifier's operating points while using low computational complexity MP algorithms.

Keywords—LTE450 transmitter, Doherty amplifier, transmitter linearization, digital predistortion DPD, power efficiency in 4G @ 5G systems

I. INTRODUCTION

TODAY, the transmitters operated in the new wireless communication systems, such as 5G and beyond, must feature low power consumption and satisfactory linearity. The high power efficiency implies increased working time between charges for mobile devices and less heat management problems in the case of stationary hardware. Thus, the reliability of the radio system can be enhanced, thereby extending its lifetime. According to estimates, electricity consumption accounts for 15% to 40% of all costs incurred by telecom providers and over 70 % of the energy in a cellular network is used by the radio access network (RAN) [1]. Considering the above, it is clear that the costs of maintaining a radio infrastructure can be reduced through the rise in power efficiency.

It can be stated in a simplified way that a modern Radio Access Network (RAN) transmitter contains SDR-based components and high-efficiency power amplifiers linearized with the Digital Predistortion (DPD) technique. Unfortunately, there are no off-the-shelf comprehensive solutions that would fully meet the needs of providers. As a result, the telecoms that want to use new frequencies released from the regulator's resources must still customize their infrastructures or commission the development of dedicated radio infrastructures. This applies to both the hardware and processing layers. Therefore, the SDR is a convenient base for rapidly implementing new radio systems like private networks.

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Dawid Rosołowski (), Daniel Gryglewski () and Wojciech Wojtasiak () are with Warsaw University of Technology, Poland (e-mail: {dawid.rosolowski; daniel.gryglewski; wojciech.wojtasiak} @pw.edu.pl).

Michał Kajczuk and Jędrzej Klocek are with IT Partners Telco Sp. z o.o., Poland (e-mail: Michał.Kajczuk@itpartners.com.pl, jklocek@vergewave.com).

Although the effectiveness of digital linearization does not depend on the frequency of the transmission band, the performance of power amplifiers is the main obstacle in universalizing the transmitter platform.

The linearization algorithm choice is usually determined by the bandwidth and nature of the transmitter's nonlinearity or the platform's computational (processing) capabilities. These algorithms are available in terms of ready-made routines as IP cores or built into just a few transceivers.

On the other hand, a custom approach to the linearization issue involves developing its own or implementing a selected algorithm using the most common techniques: Memory Polynomial, Look-up Table, or Neural Networks (NN) [2][3][4].

Adding DPD algorithms to existing baseband radio processing routines (e.g., Digital Up Converter, Digital Down Converters, etc.) implemented most often at the FPGA level requires considering available logic resources. In turn, the power amplifier specific to a radio system should be designed to meet the desired efficiency and linearity at a given output power within the range of frequency needed. To achieve transmitter efficiency, Doherty amplifiers are often used, and waveform peaks are shaped accordingly by Crest Factor Reduction algorithms preceding DPD processing.

The authors' works on the custom of radio devices have resulted in the development of the Universal Hardware Platform (UHP) [5][6], which allows for the commonality of a large part of hardware resources. Custom hardware operating over a 300 MHz to 6 GHz frequency range can be carried out using this platform, provided the software and high-power amplifier are replaced.

This paper presents the design results of two linearized transmitters using our platform for a prototype LTE450 base station. The question may arise: why LTE and not 5G? The answer may be as follows. Though 5G promises groundbreaking advancements, deploying it in the 450 MHz band faces significant challenges. LTE seems to be a more suitable option due to its prevalence, compatibility, and efficiency. Moreover, the limited bandwidth of 5 MHz makes it unsuitable for benefiting from 5G's high data rates and low latency requirements. Support for the 450 MHz band was recently included in the 5G NR standard, so at the time of writing this article, utilizing this alternative was not yet possible.

Due to the scope of the paper, the focus is mainly on high-power amplifiers as the most crucial source of nonlinearities and DPD algorithms. The effect of a course shape of output power (Pout) vs. input power (Pin) in Doherty amplifiers on the efficacy of predistortion methods with a low computational



complexity was briefly discussed. To the authors' knowledge, consciously shaping the Pout(Pin) function for linearity-efficiency optimization is a novel approach.

The paper is organized as follows. In section II, the transmit platform of the LTE450 base station is briefly outlined. Section III presents two transmitter analog paths with amplifiers of a 10 W and 400 W peak power explicitly designed for the LTE450 base station. In Section IV, it was explained how the LTE450 transmitter path was linearized. The measured results of both linearized transmitters are shown in Section V. Finally, Section VI provides a brief conclusion.

II. TRANSMITTERS

A generalized block diagram of a transmitter hardware layer of the LTE450 base station is shown in Fig.1. Our Universal Hardware Platform (UHP) based on SDR technology was employed to develop the LTE450 base station. The transmitter analog path (TAP) was considered in the paper. However, the main emphasis was placed on power amplifiers, as marked in Fig. 1.

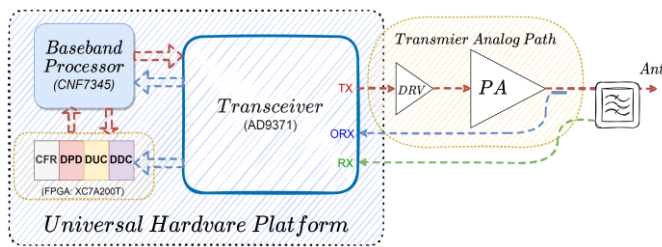


Fig. 1. Reconfigurable TX platform based on Universal Hardware Platform.

The signal processing in the transmit path begins from an integrated baseband processor Marvell SoC CNF7345, which delivers up to 8 LTE5-compliant components. Processing algorithms are implemented in the reconfigurable FPGA Xilinx (Artix7 XC7A200T) coprocessor. It provides functionalities such as interpolation, a shift to subcarriers, CF reduction, or intentional, controlled signal waveform distortion (part of the DPD procedure). The suitable baseband quadrature signal processed goes to the AD9371 Zero-IF transceiver (TRX). The AD9371 TRX includes dual channel transmitters (TX) and receivers (RX), as well as an observation receiver (ORX). All of them are integrated with effective 14-bit ADC/DAC converters and RF synthesizers.

The TRX AD9371 can be operated over a 300 MHz to 6 GHz frequency range with a synthesis bandwidth of 250 MHz and 100 MHz for TX and RX channels, respectively. A real band signal shifted to the target sub-band is received at TRX output. Due to the low power of the transceiver output signal, a custom amplifier needs to be used. The main task of the amplifier is to deliver a desired RF power level to an antenna, possibly with acceptable low level of distortion. Data acquired from the ORX are used to linearize the transmitter, i.e., to shape the signal at the TRX input in the digital domain so that the spectrum regrowth of the TRX output signal is acceptable. One of the main goals of designing a custom transmitter is to provide a trade-off between high-power efficiency and linearity suitable for a handled standard with a reasonable complexity of DPD and CFR calculations.

III. ANALOG PATHS OF THE TWO TRANSMITTERS

In the frame of design works, two analog transmit paths with different output power levels were developed for the LTE 450 base station. The task of both sub-systems is to amplify the transceiver output signal of -7 dBm peak power to 40 dBm in the first case and 56 dBm in the second one.

The choice between LTE 450 MHz base stations with 400 W and 10 W peak power depends on the specific needs of the deployment environment. For vast, sparsely populated areas, where coverage and signal strength are paramount, the 400 W Macro Cell transmitter is preferable. However, in dense urban or smaller-scale environments, e.g., in case of indoor or campus deployment scenarios, where the cell radius is significantly smaller, the 10 W Compact Micro Cell option might provide a more cost-effective solution.

The simplified block diagrams of the low- (10 W) and high-power (400 W) TAPs with a power balance and more crucial part numbers are depicted in Fig.2.

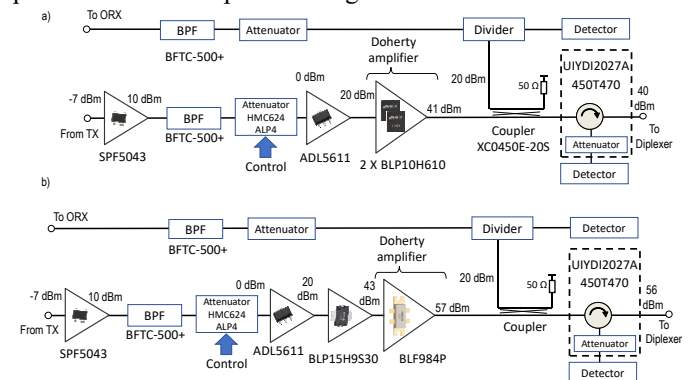


Fig. 2. Outline diagrams of analog blocks of 10 W (a) and 400 W (b) transmit paths.

It is known that the final amplifier in the TAP significantly contributes to lowering the transmitter's overall efficiency. Therefore, such amplifiers are designed in the highly efficient Doherty configuration, as depicted in Fig. 2. In contrast to conventional class B or AB amplifiers, the Doherty Amplifier (DA) achieves a higher power efficiency in a broader range of output power levels. This DA feature is beneficial, especially for radio systems with a high peak-to-average power ratio (PAPR), as in the case of LTE systems, where the PAPR exceeds 10 dB due to the OFDM modulation. However, compared to a class AB amplifier, the Doherty amplifier causes higher non-linear distortions that must be reduced significantly by the DPD processing.

Owing to the expected manufacturing of the LTE450 base station, the main components for both paths were selected based on a trade-off between performance, cost, and product availability currently and in the future. As shown in Fig. 2a, the 10 W transmit path comprises three amplifiers, i.e., preamplifier, driver, and the final stage in the Doherty configuration. The preamplifier is Qorvo's low-cost GaAs pHEMT MMIC SPF5043 with the on-chip active bias circuits. To provide a high linearity of this stage work, its maximal output power should be 10 dB lower than the output power of 20 dBm at the 1 dB gain compression point for CW mode. The bandpass filter BFTC-500+ by MiniCircuits limits the band of input stages while eliminating the out-of-band distortions, particularly those that occur far from the transmitter band.

A 6-bit digital attenuator HMC624A (AD) with a 31.5 dB attenuation control range in 0.5 dB steps is employed to adjust the output power and gain of the transmit path. It is also a feedback loop element to compensate for temperature effects. The HMC624A integrates two dies, a GaAs RF attenuator, and a CMOS driver into one package. Thus, this MMIC is convenient for users because it can be easily controlled using a series or parallel interface through the CMOS driver. The low-cost MMIC amplifier AD5611 was chosen as a driver stage, which achieves nearly 21 dBm of output power at the 1 dB compression point and more than 22 dB gain. The AD5611 is supplied with only a single DC voltage of 5 V due to an internal bias circuit. A final stage was designed in the Doherty architecture using two of the same Si LDMOSFETs BLP10H610 by Ampleon. The DA was simulated with Keysight software ADS and the BLP10H610 non-linear model delivered by Ampleon. A simplified schematic of the DA with two FETs BLP10H610 is depicted in Fig. 3.

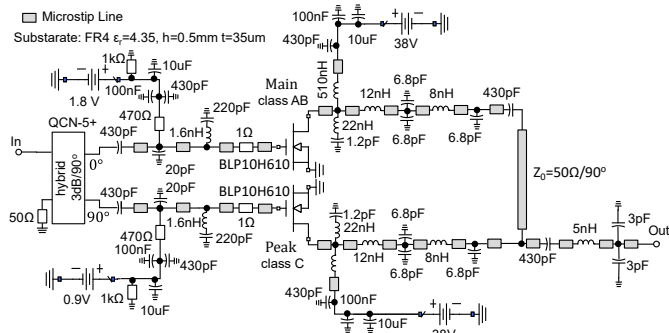


Fig. 3. Simplified schematic of the 10W Doherty amplifier with two LDMOSFETs BLP10H610.

The lower-power Doherty amplifier for the CW signal at saturation reached more than 40 dBm output power with a 20 dB gain. The transistor operating points of the Main and Peaking stages were optimized to obtain the best possible effect of the DPD algorithm. A coupler XC0450E-20S (Anaren) at the DA output provides a feedback signal to the observation receiver (ORX) and the output power monitoring system. The feedback signal taken from the transmitter's output is necessary for the DPD processing by containing information about the current regrowth of the spectrum. A circulator UIYDI2027A450T47 (UIY) is the final component of the transmit path. The circulator protects the power amplifier and enables the reflected signal to be measured to control the TAP load.

As shown in Fig. 2, a 400 W transmit path contains four amplifiers. The first two stages, the bandpass filter and the digital attenuator, are the same as those in the low-power TX path. To drive a final amplifier, another stage needed to be added. The driver designed using the LDMOSFET BLP15H9S30 by Ampleon provides an output power of more than 43 dBm with a 23 dB gain. A final amplifier was built in the Doherty configuration using Ampleon's transistor BLF984P, which includes two of the same LDMOSFET chips closed into one package.

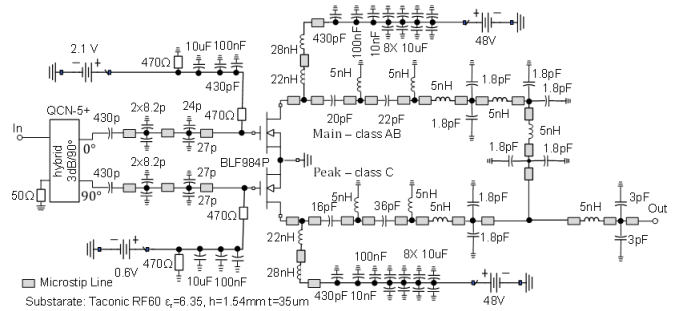


Fig. 4. Simplified schematic of the 400W Doherty amplifier with the LDMOSFET BLF984P.

As in the previous case, the DA was developed in the ADS environment using the BLF984P model provided by the manufacturer. The 400 W DA simplified schematic is depicted in Fig. 4. The DA achieves more than 57 dBm of output power at a gain of 14 dB under pulsed mode. The following component is a coupler, which delivers the feedback signal to the ORX and is further processed by the DPD and the output power monitoring system. Due to the high RF power, it was necessary to design a microstrip coupler directly on the PCB. The rest of the elements are identical to the low-power TAP. The only difference is that the 400 W TAP design was adapted to handle significantly higher power. The photos of the analog part of both paths are shown in Fig. 5.

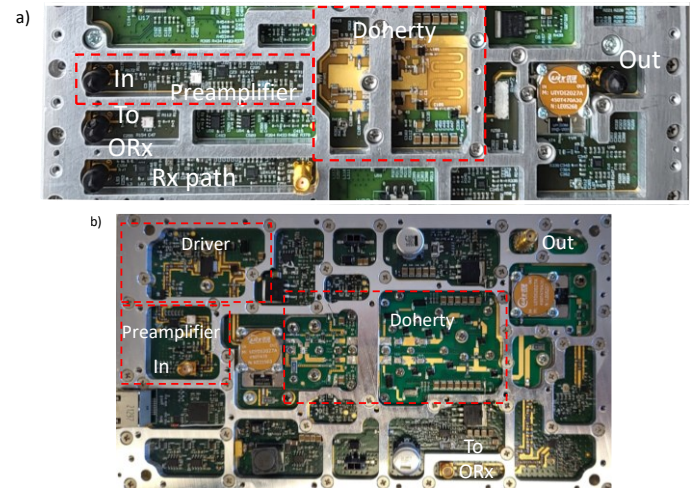


Fig. 5. View of the 10 W and 400 W TAPs, (a) and (b), respectively.

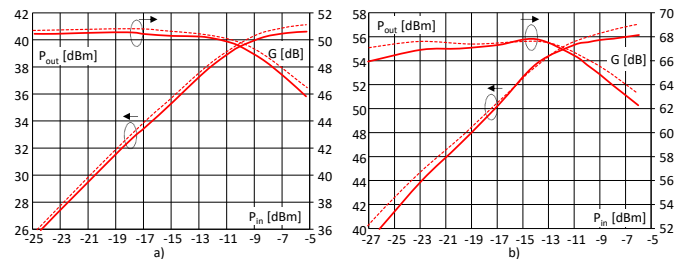


Fig. 6. Measured and simulated gain (G) and output power (P_{out}) vs. the input power level (P_{in}) for the 10 W (a) – and 400 W (b) TAPs, red-line measurements, red dotted line – simulations.

Both paths' measurements as a function of the input and output power level were performed for the frequency $f = 465$ MHz under pulsed mode for the 10 μ s pulse duration and 20 %

duty cycle. The measured and simulated gain $G(P_{in})$ and output power $P_{out}(P_{in})$ for the 10 W and 400 W TAPs are plotted in Fig. 6a and b, respectively. However, the power-added efficiency PAE(P_{out}) of the low- and high-power paths is shown in Fig. 7a and b, respectively.

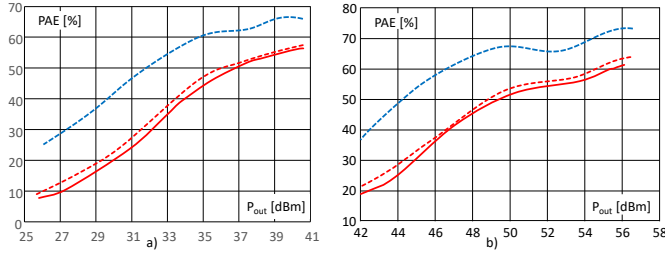


Fig. 7. Measured and simulated added-power efficiency (PAE) as a function of the output power level for the low-(a) and high-power (b) TAPs, red-line measurements, red dotted line – simulations, blue dotted line – measured PAE of the Doherty amplifier.

The high agreement between the results of measurements and simulations in Fig. 6 and 7 is worth noting. The waveforms in Fig. 6 and 7 are typical for the transmit analog path, with the final stage in the Doherty architecture [7]. The Doherty region specified by back-off and compression points can be seen in the efficiency characteristics in Fig. 7. The back-off is the output power level for the first maximum in the course of efficiency as a function of output power. An ideal two-stage DA exhibits two of the same maxima [8],[9]. The first corresponds to a back-off level of -6 dB, i.e., 6 dB below the output power level at saturation. The second is determined by the output power level at saturation, such as for class AB amplifiers.

The Doherty region is crucial for both the transmit path's linearization and the overall power efficiency of the transmitter. Therefore, the DA structure is often optimized during the design to obtain the desired back-off level. For both DAs, the back-off level was approximately equal to the average power specified for a given version of the LTE450 system. The back-off level was -7 dB and -8 dB for the 10 W and 400 W Doherty amplifiers, respectively. In the Doherty region, the gain of the low-power transmit path drops from 50 dB to 46 dB while the output power increases from 38 dBm to 40.7 dBm. Hence, the conclusion is that the 40.7 dBm output power corresponds to a 3 dB compression point, i.e., $P_{3dB} = 40.7$ dBm.

In the case of the high-power TAP, a gain decreases from 67 dB to 62 dB for the output power ranging from 54.5 dBm to 56.2 dBm. Thus, the DA features lower compression at the c.a. 2 dB. A power-added efficiency of 10 W TAP is from 40 % to 58 % over the 34 dBm to 40.7 dBm output power range. Meanwhile, 400 W TAP features a PAE of 45% for the -8 dB back-off and 61 % at a saturation of 56 dBm. Both TAPs were driven by a pulsed CW signal, as mentioned before. A PAE drop of 10 percentage points of the 10 W TAP compared to the individual DA efficiency is seen. An even more significant drop in efficiency is observed for 400 W TAP. Compared to the single 400 W DA, the difference in efficiency varies from 20 to 10 percentage points at the output power ranging from 48 dBm to 56 dBm. Hence, the contribution of the other components to total efficiency is not tiny at all. Thus, the power consumption of the other TAP components should be minimized.

Reducing the power consumption by improving the efficiency of Doherty amplifiers for a wider range of output

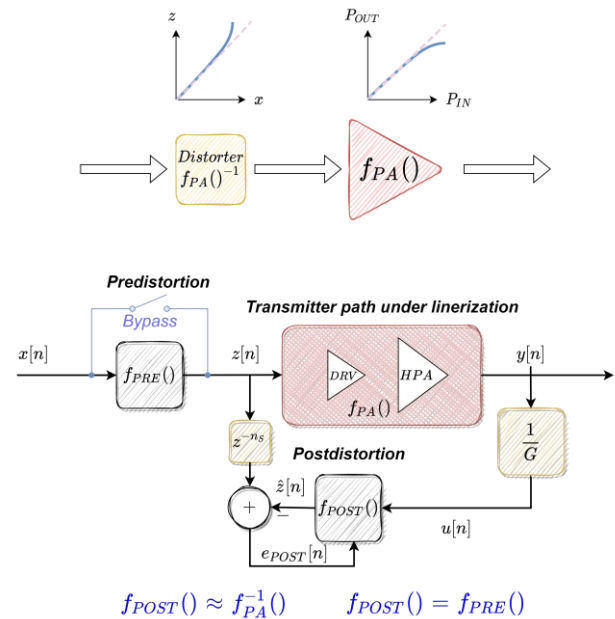
power is usually associated with a degradation of the linearity of the $P_{out}(P_{in})$ function. The back-off level lowers, and this function inflection appears. A polynomial modeling of the $P_{out}(P_{in})$ function with inflection for DPD requires increasing the number of coefficients. Raising the polynomial degree causes a rise in computational complexity. As a result, the numerical conditions of the model extraction deteriorate, and already, for the 5-th or 7-th power of the polynomial, the end of improving the linearity assessed by spectrum regrowth exhibits.

Typical linearization algorithms are efficient around a compression point. However, more is needed in the Doherty amplifier case. The DA $P_{out}(P_{in})$ course has at least two inflections - a first as the Peaking amplifier turns on and a second in the compression region. A linearization algorithm should consider both inflection points. The customary use of Volterra's polynomials in different versions offers limited options to model nonlinearities and predistortion. Hence, the classical approach, e.g., with MP, is a conscious compromise between a linearization quality and power efficiency for an assumed back-off level.

It turned out that modifying the operating points of the Main and Peaking amplifier transistors in the DA may help achieve this compromise. Such a way of shaping the $P_{out}(P_{in})$ course is simple, but it can be done to a small extent and usually at the expense of efficiency.

IV. TRANSMITTER LINEARIZATION, DPD

In most cases, today's SDR-based transmitters already have built-in mechanisms to support the linearization. The hardware support involves spectrum monitoring, while the immanent software reconfiguration allows for extensive modification and the addition of new functionalities. Modeling and predistortion for the LTE450 system TX paths were developed using the Memory Polynomial (MP) [3][4]. The method is based on the simplified Volterra's memory polynomials and our implementation using Indirect Learning Architecture (ILA), as shown schematically in Fig. 8.



$$f_{POST}() \approx f_{PA}^{-1}() \quad f_{POST}() = f_{PRE}()$$

Fig. 8 The idea of linearization by predistortion and processing scheme in the Indirect Learning Architecture.

An amplifier inverse model can be expressed as follows:

$$\hat{z}(n) = \sum_{k=0}^K \sum_{m=0}^M a_{k,m} u(n-m) |u(n-m)|^{2k} \quad (1)$$

where:

- $x(n)$ – amplifier driving signal from baseband processor (lowpass equivalent)
- $z(n)$ – intentionally distorted signal $x[n]$
- $\hat{z}(n)$ – response of the transmission path inverse model
- $a_{k,m}$ – indexed model coefficient
- $u(n)$ – signal proportional to the output signal $y[n]$
- K, M – model parameters that mean the modeling polynomial degree and memory effect depth, respectively
- f_{POST}, f_{PRE} – functions describing postdistortion and predistortion, respectively (named after the place where the distortion is introduced)

The amplifier inverse model defined by f_{POST} simultaneously describes the predistortion function f_{PRE} for the ILA given with the following relationship:

$$z(n) = \sum_{k=0}^K \sum_{m=0}^M \hat{a}_{k,m} u(n-m) |x(n-m)|^{2k} \quad (2)$$

For the linearization architecture used, $\hat{a}_{k,m}$ coefficients of the inverse amplifier model are estimated based on the distorted input signal $z(n)$ and the TX path response $u(n)$. It is worth noting that these coefficients are simultaneously coefficients of the predistorter in the case of ILA.

Research on class AB amplifiers [4] reveal that modeling nonlinearities with shallow neural networks, including Real-Valued Time-Delay Neural Networks, yields a comparable quality of linearization assessed by spectrum expansion, like the description of nonlinearities with an explicit method using MP memory polynomials.

The predistortion model is much more computationally efficient after using easy-to-implement RELU-type activation functions. Furthermore, it isn't fraught with errors resulting from poor conditioning of the U-matrix and does not use the operator of multiplying numbers. However, a drawback is the time-consuming learning of the network to determine the model.

An advantage of polynomial methods is the capability of modeling nonlinearities by a system of linear equations, which significantly facilitates the calculation of coefficients and the DPD adaptation. The model parameters are recalculated on the fly when operating in the actual transmitter, accounting for dynamic changes in the signal and amplifier parameters over time.

In the solution proposed, during the algorithm initialization or when the coefficients are determined once, the predistortion module direct transfers the signal from the input to the output. The predistortion function f_{PRE} is bypassed, as shown in Fig 8. The model coefficients are calculated with, e.g., the least squares method (LSTSQ):

$$\mathbf{a}_0 = (\mathbf{U}^H \mathbf{U})^{-1} \mathbf{U}^H \mathbf{z} \quad (3)$$

where:

$$\mathbf{U} = \begin{bmatrix} u(n) & \dots & u(n-M) & \dots & u(n)|u(n)|^{0:2K} & \dots & u(n-M)|u(n-M)|^{0:2K} \\ \vdots & \ddots & \vdots & \ddots & \vdots & \ddots & \vdots \\ u(n-N) & \dots & u(n-N-M) & \dots & u(n)|u(n)|^{0:2K} & \dots & u(n-N-M)|u(n-N-M)|^{0:2K} \end{bmatrix}$$

$$\mathbf{z} = [z[n], z[n-1], \dots, z[n-N]]^T$$

The updating of the coefficients is carried out in the LMS adaptation process by equations 4 and 5.

$$\mathbf{a}_{i+1} = \mathbf{a}_i + \mu \delta \mathbf{a}_{i+1} \quad (4)$$

$$\delta \mathbf{a}_{i+1} = \mu (\mathbf{U}_{i+1}^H \mathbf{U}_{i+1})^{-1} \mathbf{U}_{i+1}^H \mathbf{e}_{i+1}, \quad \mathbf{e}_{i+1} = \mathbf{z}_{i+1} - \mathbf{U}_{i+1} \mathbf{a}_i \quad (5)$$

The μ parameter determines and shapes the adaptation stability and speed. The algorithm for effectively implementing DPD at the UHP software reconfigurable level is shown in Fig. 9.

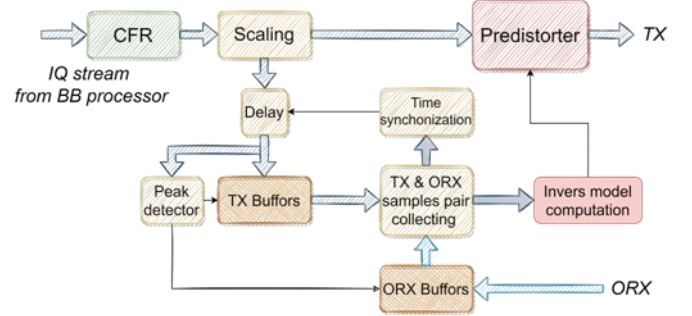


Fig. 9 DPD linearization algorithm in outline.

Some of the algorithms are implemented at the level of the actual FPGA chip (Xilinx Artix7 XC7A200T), and some at the level of the software coprocessor (uBlaze - a soft CPU implemented in the FPGA). The IQ stream processing starts with a CFR block execution implemented using the algorithm described in [10]. The next operation is to scale the signal to provide a few decibels spacing regarding the working range of the DAC. It enables the distorted signal in the predistorter to be fitted to the dynamics of the DAC built into TRX. The time synchronization of normalized ORX samples, representing the signal at the transmit path output, with intentionally transmitted TX samples, is carried out in two stages: coarse and precise, based on determining the maximum of the cross-correlation function. The samples generated in one of the polyphase interpolator branches were used to synchronize precisely. The DPD computational complexity was simplified by significantly decreasing the number of samples used to calculate the model parameters of nonlinearities similarly as described in [11]. Learning data comprises 2048 samples of continuous data and a set of samples collected around global peaks, the so-called bunch. Mechanisms to monitor the signal envelope level and buffer for the data need to be deployed to collect suitable pairs of samples ($tx[n]$ - excitation, $orx[n]$ - response) that meet the above criteria. The coefficients for the predistortion are determined in a process carried out at the coprocessor level after a gain normalization using samples from the ORX. The polynomial that models nonlinearities can be fitted to the transmit path nonlinearities by selecting proper values for its M and K parameters.

It should be noted that the MP method is typically used to linearize cases with moderate computational complexity and limited modeling options. The model coefficients are a solution to a redundant system of equations, usually solved with the mean-square minimization. However, the mean-square method requires a proper choice of representative training data to improve modeling quality. Experiments on effective selection for learning data were also performed when adjusting DPD procedures.

V. RESULTS

In the frame of the LTE 450 base station design, the 10 W and 400 W transmitters were developed. The photos of both transmitters are depicted in Fig. 5.

Tests of the transmitters were performed by the standard ETSI TS 136 141 [12] with the LTE FDD E-TM (E-UTRA Test Model) 1.1 reference signal for a 5 MHz channel width.

The peaks occurring in the test signal ($CF = 9.9$ dB @ $CCDF = 0.01$ %) were reduced with the procedure mentioned in Section IV. The computationally optimal ML model with parameters of $M=3$ and $K=3$, containing only odd powers, was determined based on the experimental study.

It should be noted that the best linearization results, particularly a spectrum regrowth improvement of about 1 dB in adjacent channels and c.a. 5 dB in channels 10 MHz apart, were achieved by a model with a maximum degree of polynomial equal to 7, also containing even powers. Results of linearity and efficiency measurements of both transmit paths are presented in the following subsections.

A. Compact Micro Cell Base Station Transmitter

The low-power transmitter of the LTE450 base station for mobile applications or temporary networks reaches close to 41 dBm peak power with a reduced peak to CF of 7.8 dB for $CCDF = 0.01$ %. The drain efficiency of the transmit path from the TRX output to the circulator output is 28 %.

The spectrum set of the highest power signal at the transmitter output is shown in Fig. 9. These spectra meet the requirements for spectral regrowth after linearization for various combinations of parameters $K=3$ and $M=2, 3$. For comparison, the spectrum (blue line) with DPD turned off also is depicted in Fig. 9.

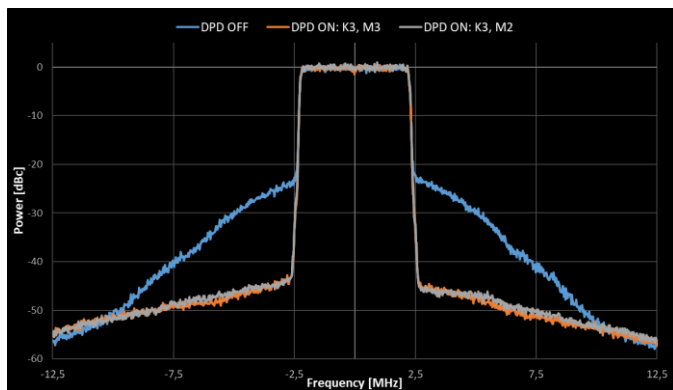


Fig. 9. Spectra at the transmitter output with DPD for the different parameters M, K and without DPD.

The measured performances of the 10 W transmitter, such as ACLR, EVM, drain efficiency for DPD model parameters $K=3$, $M=3$, and a few output power levels below the maximum value (Back-off), are given in Tab. I.

To comment on the results in Tab. I, it is worth referring to the ETSI EN 136 141 v12 p. 6.6.2 standard that imposes the following requirements for 5 MHz component:

- ACLR < -44.2 dBc
- EVM < 18.5 % for QPSK.

TABLE I

THE 10 W TRANSMITTER'S MEASURED PERFORMANCES: ACLR, EVM, AND DRAIN EFFICIENCY (H) FOR PEAK OUTPUT POWER LEVELS

$P_{PEAK@DPD_{ON}}$ [dBm] / Back-off [dB]	η [%]	ACLR_L [dBc] / DPD OFF / ON	ACLR_R [dBc] / DPD OFF / ON	EVM [%] / DPD OFF / ON
40.8 / 0	28	-29.0 / -46.4	-28.5 / -47.5	8.65 / 2.27
39.9 / -0.9	26	-29.2 / -47.3	-28.9 / -48.6	8.45 / 2.23
38.8 / -2	23	-29.6 / -46.1	-29.5 / -47.3	7.99 / 2.24
37.8 / -3	21	-30.3 / -45.7	-30.2 / -46.9	7.4 / 2.24
36.8 / -4	19	-31.4 / -45.6	-31.1 / -46.6	6.6 / 2.31
36.0 / -4.8	18	-32.6 / -46.0	-32.3 / -47.0	5.84 / 2.21
34.9 / -5.9	16	-34.4 / -48.2	-34.0 / -49.0	4.81 / 2.16
33.8 / -7	13	-36.4 / -51.8	-35.8 / -52.4	4.05 / 2.12

The measured ACLR and EVM parameters with DPD activated meet the above requirements for all output power levels from the -7 dB back-off point. ACLR exhibits a slight lack of symmetry c.a. 1 dB.

B. Macro Cell Base Station transmitter

The high-power transmitter is designed to build radio networks reaching a dozen kilometers. It provides close to 55 dBm of output power with a power efficiency of 37 % at the assumed spectral regrowth and permissible transmission errors for the LTE450 signal. The transmitter ACLR and EVM parameters measured for the average power below and at the compression point for reduced PAPR 7 dB are presented in Table II.

TABLE II

THE 400 W TRANSMITTER'S MEASURED PARAMETERS: ACLR, EVM, AND DRAIN EFFICIENCY (H) FOR PEAK OUTPUT POWER LEVELS

$P_{PEAK@DPD_{ON}}$ [dBm] / Back-off [dB]	η [%]	ACLR_L [dBc] / DPD OFF / ON	ACLR_R [dBc] / DPD OFF / ON	EVM [%] / DPD OFF / ON
54.9 / 0	35	-34.7 / -44.5	-30.4 / -45.6	5.26 / 2.54
53.9 / -1	34	-33.8 / -45.8	-29.9 / -45.6	5.73 / 2.49
52.7 / -2.2	29	-33.6 / -47.2	-30.1 / -46.6	5.91 / 2.35
51.4 / -3.5	26	-32.5 / -48.5	-30.0 / -47.4	6.22 / 2.26
50.1 / -4.8	22	-32.2 / -49.8	-30.1 / -48.3	6.41 / 2.29
48.9 / -6	20	-31.9 / -50.7	-29.8 / -50.7	6.51 / 2.15
47.8 / -7.1	18	-31.7 / -51.7	-30.2 / -50.4	6.49 / 2.12
46.6 / -8.3	15	-31.9 / -52.5	-30.6 / -51.2	6.30 / 2.08
45.3 / -9.6	14	-32.5 / -52.4	-31.1 / -51.4	5.94 / 2.11

Similarly, as in the previous case, the measured ACLR and EVM values with DPD-on were below the level required by the ETSI standard within the output power range from -9.6 dB to 0 dB back-off. The lack of symmetry in ACLR is also tiny and does not exceed 1 dB.

The output signal spectra of the 400 W transmitter for the output power of 0 dB back-off level (54.9 dBm) are shown in Fig. 10a and b, without and with DPD, respectively. The spectrum shown in Fig. 10b with DPD is met the spectrum mask requirement by ETSI standard.

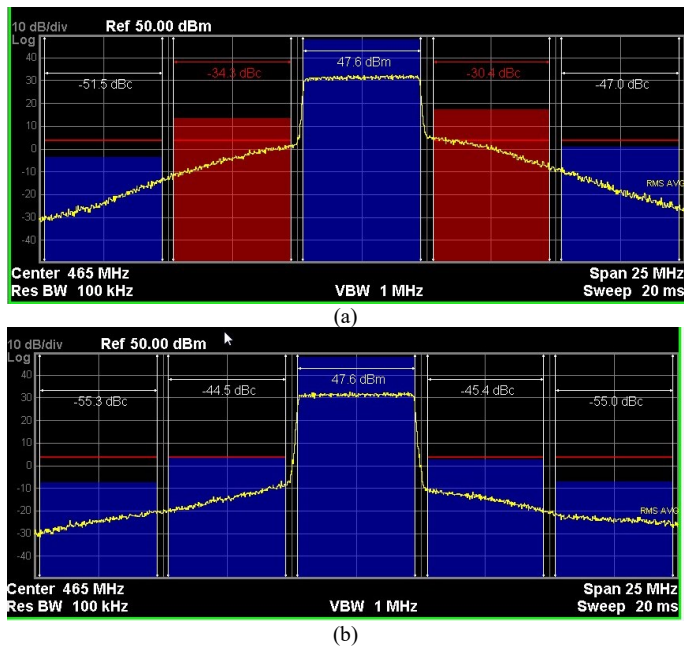


Fig. 10. Output signal spectra of the high-power transmitter without (a) and with DPD (b)

The operation of the DPD linearization can be seen in Fig. 10. ACLR was improved by more than 15 dB.

VI. CONCLUSIONS

The paper presents the 10 W and 400 W transmitter paths developed to adjust Universal Hardware Platform functionality for the LTE 450 system needs. The final amplifier in each path was designed in Doherty architecture to obtain high efficiency. The effect of the Pout(Pin) course shape of the Doherty amplifier on the DPD linearization process and the efficiency of the transmitter was considered briefly. The linearization process was based on the memory polynomial (MP) algorithm with depth-of-memory effect modeling at $M=3$ and the odd degree polynomial of 7. It enabled the trade-off between efficiency and linearity to be reached with a moderate implementation effort. Modifying the operating points of the Main and Peaking amplifier transistors in the DA helped achieve this compromise. The feasible linearization range of the amplifiers was approximately 4 dB higher than in the case of the off-the-shelf solution used in the AD9375.

To sum up, both transmitters met the requirements specified by ETSI EN 136 141 v12 p. 6.6.2 standard. The field tests of the LTE base station were performed successfully. The LTE450 system is currently being deployed into production.

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