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Nearest level control for improving total harmonic distortion in a 13-level three-phase multilevel inverter

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Abstract: This research investigates the application of nearest level control (NLC) in a three-phase transistor-clamped H-bridge (TCHB) multilevel inverter (MLI) to enhance power quality and reduce harmonic distortion. The TCHB topology offers high performance with fewer components compared to traditional MLI configurations, making it particularly suitable for renewable energy applications. By operating at fundamental switching frequency, the NLC technique effectively minimizes switching losses while reducing total harmonic distortion (THD). The study includes MATLAB/Simulink-based simulation modeling and experimental validation using dSPACE, tested under varying load conditions. For a 13-level TCHB inverter with equal DC supplies and a modulation index of $M = 1$, the voltage THD was 5.22% (resistive load) and 5.17% (inductive-resistive load) in simulations, which was further reduced to 4.5% and 4.2% in experiments. The NLC technique demonstrated superior harmonic performance and efficiency compared to conventional methods, particularly at higher voltage levels. This study highlights the practical advantages of the TCHB inverter, including reduced component count, simplified control implementation, and enhanced output waveform quality. These findings confirm the potential of the NLC-based TCHB inverter for high-performance motor drives and grid-tied renewable energy systems, positioning it as a promising solution for modern power electronics applications.

Key words: harmonic minimization, multilevel inverter, nearest level control, renewable energy, total harmonic distortion, TCHB MLI

1. Introduction

The expansion of renewable energy sources, electric cars, and industrial applications has led to a large increase in demand for power electronic systems with high power, high efficiency, and low harmonic distortion in recent years [1–5]. Multilevel inverters have emerged as a promising

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solution to address these demands by offering improved performance characteristics compared to conventional two-level inverters [6]. Multilevel inverters utilize multiple levels of DC voltage to synthesize an AC output waveform, thereby reducing harmonic distortion, minimizing voltage stress on power semiconductors, and enhancing system efficiency [7, 8]. This technology has attracted considerable interest from researchers and industry experts, resulting in the creation of several multilevel inverter structures and modulation techniques [9, 10].

Among the primary multilevel inverter topologies are the neutral-point-clamped (NPC), flying capacitor (FC), and cascaded H-bridge (CHB) inverters [11]. The NPC inverter, characterized by its ability to mitigate common-mode voltage issues and reduce switching losses, has found extensive application in medium to high-power grid-connected systems [12]. On the other hand, FC inverters, known for their simplicity and reduced component count, are often employed in low to medium-power applications such as renewable energy systems and motor drives [13]. Meanwhile, CHB inverters, with their scalability and fault-tolerance operation, are widely utilized in high-voltage applications including electric vehicles and high-power motor drives [14]. Additionally, emerging topologies like Transistor-Clamped H-Bridge (TCHB) offer further advancements in performance and flexibility. The TCHB topology, which combines carrier-based modulation with H-Bridge cells, improves harmonic performance and voltage quality, making it well-suited for high-power grid-connected applications [15].

Modulation techniques are essential for shaping the output waveform of multilevel inverters, significantly influencing their harmonic performance, and switching losses. Among these, pulse width modulation (PWM) is commonly employed, where the pulse width dictates the amplitude of the output voltage. PWM ensures precise control of the output voltage and effectively reduces harmonic distortion [16, 17]. Another advanced method, space vector pulse width modulation (SVPWM), optimally utilizes the available voltage vectors, resulting in reduced harmonic content and improved efficiency [18]. Selective harmonic elimination (SHE) aims to eliminate specific harmonics by solving nonlinear equations, offering superior harmonic performance at the expense of increased computational complexity [19, 20]. Techniques like nearest vector control (NVC) and nearest level control (NLC) are designed to mitigate specific harmonics by introducing notches in the output voltage waveform, thus enhancing harmonic suppression capabilities [21]. High switching frequency (HSF) modulation methods, including PWM and SVPWM, offer better harmonic performance but may incur higher switching losses due to increased switching frequency [22, 23]. Conversely, low switching frequency modulation techniques like SHE, NVC, and NLC can reduce switching losses but may lead to higher harmonic distortion [24]. Therefore, the selection of modulation technique and switching frequency depends on the specific requirements of the application, balancing harmonic performance and switching losses to achieve optimal system efficiency and reliability.

Harmonics are a critical factor influencing the performance and efficiency of power converters, particularly in multilevel inverter systems [25, 26]. The presence of harmonics in any electrical system poses significant risks, including overheating, losses, reduced performance, and shortened service life of electrical components. Therefore, minimizing harmonics is a critical objective to mitigate these issues effectively. Harmonics refer to the presence of frequency components that are integer multiples of the fundamental frequency, causing distortions in output voltage waveform. These harmonics can cause various detrimental effects, including increased losses, electromagnetic interference, and reduced system efficiency. total harmonic distortion (THD) is a quantitative measure used to assess the level of harmonic distortion in the output waveform relative to the fundamental frequency [27, 28]. In multilevel inverters, the presence of multiple voltage levels and switching states offers inherent advantages in mitigating harmonics compared to traditional two-level inverters. However, careful design and selection of modulation techniques are crucial to further minimize harmonic distortion and enhance system performance [29]. Additionally, advancements in control strategies and modulation techniques continue to play a significant role in improving harmonic performance and overall system efficiency in multilevel converter applications [30, 31].

This study focuses on the TCHB MLI, a topology that achieves high power quality with fewer electronic components compared to conventional MLIs. The key novelty lies in utilizing the NLC method to optimize THD reduction and switching loss minimization. Unlike traditional modulation techniques, NLC achieves a balance between efficiency and harmonic suppression without introducing computational complexity. Additionally, the symmetrical configuration of the TCHB inverter further enhances waveform quality, producing an output that closely approximates a sinusoidal waveform.

A comprehensive performance analysis is conducted, comparing the proposed method with existing literature to highlight its advantages in THD reduction and efficiency improvement. This research contributes to advancing power electronic systems by addressing key challenges in multilevel inverter modulation and renewable energy integration.

2. The TCHB inverter and its modulation

A three-phase 13-level TCHB MLI and its control technique (NLC) are modeled through simulation using MATLAB/Simulink.

2.1. Adopted 13-level TCHB MLI

The three-phase 13-level TCHB inverter configuration is shown in Fig. 1(a). This configuration consists of three identical TCHB cells, each powered by an equal DC voltage supply. As shown, the configuration employs fifteen switches and twelve diodes to produce a 13-level output voltage. Each TCHB cell operates with an input voltage of 60 V, while the DC-link capacitors have uniform capacitances of 2 200 μF. Table 1 summarizes the specification used for the simulation parameters for the TCHB MLI. The switching state of the TCHB inverter are given in Table 2, where active switches are on state of the switches during each level generation. By adding three cascaded TCHB cells (v_1, v_2, v_3), the 13-level output (v_{inv}) is formed as in Eq. (1).

$$v_{\text{inv}} = v_1 + v_2 + v_3. \tag{1}$$

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Figure 1(b) depicts the voltage output waveforms generated by cell-1, cell-2, and cell-3 for the 13-level inverter. The 13-level output of the TCHB inverter is achieved by combining the individual voltages of the three TCHB cells.

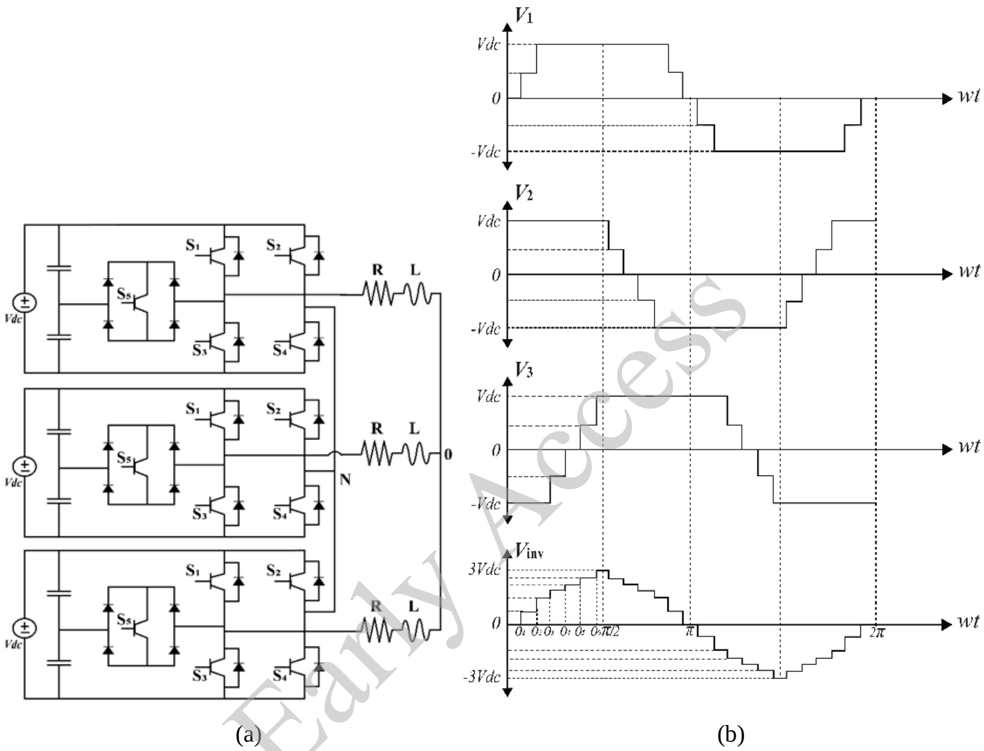

Fig. 1. Three-phase 13-level TCHB MLI: (a) circuit diagram; (b) output waveform generation

Table 1. Summarizes the specification used for the simulation parameters for the TCHB MLI

Parameters	**Values**
DC supply for cell-1, 2, 3	60 V
Load resistance	100 Ω
DC-link capacitor	2 200 µF
Load inductance	18.4 mH
Fundamental frequency	50 Hz

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2.2. Nearest level control technique

The application of the NLC technique for the 13-level TCHB inverter is depicted in Fig. **3**. The principle involves comparing the reference signal with the desired voltage levels. Initially, the output remains at zero until the first switching angle is reached. The output transitions to $0.5v_{dc}$ when the reference signal reaches or exceeds $0.25v_{dc}$ and maintains this level until the reference surpasses $0.75v_{dc}$. At this point, the output switches to v_{dc}. This process continues sequentially to achieve all desired output levels. With each step of the TCHB inverter corresponding to $0.5v_{dc}$, the maximum approximation error is limited to $0.25v_{dc}$, as illustrated in Fig 3(a).

The control logic of the NLC method for TCHB inverter is illustrated in Fig 3(b). The nearest voltage level can be obtained by:

$$v_{\mathrm{inv}} = 0.5v_{dc} * \mathrm{round}_{0.5}\left\{\frac{v^*}{0.5v_{dc}}\right\}. \tag{2}$$

The nearest round function is defined such that round$\{x\}$ is the integer closest to x. To resolve ambiguity for half-integers, the convention is that half-integers are always rounded to the nearest even number [32]. For example, round{1.4} = 1, round{1.5} = 2, round{1.6} = 2 as well and so on.

The switching angles for any number of levels using the NLC method are determined by the following equation:

$$\theta_i = \sin^{-1}\left(\frac{i-0.5}{x}\right), \tag{3}$$

where i = 1, 2..., $\frac{\boldsymbol{n-1}}{\boldsymbol{2}}$, n is the number of levels and $\boldsymbol{x} = \frac{\boldsymbol{n-1}}{\boldsymbol{2}}$.

As the number of levels increases, the switching angles θ_i become closer to each other, resulting in a waveform that closely approximates a sinusoidal shape.

For a symmetrical TCHB inverter, the modulation index M is calculated using:

$$M = \frac{V_{\mathrm{ref}}}{s*0.5v_{dc}}, \tag{4}$$

where $\boldsymbol{s}$ is the step number in a quarter wave, and $\boldsymbol{V}_{\mathbf{ref}}$ is the amplitude of the reference.

The waveform of the inverter's output voltage is depicted in Fig. 2, with the intervals for switch activation illustrated within the same figure. A single cycle of the TCHB output waveform is divided into six distinct regions, as detailed in Table 3.

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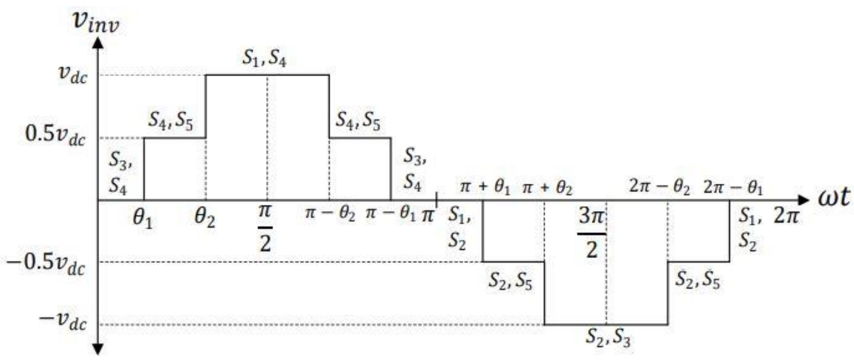

Fig. 2. Five-level TCHB inverter output voltage waveform

To avoid the risk of a short circuit fault across the DC voltage source, switches S_1 and S_3 or S_2 and S_4 (the switches within one leg of the H-bridge) should not be simultaneously activated.

The process of flow diagram of NLC technique is shown in Fig. 4. The flowchart illustrates the NLC technique for determining the output voltage (v_{inv}) of a multilevel inverter. The process begins by initializing the reference voltage (v^*) and the DC voltage step size ($0.5v_{dc}$). The system compares the reference voltage to predefined thresholds to select the appropriate output level. For instance, if v^* is less than $0.25v_{dc}$, the output is set to $0v_{dc}$, if it lies between $0.25v_{dc}$ and $0.75v_{dc}$, the output is $0.5v_{dc}$; and if it exceeds $0.75v_{dc}$, the output switches to v_{dc}.This comparison continues for all levels to minimize the error between v^* and v_{inv}. The iterative process ensures that the reference voltage is matched to the nearest voltage level, with the output voltage updated accordingly. The final output voltage is then applied to the inverter, ensuring efficient and accurate voltage control with minimal error.

Table 2. Switching state for proposed 13-level TCHB MLI

No. of level	**Active switches (on state)**	V_{inv}
1	$S_{11}, S_{14}, S_{21}, S_{24}, S_{31}, S_{34}$	$3V_{dc}$
2	$S_{11}, S_{14}, S_{21}, S_{24}, S_{34}, S_{35}$	$2.5V_{dc}$
3	$S_{11}, S_{14}, S_{24}, S_{25}, S_{34}, S_{35}$	$2V_{dc}$
4	$S_{14}, S_{15}, S_{24}, S_{25}, S_{34}, S_{35}$	$1.5V_{dc}$
5	$S_{14}, S_{15}, S_{24}, S_{25}, S_{33}, S_{34}$	V_{dc}
6	$S_{14}, S_{15}, S_{23}, S_{24}, S_{33}, S_{34}$	$0.5V_{dc}$
7	$S_{13}, S_{14}, S_{23}, S_{24}, S_{33}, S_{34}$ or $S_{11}, S_{12}, S_{21}, S_{22}, S_{31}, S_{32}$	0
8	$S_{12}, S_{15}, S_{21}, S_{22}, S_{31}, S_{32}$	$-0.5V_{dc}$

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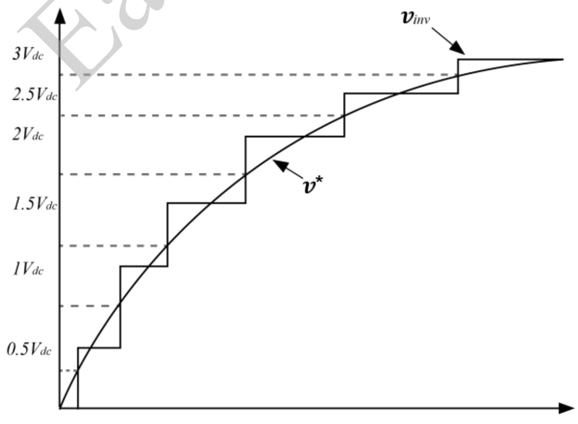
9	$\mathrm{S}_{12}, \mathrm{S}_{15}, \mathrm{S}_{22}, \mathrm{S}_{25}, \mathrm{S}_{31}, \mathrm{S}_{32}$	$-V_{dc}$
10	$\mathrm{S}_{12}, \mathrm{S}_{15}, \mathrm{S}_{22}, \mathrm{S}_{25}, \mathrm{S}_{32}, \mathrm{S}_{35}$	$-1.5V_{dc}$
11	$\mathrm{S}_{12}, \mathrm{S}_{13}, \mathrm{S}_{22}, \mathrm{S}_{25}, \mathrm{S}_{32}, \mathrm{S}_{35}$	$-2V_{dc}$
12	$\mathrm{S}_{12}, \mathrm{S}_{13}, \mathrm{S}_{22}, \mathrm{S}_{23}, \mathrm{S}_{32}, \mathrm{S}_{35}$	$-2.5V_{dc}$
13	$\mathrm{S}_{12}, \mathrm{S}_{13}, \mathrm{S}_{22}, \mathrm{S}_{23}, \mathrm{S}_{31}, \mathrm{S}_{33}$	$-3V_{dc}$

Table 3. Regions of one output cycle of the TCHB inverter

Region	**Interval**	**ON switches**	**Voltage level**
1	$0 \le \omega t \le \theta_1$ and $\pi - \theta_1 \le \omega t \le \pi$	$\mathrm{S}_1, \mathrm{S}_2$ (or $\mathrm{S}_3, \mathrm{S}_4$)	0
2	$\theta_1 \le \omega t \le$ and $\pi - \theta_2 \le \omega t \le \pi - \theta_1$	$\mathrm{S}_1, \mathrm{S}_4$	$+V_{dc}$
3	$\theta_2 \le \omega t \le \pi - \theta_2$	$\mathrm{S}_4, \mathrm{S}_5$	$+\frac{1}{2}V_{dc}$
4	$\pi \le \omega t \le \pi + \theta_1$ and $2\pi - \theta_1 \le \omega t \le 2\pi$	$\mathrm{S}_1, \mathrm{S}_2$ (or $\mathrm{S}_3, \mathrm{S}_4$)	0
5	$\pi + \theta_1 \ \ \omega t \le \pi + \theta_2$ and $2\pi - \theta_2 \le \omega t \le 2\pi - \theta_1$	$\mathrm{S}_2, \mathrm{S}_5$	$-\frac{1}{2}V_{dc}$
6	$\pi + \theta_2 \le \omega t \le 2\pi - \theta_2$	$\mathrm{S}_2, \mathrm{S}_3$	$-V_{dc}$



(a)

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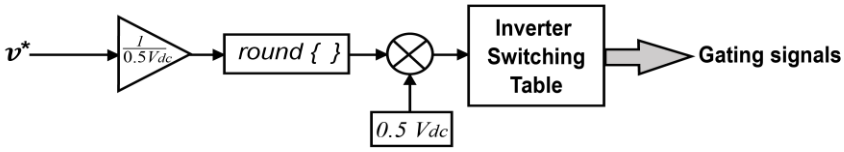

(b)

Fig. 3. NLC method (a) waveform synthesis and (b) control diagram

The primary advantage of the NLC technique lies in its simplicity in concept, easy implementation, and better efficiency. However, its main drawback is its reduced effectiveness when dealing with a smaller number of levels, as the approximation error becomes more significant [33].

3. Simulation and experimental results

This section provides simulation and experimental results for the 13-level TCHB multilevel inverter. It starts with simulation results using R loads and then extends to RL loads. Output results for simulation and experiments show the inverter phase voltage and phase current. The comparison between simulation and experimental findings is carried out to confirm the effectiveness of the proposed topology and its control strategy. Additionally, the selection of parameters such as DC supply voltage, inductance, and capacitance for both simulation and experimental setups is based on previous research on TCHB inverters [34], ensuring optimal performance. This approach simplifies the component selection process, leading to improved efficiency, stability, and harmonic reduction in the system.

3.1. Simulation results

This section presents the simulation results of a 13-level TCHB multilevel inverter. The model of this simulation was explained in the previous section 2. As mentioned earlier, all three TCHB cells are powered by 60 V DC supply, the gate pulse for the switches (S_1 to S_5) for all three TCHB cells are shown in Fig. 5.

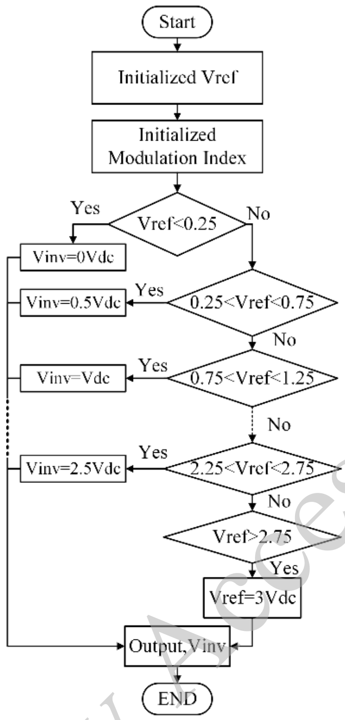

Fig. 4. NLC technique output generation flow diagram

For better understanding to make the calculation easier, the modulation index is considered as M = 1, so according to Eq. (4), it can be concluded ratio between the reference amplitude V_{ref} and sum of the DC voltage supply is equal to 1. The output voltage and current waveform of the inverter is shown in Fig. 6. Voltage and current THD at M = 1, using R load (R = 100 Ω) are illustrated in Fig. 7. The voltage and current THD of 5.22% was obtained from

the simulation using R load. The voltage and current THD is similar due to the use of R load, resistance alone does not affect the current waveform in terms of shape.

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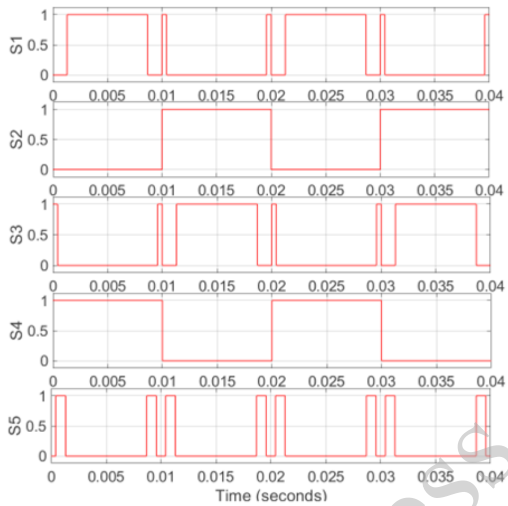

Fig. 5. Gate pulse for switches S_1 to S_5

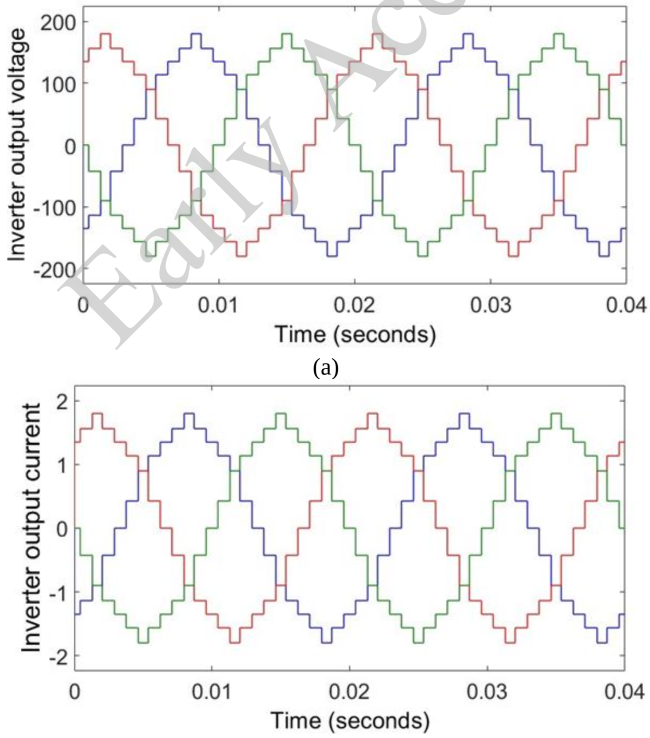

Fig. 6. Output waveform at M = 1, using R load: (a) voltage; (b) current

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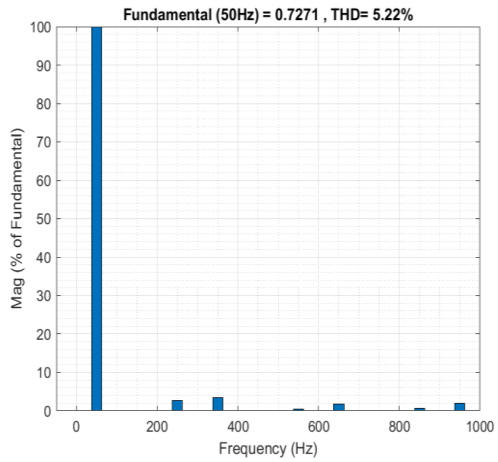
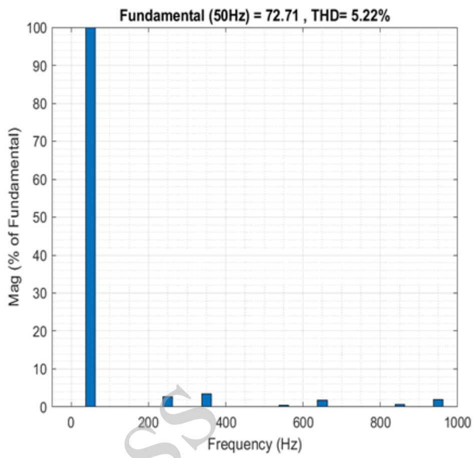
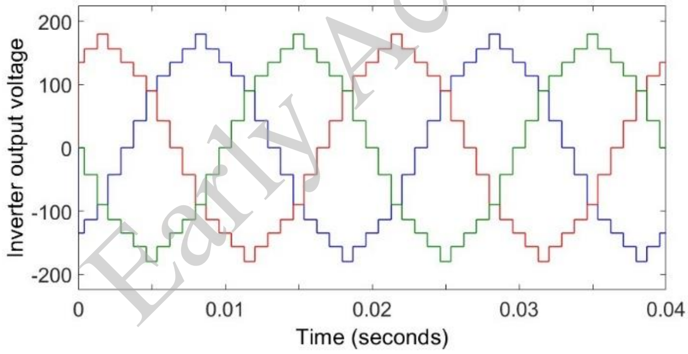


(a)

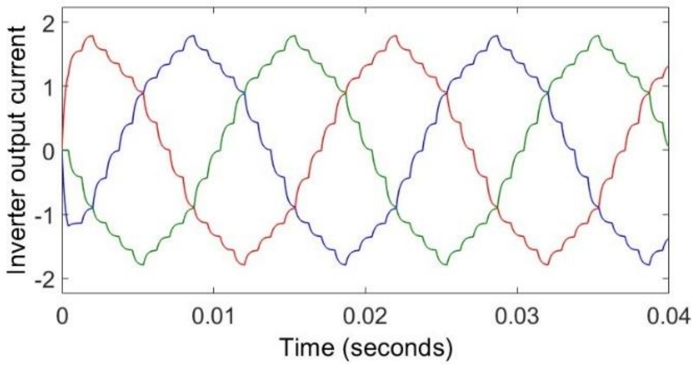


(b)

Fig. 7. Output THD at M = 1, using R load: (a) voltage; (b) current



(a)



(b)

Fig. 8. Output waveform at M = 1, using RL load: (a) voltage; (b) current

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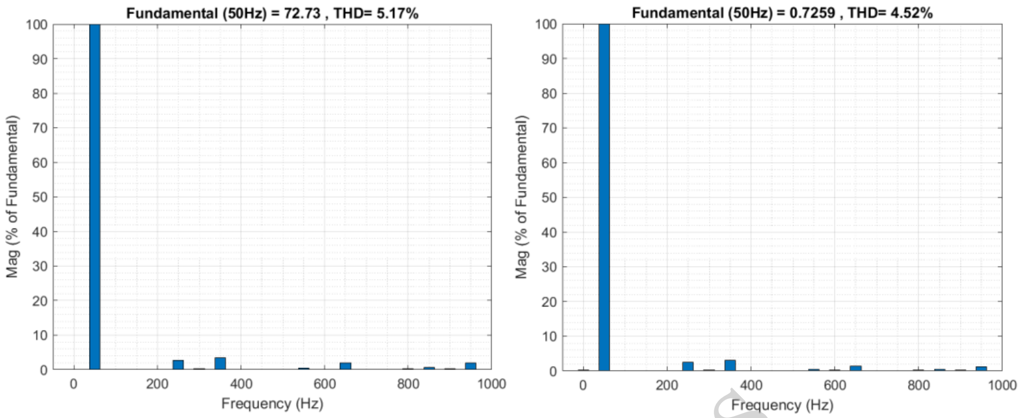

(a) (b)

Fig. 9. Output THD at M = 1, using RL load: (a) voltage and (b) current

The results are also tested using RL load (R = 100 Ω and L = 20 mH). As the RL load acts like a filter, it makes the output closer to the sinusoidal. Figure 8 presents the output voltage and current waveforms of the inverter, while Fig. 9 illustrates the voltage and current THD for M = 1. The voltage and current THD of 5.17% and 4.52% was obtained from the simulation using RL load. If a larger inductance is used, the current waveform becomes approximately sinusoidal.

3.2. Experimental results

This section presents the experimental results of the 13-level TCHB multilevel inverter. The output voltage and current waveforms are captured using a Tektronix TDS 2024C Oscilloscope, while a Fluke 435 power quality analyzer was employed to measure the voltage and current THDs as well as individual harmonic components. Results are examined using both R and RL load explained earlier. The experimental setup utilizes the dSPACE DS1003 real-time control platform, which is responsible for implementing the NLC technique for the inverter. It is programmed using MATLAB/Simulink and ControlDesk, enabling real-time tuning and monitoring of inverter performance.

Table 4 outlines the system parameters and components used in the experimental setup and hardware prototype. Figure 10 illustrates the experimental setup, highlighting the power supply, dSPACE, inverter circuit with gate drives, load and measuring instruments are shown.

The gate signals for the switches of cell-1 ($S_{11} - S_{51}$), cell-2 ($S_{12} - S_{52}$), and cell-3 ($S_{13} - S_{53}$) of the 13- level TCHB MLI are shown in Fig. 11(a) and 11(b). These gate signals are similar to the simulation results.

Figure 12(a) and 12(b) shows the voltage and current waveforms for 13-level TCHB multilevel inverter using R load at M = 1. Both voltage and current THD are 4.5% and 4.2%, as shown in Fig. 13(a) and 13(b), respectively.

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The results using RL load also verified using the experiment. Inverter output voltage and current waveforms shown in Fig. 14(a) and 14(b) respectively at M = 1. Both voltage and current THD are 4.2% and 3.4%, as can be seen in Fig. 15(a) and 15(b), respectively.

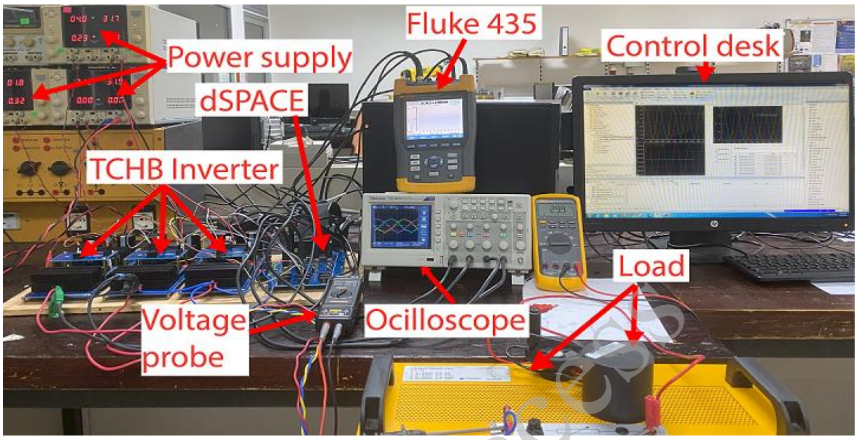

Fig. 10. Experimental setup of the system including inverter prototype

Table 4. System parameters and components used in the experimental setup

Parameters	Values
Number of cells	3
IGBT module	IRGP4062D
DC-link capacitor	2 200 µF
DC link diode	RURG8060
Fundamental frequency	50 Hz
Load resistance	100 Ω
Load inductance	18.4 mH
Dead band*	3 µSec

*(between the gate pulse of two IGBTs in the same leg)

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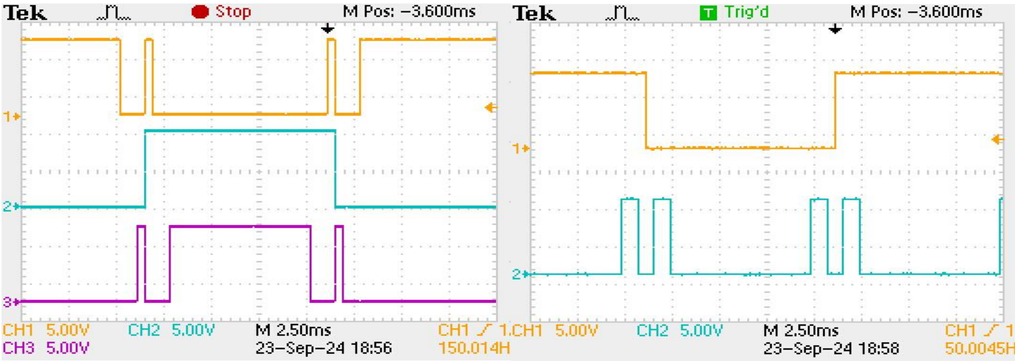
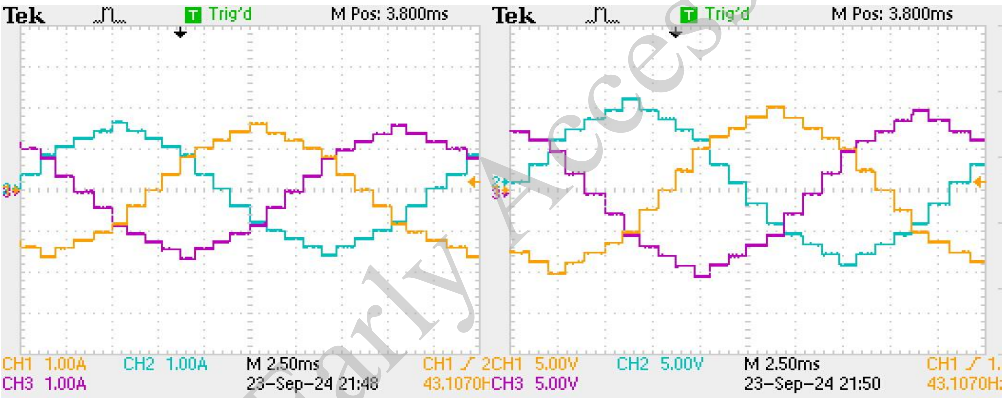


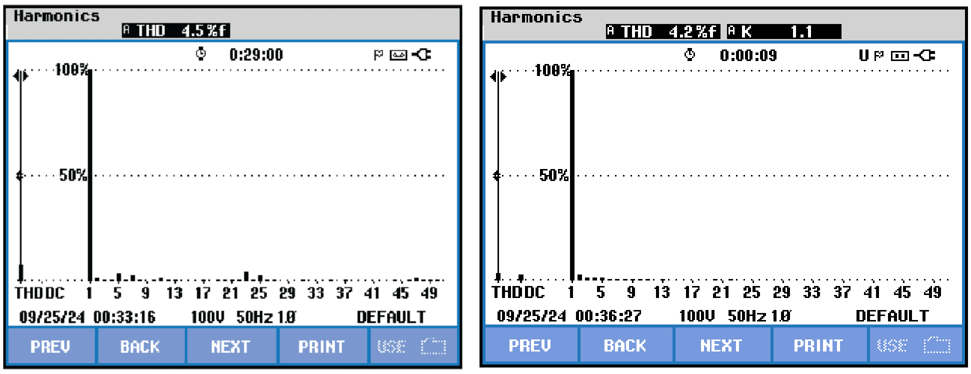
(a) (b)

Fig. 11. Gate signals for the IGBT switches: (a) switches S_1, S_2 and S_3, and (b) switches S_4 and S_5



(a) (b)

Fig. 12. Experimental results using R load at M = 1: (a) output voltage; (b) output current



(a) (b)

Fig. 13. Experimental results using R load at M = 1: (a) voltage THD; (b) current THD

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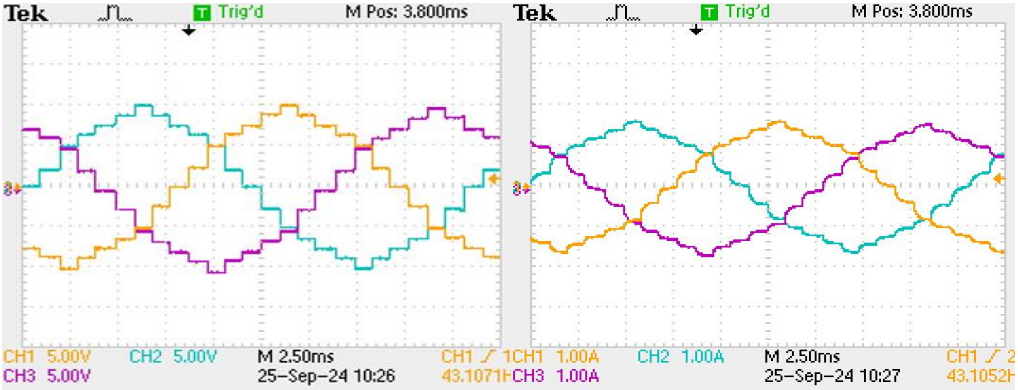
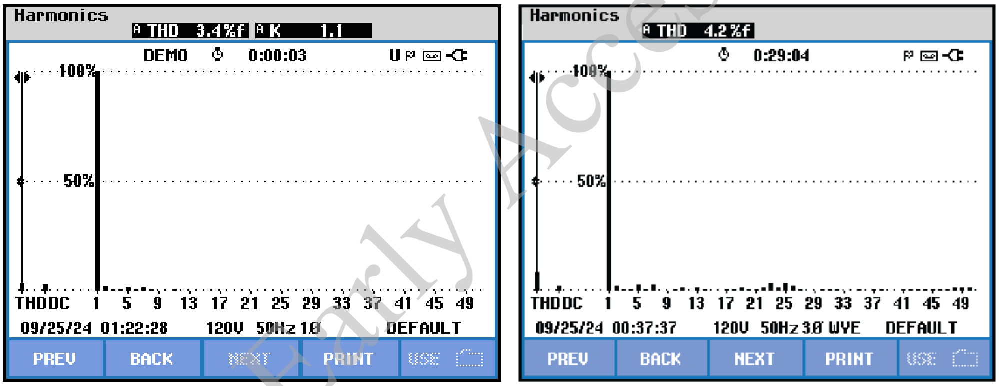


(a) (b)

Fig. 14. Experimental results using RL load at M = 1: (a) output voltage; (b) output current



(a) (b)

Fig. 15. Experimental results using R load at M = 1: (a) voltage THD; (b) current THD

4. Results and discussion

The results from simulation and experiments have been carried out using R and RL load. The voltage and current THD from both simulation and experiments are very close with a slight deviation. The voltage and current THDs from modeling and experimental results utilizing R and RL loads for various modulation indices are displayed in Table 5 and Fig. 16. THD was calculated up to the 20th harmonic order (N = 20) with a maximum frequency of 1000 Hz in both MATLAB simulation and experimental measurements using the Fluke 435 power analyzer. This ensures consistency between simulation and experiment while capturing all significant harmonics affecting power quality.

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For values of the modulation index M below 0.75, the output waveform reduces to a 9-level structure, resulting in a significant increase in THD. Similarly, when M exceeds 1.08, THD begins to rise again, even though the number of output levels remains unchanged. To present the most meaningful results and provide clarity on system performance, we have therefore focused on reporting the outcomes specifically for M = 0.75 and M = 1.08, excluding other values aside from M = 1.0. This allows for a clearer understanding of the critical behaviors within this operating range.

The THD from simulation using R load shows the same value, however in the experiments results it slightly different. As RL load acts as a filter, it makes the current waveform more sinusoidal and using RL load significantly improve the current THD. The simulation results are in good agreement with the experimental results in both loads conditions.

It can be seen that, unlike the voltage THD, current THD in experiments is lower than the that in simulation for both R and RL load. This slight occurs due to the measurement equipment's that is used, like current prove filters some current, thus reducing the THD in the experiments.

Table 5. Summary of the simulation and experimental results

Parameters		**THD (*v*)**			**THD (*i*)**		
Modulation index		0.75	1	1.08	0.75	1	1.08
R load	Simulation	10.07	5.22	6.79	10.08	5.22	6.97
	Experiment	10.6	4.5	6.8	10.3	4.2	6.6
RL load	Simulation	10.07	5.17	6.95	7.69	4.52	6.6
	Experiment	10.3	4.2	7.1	7.3	3.4	6.4

The comparison between simulation and experimental results shows strong consistency, affirming the effectiveness of the NLC method in minimizing harmonics for the chosen MLI topology. As demonstrated in the figures, THD increases when the modulation index is reduced, resulting in a lower number of output voltage levels. Similarly, when the modulation index exceeds its optimal value, the THD rises again, even though the system retains 13 output voltage levels. These findings reinforce the importance of selecting an appropriate modulation index for balancing THD reduction and maintaining adequate output levels in the inverter system.

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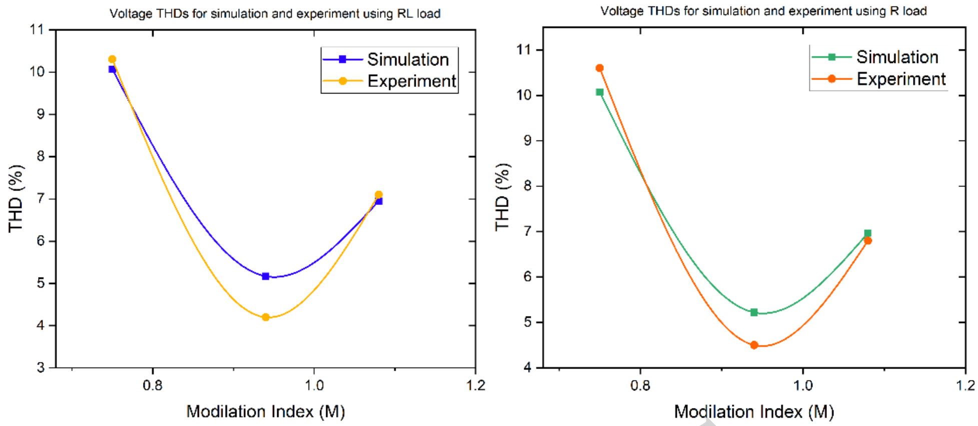

(a) (b)

Fig. 16. THD comparison of inverter for simulation and experiment using different modulation index: (a) using R load and (b) using RL load

Although this study focuses on the 13-level TCHB inverter, the principles of THD reduction and efficiency improvement using NLC are applicable to TCHB inverters with varying levels. Increasing the number of levels in a TCHB inverter generally leads to better waveform quality and lower harmonic distortion, making NLC a suitable modulation strategy for higher-level configurations (e.g., 17-level, 21-level). However, scaling up introduces challenges such as control complexity and increased switching components, which should be explored in future work.

4.1. Comparison with relevant literature studies

This research assesses the performance of the proposed NLC method implemented in a three-phase TCHB inverter compared to other methods existing in the literature. The comparison focuses on two main performance metrics, THD and the number of levels generated to demonstrate how the NLC method enhances system efficiency and power quality. Table 6 summarizes the benefits of NLC in achieving superior performance in THD reduction, efficient power quality. The NLC technique offers significant advantages over PWM, SVPWM, and SHE by achieving a THD of 4.73% while reducing switching losses by 30–50%, leading to improved efficiency and thermal performance [35]. Unlike high-frequency PWM and SVPWM, NLC operates at a lower switching frequency, minimizing stress on power semiconductor devices and extending hardware lifespan. Additionally, NLC eliminates the need for complex nonlinear equations required in SHE, simplifying implementation and reducing computational burden on controllers. Its scalability allows seamless integration into various multilevel inverter topologies, making it an optimal choice for high-power applications such as electric vehicles, industrial motor drives, and grid-connected renewable energy systems [36].

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4.2. Real world applications assesment

To assess the real-world applicability of the proposed inverter system for EVs, an urban drive cycle was employed to evaluate its performance. Figure 17 illustrates the drive cycle trajectory and the system's precise tracking of the reference, demonstrating the inverter's ability to respond dynamically to the fluctuating demands of an urban driving environment. This result underscores the system's suitability for real-world EV applications, validating its capacity for accurate speed and torque tracking, as required for efficient and reliable EV operation.

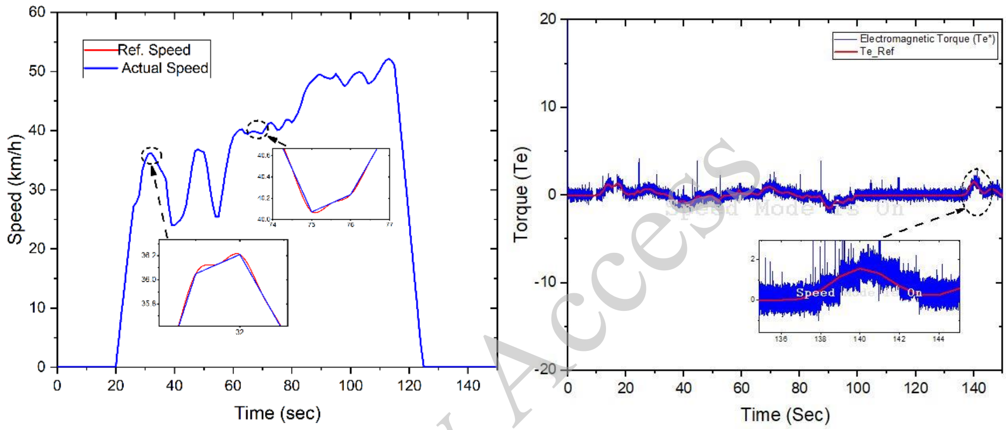

Fig. 17. Drive cycle trajectory and the system's precise tracking of the reference: (a) speed tracking; (b) torque tracking

5. Conclusion

In this research, the NLC technique was implemented in a three-phase TCHB multilevel inverter to minimize harmonic distortion. The TCHB inverter requires fewer components than traditional MLI topologies to achieve the same output levels, making it a cost-effective and efficient solution. The NLC technique is straightforward to implement, as it does not require complex calculations like SHE or NVC. Operating at fundamental switching frequency, it reduces switching losses while effectively lowering THD. Unlike other methods that target specific harmonics, NLC optimizes overall harmonic performance. The simulation model was developed using MATLAB/Simulink, and experimental validation was conducted via dSPACE under different load conditions. For the 13-level TCHB inverter with equal DC supply values at a modulation index of 1, the voltage THD was 5.22% (resistive load) and 5.17% (inductive-resistive load) in simulations, further reduced to 4.5% and 4.2% in experiments. These results demonstrate strong agreement between simulation and experimental findings, confirming the effectiveness of the proposed approach. Additionally, a comparative analysis with existing TCHB modulation techniques based on harmonic distortion showed that NLC outperforms traditional methods in THD reduction, particularly at higher voltage levels. This highlights NLC's potential for high-performance applications such as motor drives and grid-connected renewable energy systems.

Table 6. Summary of recent modulation technique applied to TCHB MLI

Modulation technique	Inverter type	THD (%)	Observations
SHE [37]	13-Level TCHB	6.77%	Effective in narrow range but THD increases outside narrow modulation range
CBPWM [25]	5-Level TCHB	29.17%	Higher THD compared to SVPWM, which offers better performance
SVPWM [25]	5-Level TCHB	13.12%	Improved THD reduction over CBPWM
PDPWM [38]	9-Level TCHB	9.3%	Achieved with 30 switches; moderately high THD
MPC [39]	13-Level TCHB	10.22%	Though it uses 15 switches for 13-level, it still has high voltage THD.
ANN-based modulation [40]	5-Level TCHB	14.48%	ANN technique provides lower THD content at output compared with PSO technique, but higher than NLC
NLC [36], [41], [42] (adopted method)	13-Level TCHB	4.73%	NLC maintains low THD across a wide modulation range, superior harmonic performance.

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