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Design of a nanoswitch in 130 nm CMOS technology for 2.4 GHz wireless terminals

M. ARIF SOBHAN BHUIYAN*, M. BIN IBNE REAZ, J. JALIL, and L. FARZANA RAHMAN

Department of Electrical, Electronic and Systems Engineering, Universiti Kebangsaan Malaysia, 43600 Bangi, Selangor, Malaysia

Abstract. This paper proposes a transmit/receive (T/R) nanoswitch in 130 nm CMOS technology for 2.4 GHz ISM band transceivers. It exhibits 1.03-dB insertion loss, 27.57-dB isolation and a power handling capacity ($P_{1\,dB}$) of 36.2-dBm. It dissipates only 6.87 μW power for 1.8/0 V control voltages and is capable of switching in 416.61 ps. Besides insertion loss and isolation of the nanoswitch is found to vary by 0.1 dB and 0.9 dB, respectively for a temperature change of 125°C. Only the transistor W/L optimization and resistive body floating technique is used for such lucrative performances. Besides absence of bulky inductors and capacitors in the schematic circuit help to attain the smallest chip area of 0.0071 mm^2 which is the lowest ever reported in this frequency band. Therefore, simplicity and low chip area of the circuit trim down the cost of fabrication without compromising the performance issue.

Key words: CMOS, ISM band, nanometer, transceiver, T/R switch, wireless.

1. Introduction

The increased popularity of 2.4 GHz ISM band devices for a different end user and corporate applications such as RFID, Bluetooth, Zigbee and Wi-Fi devices, non-contacting medical instruments, sensors etc., in the recent years, has raised the demand for small power and less off-chip components which tends to achieve integration of multiple transmitter/receiver chains on the same die [1–3]. As a result, highly integrated and area efficient designs are the current trends of IC design. The rapid advancement of CMOS technology is making the circuits operated at RF regime feasible nowadays [4–6]. Concurrent technologies allow the scientists to fabricate high performance RFICs in laboratories as well as for commercial applications. Researchers, all over the world, are working to further enhance the performances of RFICs by mitigating the CMOS problems at higher frequencies.

Transmit/Receive (T/R) switch is a fundamental device at every modern transceiver front-end which performs the task of linking a common antenna either to the receiver or to the transmitter depending on the control signal. At the time of transmission, there is a tie between the antenna and the transmitter which isolates the receiver that handles very small power. So the receiver remains safe from getting damaged. The opposite is true for reception period and the isolated transmitter helps to retain the low insertion loss at the receiver terminal. Figure 1 shows the basic building blocks of a typical wireless transceiver frond-end. The receiver front-end block receives signal from the antenna and send it to a low noise amplifier (LNA) to amplify the weak signal. Then it is made to pass through a down conversion mixer, a variable gain amplifier (VGA) and a low pass filter (LPF). The output signal from LPF is sent to an analog to digital converter (ADC) for processing. On the other hand, the transmitter block receives the processed signal from a digital to analog converter (DAC). Then it is filtered by a low pass filter and send for mixing at an up conversion mixer. Then it is again filtered by a band pass filter (BPF) and amplified by a power amplifier and radiated out through the antenna. The T/R switch handles both these high power and low power signal for efficient use of the antenna.

Many researchers all over the world are adopting many techniques such as optimizing gate width of the transistors, dc biasing of the transistors, impedance transformation method, parallel resonance, increasing the substrate impedance etc. to enhance their performances [7]. Yamamoto et al. (2001) demonstrated the basic consideration for improvement of performance of typical series-shunt type T/R switch by only optimizing the gate width of the transistors [8]. Therefore that design exhibited low isolation and low power handling capacity. Besides, due to the usage of large transistors, the size of the chip was large. To improve the performance, Huang (2001) adopted DC biasing technique along with optimization of transistor gate width in his design which resulted in low insertion loss along with moderate isolation and power handling capacity [9]. High control voltages (6.0/2.0 V) were used for switch and the size of the chip was also reduced to a half which is still large compared to present circuits.

In the year 2004, Huang (2004) and Hove et al. (2004), introduced impedance transformation and parasitic MOSFET model, respectively, to improve the isolation and insertion loss of the switch [10, 11]. But power handling capacity of both the circuits was poor and also they could not reduce the size of the switches. Yeh et al. (2006) utilized the resistive body floating technique to improve the overall performance of the switch but the $P_{1\,dB}$ and isolation of the switch was not adequate for high power transceivers. But they reduced the size drastically [12].

*e-mail: asobhan@eng.ukm.my

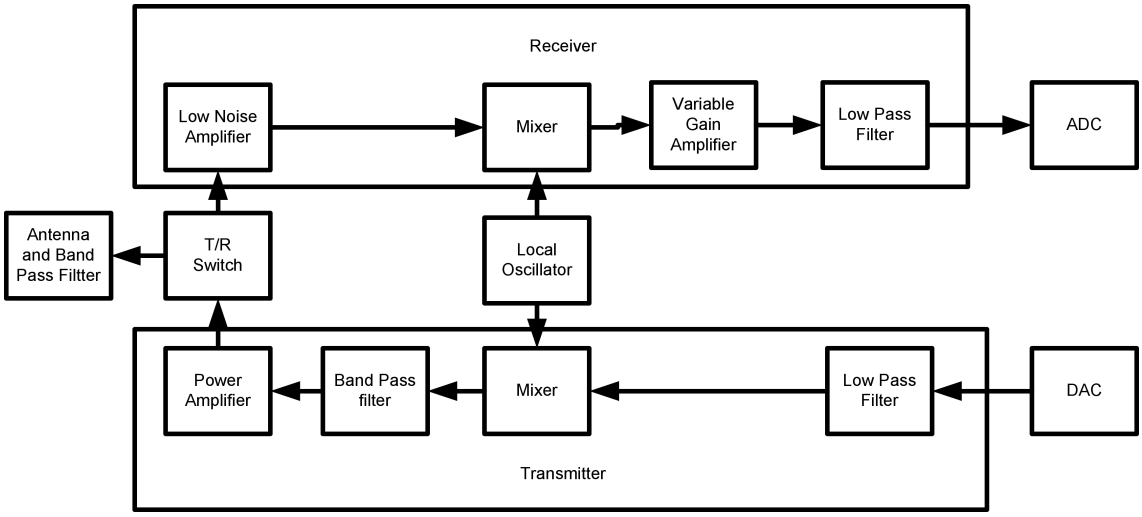

Fig. 1. Block diagram of analog front-end of a typical wireless transceiver

In this paper, resistive body floating technique and proper optimization of transistors are used to obtain high performance series-shunt T/R nanoswitch at 2.4 GHz ISM band in 130 nm CMOS technology. At the same time, avoiding the usage of bulky inductors and capacitors in the circuit resulted in achieving very small chip size. Such a switch will be very useful for 2.4 GHz ISM band RF transceivers.

2. Nanoswitch design methodology

The schematic circuit of the proposed nanoswitch in series-shunt topology is illustrated in Fig. 2. Complement control signals, Vc and Vc′, are applied at the gate terminals of the transistors ($M1$, $M2$, $M3$, $M4$, $M5$ and $M6$) to alternate their ON/OFF states. An inverter, consists of transistors ($M7$ and $M8$) along with the source VDD, does the task of inverting the control voltage. These control voltages are applied through gate resistances (R_{G1}-R_{G6}) to minimize the consequence of capacitive coupling around the gates of the OFF transistors [13]. The series transistors ($M1$ and $M2$) execute the original switching while the shunt transistors ($M3$, $M4$, $M5$ and $M6$) provide low-impedance paths for the unwanted signals to the RF ground. Therefore, the shunt arms make the switch obtaining relatively better isolation between the transmitter and the receiver port but at the cost of insertion loss.

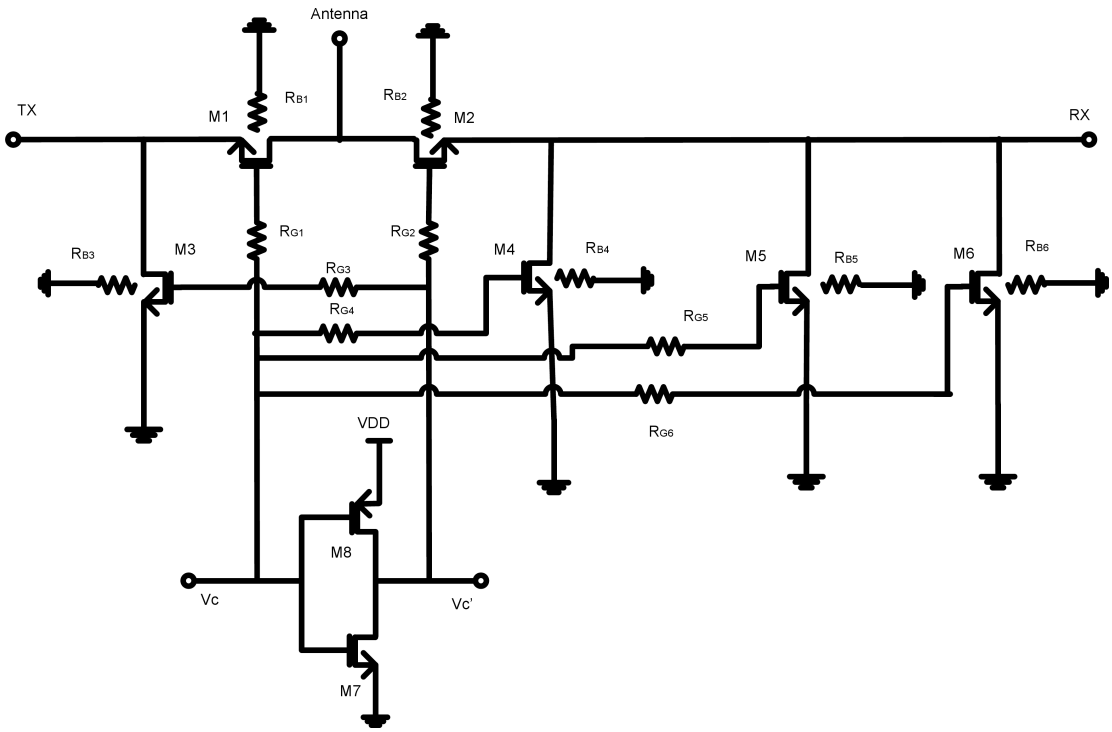

Fig. 2. Circuit schematic of proposed nanoswitch

During the transmit mode, a high control voltage Vc (1.8 V) is applied at the gate of transistors ($M1$, $M4$, $M5$ and $M6$) while control voltage Vc' at the gates of ($M2$ and $M3$) is kept low (0 V). As a result, the signal from the transmitter (power amplifier) is sent to the antenna and any signal leaking through $M2$ toward the receiver (Low noise amplifier) is shunted by the transistors $M4$, $M5$ and $M6$. The vice-versa is true for receive mode.

Figure 3 shows the simplified models of an NMOS transistor in both triode and cut-off mode of operation with body floated. During the nonconducting state, the NMOS acts as a simple capacitor (C_{off}) whereas during the conducting period it consists of a capacitor (C_{on}) shunted by the resistor (R_{on}) [7]. In the receive mode, the circuit in Fig. 2 is abridged to the equivalent circuit in Fig. 4 by using these models while the coupling effect to the transmitter is overlooked.

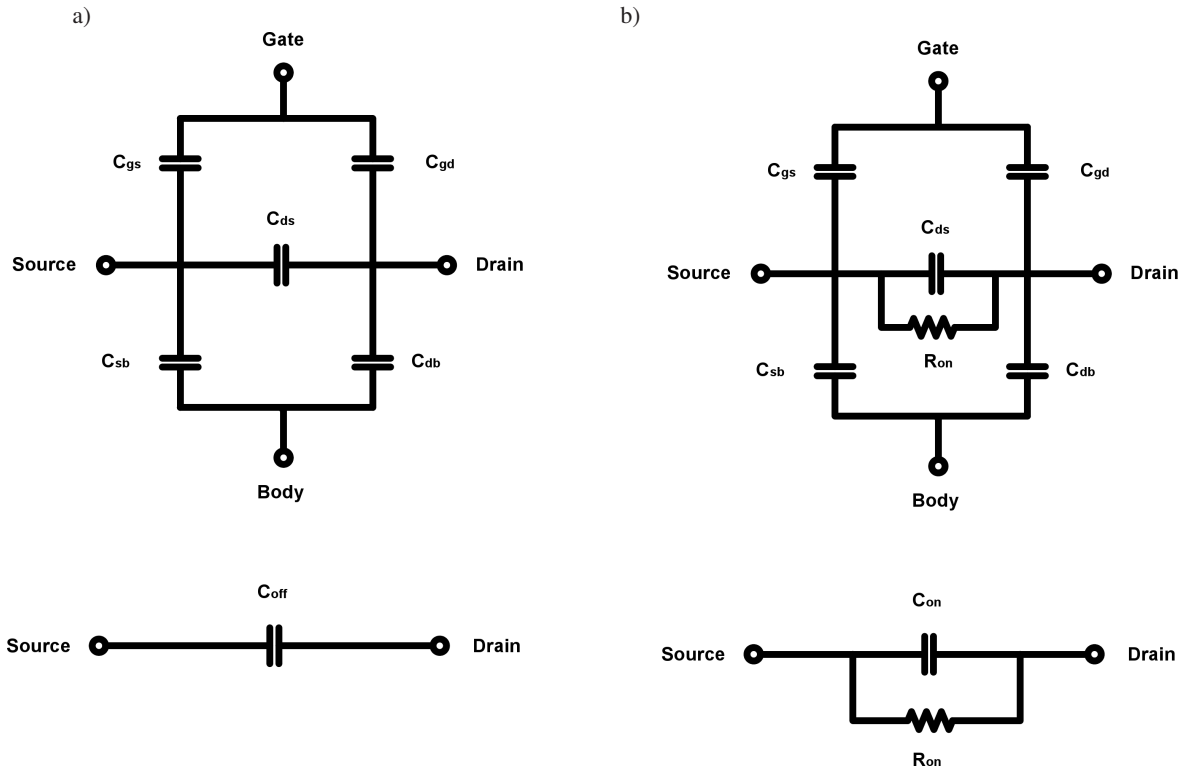

Fig. 3. Models of NMOS transistor in (a) Cut-off mode and (b) Triode mode

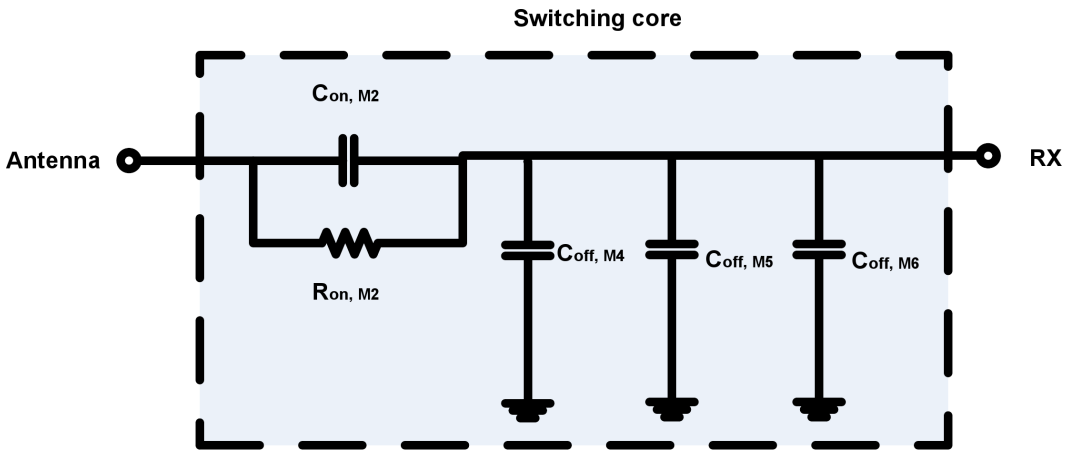

Fig. 4. Abridged equivalent circuit of the nanoswitch at receive mode

In order to quantitatively understand the impact of substrate resistances, capacitances and on-resistances on the circuit, insertion loss of the T/R nanoswitch in receive mode has been analyzed for simplicity. For this analysis, the transistor $M2$ is biased in the linear region whereas the transistors $M4$, $M5$ and $M6$ are kept in cut-off mode.

Insertion loss measures the small signal power loss through an RF switch when the switch is turned on. Insertion loss is inversely proportional with the S_{21} parameter of the switching core i.e.

$$IL \propto \frac{1}{|S_{21}|^2}. \tag{1}$$

According to Fig. 5, the value of S_{21} is

$$S_{21} = \frac{V_2 - I_2 Z_0}{V_1 + I_1 Z_0} = \frac{2V_2}{I_1(Z_1 + Z_0)}. \tag{2}$$

Here, Z_0 denotes the characteristic impedance of system and Z_1 is the total impedance seen at the port 1 whereas I_1 and I_2 are the currents at the antenna and receiver junction, respectively. The current I_1 and the impedance Z_1 are given by

$$Z_1 = Zeq + \left(\frac{1}{j\omega C_{off,M4}} + \frac{1}{j\omega C_{off,M5}} + \frac{1}{j\omega C_{off,M6}}\right) \tag{3}$$

and

$$I_1 = \frac{V_1}{Z_1} = \frac{V_1}{Zeq + \left(\frac{1}{j\omega C_{off,M4}} + \frac{1}{j\omega C_{off,M5}} + \frac{1}{j\omega C_{off,M6}}\right)}. \tag{4}$$

So we have,

$$S_{21} = \frac{2\left(Z_0 // \left(\frac{1}{j\omega C_{off,M4}} + \frac{1}{j\omega C_{off,M5}} + \frac{1}{j\omega C_{off,M6}}\right)\right)}{Z_0 + Zeq + \left(Z_0 // \left(\frac{1}{j\omega C_{off,M4}} + \frac{1}{j\omega C_{off,M5}} + \frac{1}{j\omega C_{off,M6}}\right)\right)}, \tag{5}$$

where

$$Z_{eq} = \frac{1}{j\omega C_{on,M2} + \frac{1}{R_{on,M2}}} \tag{6}$$

and

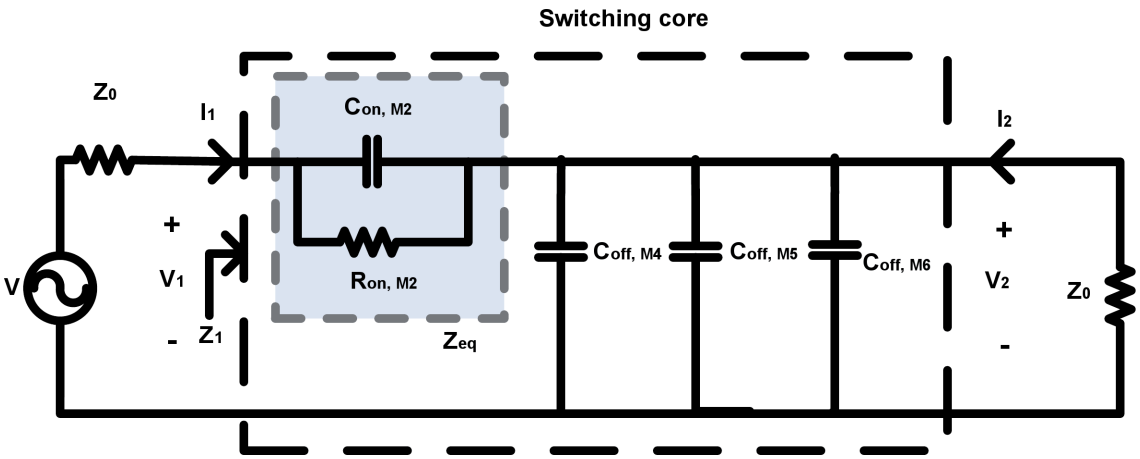

Fig. 5. Simplified receive mode circuit for determination of S_{21}

By substituting Eq. (5) into Eq. (1) we have,

$$IL \propto \left(\frac{Z_0 + Zeq + \left(Z_0 // \left(\frac{1}{j\omega C_{off,M4}} + \frac{1}{j\omega C_{off,M5}} + \frac{1}{j\omega C_{off,M6}} \right) \right)}{2\left(Z_0 // \left(\frac{1}{j\omega C_{off,M4}} + \frac{1}{j\omega C_{off,M5}} + \frac{1}{j\omega C_{off,M6}} \right) \right)} \right)^2, \tag{7}$$

where $R_{on,M2}$ is on resistance of the $M2$ transistor. Moreover, by neglecting the values of $C_{on,M2}$, $C_{off,M4}$, $C_{off,M5}$ and $C_{off,M6}$, Eq. (7) simplifies to

$$IL \propto \left(\frac{2Z_0 + R_{on,M2}}{2Z_0} \right)^2. \tag{8}$$

According to Eq. (8), the insertion loss of a transistor is primarily depends on its on-state resistance (R_{on}) which is given by

$$R_{on} = \frac{1}{\mu_n C_{ox} \dfrac{W}{L}(V_{GS} - V_{TH})}, \tag{9}$$

where μ_n is the mobility of electrons and C_{ox} represents capacitance of the gate.

Equation (9) shows that lower R_{on} can be achieved by using transistors having high mobility, large aspect ratio (W/L) and high gate-to-source/channel voltage (V_{GS}). Therefore, NMOS transistors are chosen to implement the proposed nanoswitch since mobility of the NMOS transistors is approximately three times higher than the mobility of PMOS transistors. Besides the transistors in the ON state are biased by 1.8 V gate-to-channel voltage which prevents both avalanche and gate-oxide breakdown. Additionally, aspect ratio (W/L) is the dominant factor determining the ON resistance of transistors $M1$ or $M2$ and *IL* as well. From Eq. (9), as the aspect ratio is made to increase, insertion loss of the switch decreases. But there is a practical limit in enlargement of transistor width because the source/drain to body parasitic capacitance becomes prominent which in turn degrades the isolation. In other words, there is a trade-off between R_{on} and parasitic capacitances which results in an optimum value for width of the transistor at a given operating frequency. The optimum width for 2.4 GHz ISM band is found to be 100 μm.

On the other hand, body floating technique is used to improve power handling of the switch by reducing the signal loss through source/drain-to-body junctions [14]. Usually, the body of a transistor is connected to its source and the equivalent circuit is shown in Fig. 6a. For small input power, the drain-to-source current is almost zero when the transistor turns off. However, when the input power is made to increase, the drain-to-source voltage becomes so negative as to turn on the diode between drain and body and the input impedance of the transistor becomes lower. But if the body floating technique is adopted, the body of the transistor is tied with the ground with a high resistance (R_B) as shown in Fig. 6b. Therefore, it retains high input impedance of the transistor to maintain better power performance of the switch. The gate resistances are used to provide DC bias isolation at the gates. These resistances are used to mitigate the voltage fluctuations around the gate terminal which can affect the channel resistance as well as can cause breakdown at the gate terminal [15]. Moreover, in order to keep the switching speed of the transistor, choosing a suitable gate bias resistor is very important [16]. So, we used 5 KΩ resistors for body floating (R_{B1}-R_{B6}) and 5 Ω for gate biasing (R_{G1}-R_{G6}). The circuit elements utilized in this architecture and their values are given in Table 1.

Table 1
Nanoswitch elements and their values

Elements	Value
M1–M8	100/0.13 (μm/μm)
R_{G1}–R_{G6}	5 Ω
R_{B1}–R_{B6}	5 KΩ

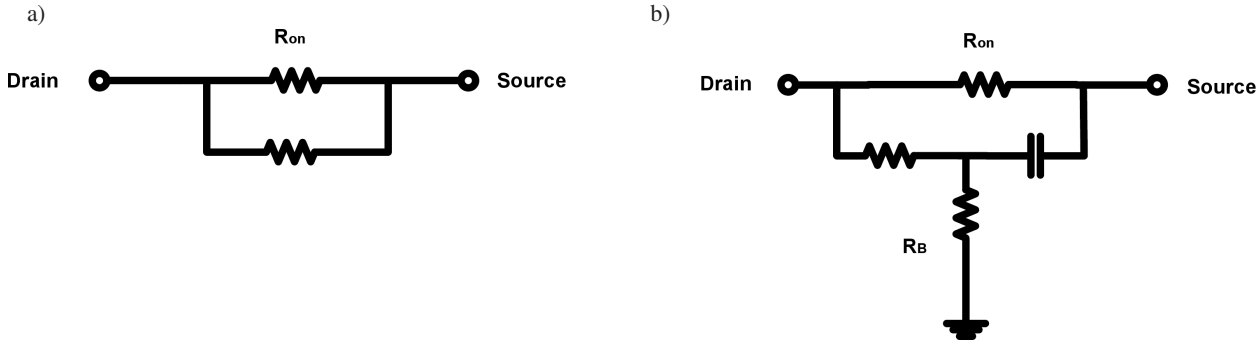

Fig. 6. MOS transistor (a) without and (b) with body floating technique after Ref. 12

3. Results and discussions

Mentor Graphics 130 nm CMOS process has been used for the design and simulation of the proposed nanoswitch. Figure 7 illustrates the isolation and insertion loss property of the switch for the variation of 100 MHz frequency from 2.4 GHz to 2.5 GHz. It is clear that the insertion loss and isolation remain almost constant for 2.4 GHz ISM band which are 1.03 dB and 27.57 dB respectively.

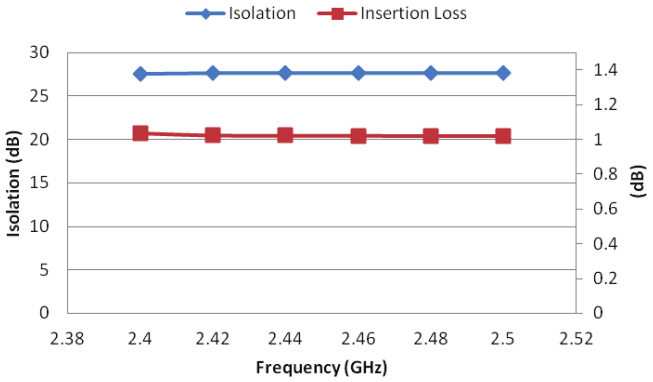

Fig. 7. Isolation and Insertion Loss of the proposed nanoswitch

The variations of insertion loss and isolation of the nanoswitch with input power (P_{in}) are shown in Figs. 8 and 9. In the TX mode, isolation is measured from the TX port to the RX port, whereas the insertion loss is measured from TX port to Antenna port. Similarly, in the RX mode, isolation is measured from the Antenna port to the TX port whereas the insertion loss is measured from Antenna port to RX port. The insertion loss is observed to increase almost exponentially with input power in both modes but the rate of change is higher in RX mode. On the other hand, for the isolation, the slope is negative for both modes but the rate of change of isolation in RX mode is stiffer. The values of the insertion loss and isolation are 1.03 dB (TX mode) and 1.76 dB (RX mode) and 27.57 dB (TX mode) and 13.05 dB (RX mode), respectively.

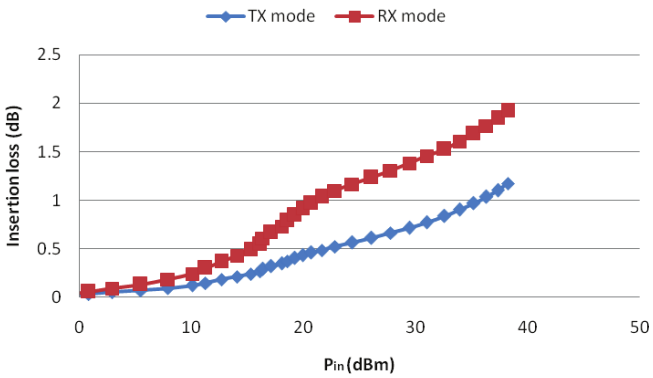

Fig. 8. Insertion Loss of the proposed nanoswitch with input power

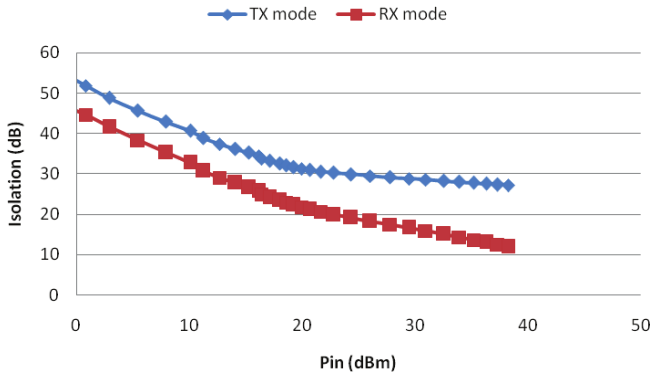

Fig. 9. Isolation of the proposed nanoswitch with input power

The linearity of a switch determines the input power limit for which it works in the lianear manner which is evaluated by 1 dB compression point ($P_{1\,\mathrm{dB}}$). Figure 10 describes the measurement of $P_{1\,\mathrm{dB}}$ of the nanoswitch the value of which is 36.2 dBm. The linearity of the nanoswitch in the 2.4 GHz band is shown in the Fig. 11. The maximum variation in $P_{1\,\mathrm{dB}}$ point found in this band is 0.01 dBm which demonstrates the stability of the nanoswitch.

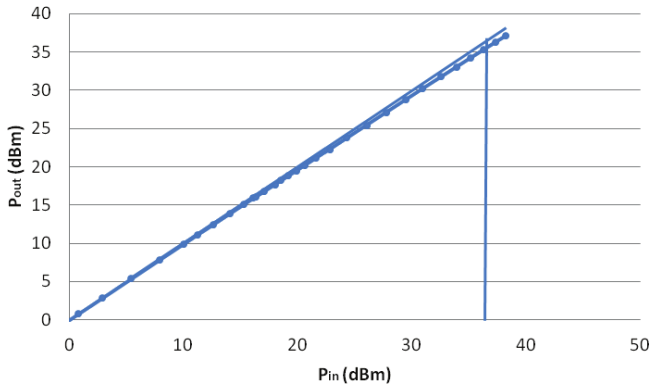

Fig. 10. Linearity measurement of the nanoswitch

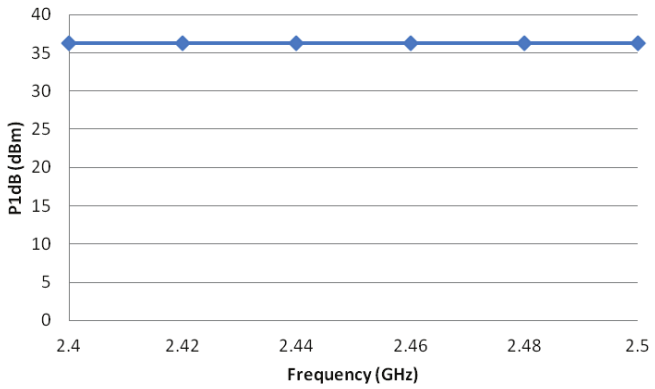

Fig. 11. Linearity of the proposed nanoswitch at 2.4 GHz band

The reliability and stability of a T/R switch is also important along with its performance. For a circuit, it is necessary to determine the reliability against the temperature of the surroundings. Both the insertion loss and isolation against the

temperature for the proposed T/R switch, as shown in Fig. 12, are observed to decrease. For 125°C temperature difference (from −25°C to 100°C) the variations in insertion loss and isolation are 0.1 dB and 0.9 dB respectively.

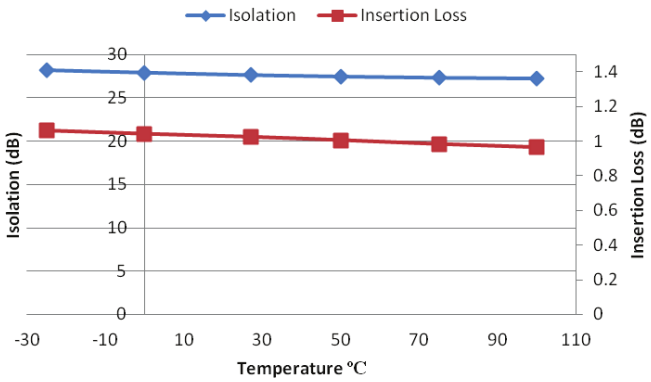

Fig. 12. Insertion loss and isolation of the nanoswitch with temperature

In the proposed nanoswitch design, the best trade-off among insertion loss, isolation and power handling ($P_{1\,\mathrm{dB}}$) has been set up at 2.4 GHz frequency band to obtain the optimal performance. As a result, it exhibits high power handling capability with a very small insertion loss and better isolation of receiver during transmission mode. High isolation during the transmission period improves the transmission efficiency as well as protects the low power receiver circuit from being got damaged. The low insertion loss ensures that more power is transferred to the intended port with minimum loss. Furthermore, the high power handling capacity of the nanoswitch makes it reliable for larger signal transmission with better linearity. Similarly, low insertion loss and high isolation is vital for reception mode as the receiver handles low power signals. Moreover, small switching time is a crucial issue specially for high frequency applications.

Therefore, the nanoswitch is found to exhibit 1.03-dB insertion loss, 27.57-dB isolation and 36.2-dBm power handling capacity with 6.87 μW power dissipation and 416.61 ps switching time (Fig. 13), which are very much competitive to the previous works at 2.4 GHz ISM band. Besides the reliability and stability of the nanoswitch make it appropriate for IEEE 802.11b/g/n CMOS transceivers. Moreover, it occupies only 0.0071 mm^2 of IC space, as illustrated in Fig. 14, which is the lowest ever reported in this frequency band. A comparison of this work to the recently reported performances of 2.4 GHz CMOS switches is given in Table 2.

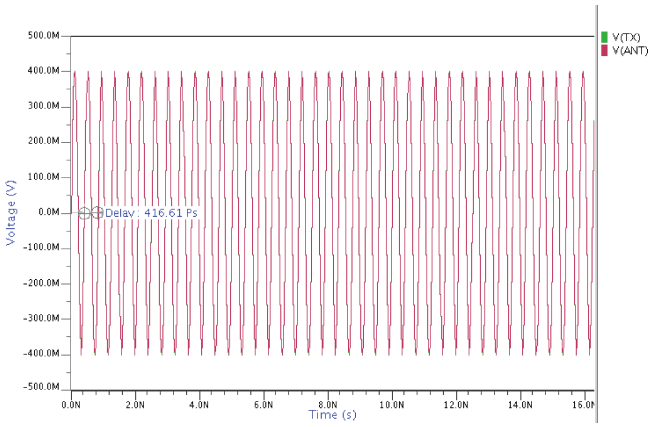

Fig. 13. Switching delay of the nanoswitch at 2.4 GHz band

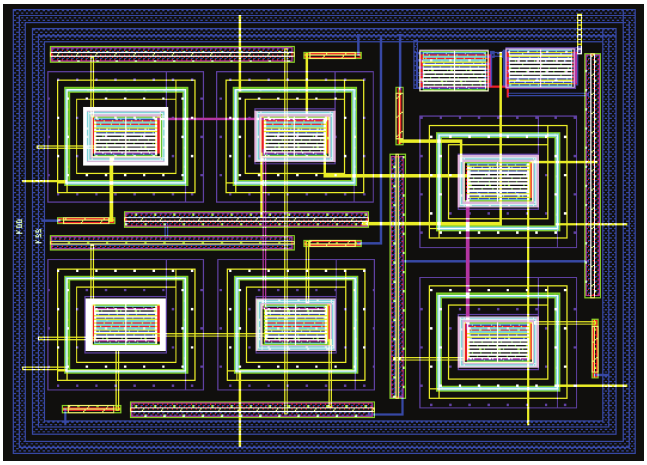

Fig. 14. Layout of the proposed nanoswitch (0.1 mm × 0.071 mm)

Table 2
Performance comparison of series-shunt CMOS switches for 2.4 GHz band applications

Ref.	Year	CMOS Process	Vc/Vc′ [volts]	Isolation [dB]	$P_{1\,\mathrm{dB}}$ [dBm]	IL [dB]	Area [mm^2]	Comments
[8]	2001	0.18-μm	1.8/0	24	11	1.5	0.45*	Optimizing gate width
[9]	2001	0.18-μm	6.0/2.0	24.4	17	0.8	0.28	Optimizing transistor widths and dc biasing
[10]	2004	0.18 μm	6.0/2.0	20.6	20.6	1.1	0.28	Impedance transformation
[11]	2004	0.35μm	3.6/0	42	16	1.3	0.026	Parasitic MOSFET model
[14]	2006	0.18-μm	1.8/0	35	21.3	0.7	0.03	Body-floating
[16]	2008	0.5μm	1.2/0	–	25.33	1.085	–	DC biasing
This work	2014	0.13 μm	1.8/0	27.57	**36.2**	1.03 (TX)	**0.0071**	Optimizing gate width and body floating

* including pads

4. Conclusions

In an RF switch design, the best trade-off among insertion loss, isolation and power handling ($P_{1\,dB}$) must be set up at a given frequency band for its optimum performance. In this paper, a miniature SPDT nanoswitch in 130 nm CMOS technology for 2.4 GHz wireless terminals is presented. It exhibits 1.03-dB insertion loss, 27.57-dB isolation and 36.2-dBm $P_{1\,dB}$ for 1.8/0 V control voltages. This T/R switch need only 416.61 ps time and dissipates 6.87 μW power for its switching. Moreover it occupies only 0.0071 mm^2 of IC space, to the authors' best knowledge, which is the lowest ever reported in this frequency band. The stability and reliability of the switch makes it very much suitable for 2.4 GHz wireless terminals.

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