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Multiple output CMOS current amplifier

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Abstract. In this paper the multiple output current amplifier basic cell is proposed. The triple output current mirror and current follower circuit are described in detail. The cell consists of a split nMOS differential pair and accompanying biasing current sources. It is suitable for low voltage operation and exhibits highly linear DC response. Through cell devices scaling, not only unity, but also any current gains are achievable. As examples, a current amplifier and bandpass biquad section designed in CMOS TSMC 90nm technology are presented. The current amplifier is powered from a 1.2V supply. MOS transistors scaling was chosen to obtain output gains equal to –2, 1 and 2. Simulated real gains are –1.941, 0.966 and 1.932 respectively. The 3dB passband obtained is above 20MHz, while current consumption is independent of input and output currents and is only 7.77μA. The bandpass biquad section utilises the previously presented amplifier, two capacitors and one resistor, and has a Q factor equal to 4 and pole frequency equal to 100 kHz.

Key words: current amplifier, current follower, current mirror, CMOS technology.

1. Introduction

Current conveyors, current mirrors, and current followers have received much attention during recent years of electronics development [1–9]. Current mode amplifiers are often used in filtering applications [4–9]. Among others, filters employing multiple output amplifiers are especially interesting. The use of multiple output amplifiers results in a simpler filter structure, a smaller area occupied, and lower costs and power consumption of the system [6]. The simple current mirror may be used as a current amplifier. Unfortunately, such a circuit has a negative current gain. To obtain positive current gain, usually a pMOS current mirror follows a nMOS mirror [1]. Such a solution is quite simple – it only adds 2 devices. Unfortunately, due to about 3 times lower mobility of holes as compared to electrons, the frequency response of a pMOS mirror working in the same conditions as the nMOS mirror is about 3 times worse. This is because pMOS devices must be 3 times larger than their nMOS counterparts to achieve the same transconductance factor, which in turn results in 3 times increased capacitance. Another solution to obtain positive current gain is the use of a differential pair instead of a double current mirror [2, 3]. Such a circuit requires special polarisation [2] or nMOS to pMOS devices matching [3] and also yields only gains equal to –1 or 1. In fact, those circuits are current followers and to obtain any real gain an additional stage is necessary. In this paper, a current amplifier based on a split nMOS pair is presented. It has 3 current outputs, one inverting and two non-inverting. Although the basic amplifier cell described below has current gains equal to –1 and 1, through proper nMOS devices scaling, other values of current gains are possible. Such a solution is used in the examplary application of the core cell described in the next chapter.

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2. Core of current amplifier circuit

Proposed current mirror/follower is based on nMOS differential pair and is presented in Fig. 1. Both differential pair devices are split into equal M_{1A}, M_{1B} and M_{2A}, M_{2B} transistors, respectively. Assuming that all devices are in saturation and neglecting second order effects, such as body effect and channel length modulation, due to equal gate-source voltages, drain currents of M_{1A} and M_{1B} are identical and the drain currents of M_{2A} and M_{2B} are also equal. Assuming $I_{IN} = 0$ for bias point calculation, it gives current of $I_{D\,(M1A)}$ and $I_{D\,(M1B)}$ equal to I_{BIAS}. According to Kirchhoff's Current Law (KCL) in sources node, the sum of all transistors currents is equal to $4*I_{BIAS}$, taking into account that $I_{D\,(M2A)} = I_{D\,(M2B)}$ gives all transistors currents equal to I_{BIAS}. Due to the currents' equality, the voltage seen at the gate of M_{1A} and M_{1B} must be identical to the voltage at gate of M_{2A}

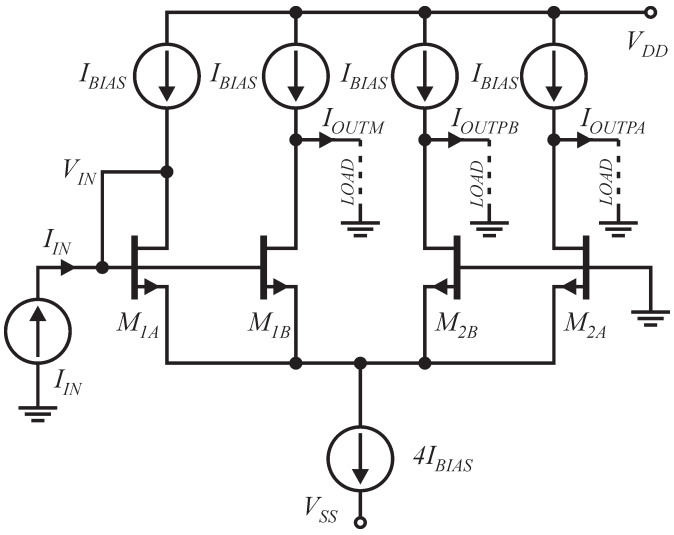

Fig. 1. Core of the proposed current amplifier cell

and M_{2B}, and is also equal to 0. Note that voltage set at gates of M_{2A} and M_{2B} automatically passes to the input of the circuit (gates of M_{1A} and M_{1B}).
In the case when input current occurs, KCL in sources node gives:

$$\begin{aligned} &I_{S(M1A)} + I_{S(M1B)} + I_{S(M2A)} + I_{S(M2B)} \approx \\ &2(I_N + I_{BIAS}) + I_{D(M2A)} + I_{D(M2B)} = 4I_{BIAS} \end{aligned}, \quad (1)$$

and after taking into account $I_{D\,(M2A)} = I_{D\,(M2B)}$ and transformation, it yields output currents equal to:

$$I_{OUTM} = -I_N\ , \quad (2)$$

$$I_{OUTPA} = I_{OUTPB} = I_N\ . \quad (3)$$

The circuit is linear if all the devices are identical. The function's shape of drain current in regard to gate-source voltage is not important as long as all the devices are identical. It can be proven that this linearity condition is in fact less demanding and theoretical full linearity occurs only if M_{1A} and M_{2A} and simultaneously M_{1B} and M_{2B} are the same. Also, since all the transistors have their source terminals tied together, the body effect is identical in all the devices and does not alter transfer function. Note that the presented current amplifier has one inverting output and two non-inverting outputs. The two non-inverting outputs can be linked together to obtain one output with gain equal to 2. The amplifier works with constant current consumption independent of input signal level. This also limits input and output currents to I_{BIAS}:

$$\begin{aligned} &\left|I_{IN}\right| \le I_{BIAS},\ \left|I_{OUTM}\right| \le I_{BIAS}\ ,\ \left|I_{OUTPA}\right| \le I_{BIAS} \\ &\text{and } \left|I_{OUTPB}\right| \le I_{BIAS} \end{aligned} \quad (4)$$

Higher input currents than given by (4) will cause pair saturation and cannot be transferred to the amplifier outputs. The range of voltages at outputs is restricted by saturation of M_{1B}, M_{2A} and M_{2B} transistors and should be kept according to:

$$\begin{aligned} &V_{OUTM} \ge V_{IN} - V_{Th,\,M1B},\ V_{OUTPA} \ge -V_{Th,\,M2A}, \\ &V_{OUTPB} \ge -V_{Th,\,M2B} \end{aligned} \quad (5)$$

where: $V_{Th,\,M1B}$, $V_{Th,\,M2A}$ and $V_{Th,\,M2B}$ are the threshold voltages of devices M_{1B}, M_{2A} and M_{2B}, respectively and V_{IN} is the actual voltage at input terminal.

3. Small-signal analysis of core cell

Small-signal analysis is performed assuming a simplified MOS model which only contains main transconductance gm, output resistance r_o (for output resistance estimation) and gate-source capacitance C_{GS} (for frequency response estimation). Note that all devices in Fig. 1 are identical and polarised with the same drain current I_{BIAS}. This results in equal parameters of small-signal model for all transistors. Assuming saturation of MOS devices, their equivalent small-signal transconductance parameter is as follows [10]:

$$gm = 2\sqrt{KI_{BIAS}} \quad (6)$$

where: $K = 0.5\mu_n C_{OX} W/L$, W and L are width and length of MOS devices, μ_n is mobility of carriers, C_{OX} is oxide capacitance by unit area. Similarly, output resistance r_O and gate-source capacitance C_{GS} can be expressed as [10]:

$$r_O = 1/(\lambda I_{BIAS}),\ C_{GS} = 2/3 C_{OX} W/L, \quad (7, 8)$$

where λ is channel length modulation parameter. Using above parameters and additionally assuming ideal input current source and ideal short-circuit load to the signal ground, one can evaluate small-signal parameters as:
– input resistance for low frequencies equal to:

$$r_{in} \approx 2/gm \quad (9)$$

– output resistance for low frequency inverting output:

$$r_{OUTM} \approx r_O + 1/(2gm) \approx r_O \quad (10)$$

– output resistance for low frequency non-inverting outputs:

$$r_{OUTPA} = r_{OUTPB} \approx r_O\left(2 + \frac{1}{gmr_O}\right) \approx 2r_O \quad (11)$$

– current transmittance to inverting output:

$$\frac{i_{OUTM}(s)}{I_N(s)} \approx -\frac{gm}{gm + 2sC_{GS}} \quad (12)$$

– current transmittance to non-inverting outputs:

$$\frac{i_{OUTPA}(s)}{I_N(s)} = \frac{i_{OUTPB}(s)}{I_N(s)} \approx \frac{gm}{gm + 2sC_{GS}} \cdot \frac{gm + sC_{GS}}{gm + sC_{GS}} \quad (13)$$

Note that non-inverting output transmittance (13) has identical pole and zero; this transmittance transforms to an inverting output given by (12). In fact, extra capacitance in node connecting all sources of MOS devices, which in real circuit is caused by current source $4I_{BIAS}$, results in a shift of the pole and a non-ideal compensation of (13) occurs. Designating this extra capacitance as C_{SOURCE}, one can calculate non-inverting current transmittance as:

$$\begin{aligned} &\frac{i_{OUTPA}(s)}{I_N(s)} = \frac{i_{OUTPB}(s)}{I_N(s)} \approx \\ &\approx \frac{gm}{gm + 2sC_{GS}} \cdot \frac{2gm + 2sC_{GS}}{2gm + s\left(2C_{GS} + C_{SOURCE}\right)} \cdot \end{aligned} \quad (13)$$

Despite this extra capacitance, the dominant pole remains unchanged and is located at $-gm/(2C_{GS})$.

4. Comparison to other current followers and current mirrors

To validate the performance of the proposed circuit, a comparison to a typical current mirror, double current mirror and circuit reported in [3] is presented in Table. 1. Double current mirror here signifies an nMOS current mirror, followed by a pMOS current mirror in order to obtain non-inverting current gain. To further simplify the comparison, any MOS transistor or current source is counted as one device. To calculate the range of input/output voltages, V_{DD} and V_{SS} are treated as power supply nodes, V_{GS} is treated as polarising gate-source voltage (in real circuits it depends mainly on MOS threshold voltage and drain current, typically within the range of 0.6 V–1.2V) and $V_{DS,\,SAT}$ is treated as minimal polarising voltage between drain and source to maintain MOS in saturation (in real circuits this voltage is lower than V_{GS} by threshold voltage, typically within the range of 0.2V–0.6V). To further simplify the comparison, pMOS devices are treated as having a transconductance parameter 3 times lower than nMOS, due to lower holes mobility than electron mobility in the device channel. This implies that to obtain the same transconductance for pMOS device as for nMOS, having the same drain current, the dimensions of pMOS device must be 3 times higher and resulting gate-source capacitance C_{GS} of such a device will also be 3 times higher than that of its nMOS counterpart. In small-signal analysis, the following parameters' designators were used: MOS device transconductance $gm = 2\sqrt{KI_{BIAS}}$, where $K = 0.5\mu_n C_{OX} W/L$, W and L are width and length of MOS devices, μ_n is mobility of carriers, C_{OX} is oxide capacitance by unit area; MOS output resistance $r_O = 1/(\lambda I_{BIAS})$, where λ is channel length modulation parameter and gate-source capacitance $C_{GS} = 2/3C_{OX}W/L$ [10].

The proposed amplifier uses more transistors than other structures in Tab. 1, but in return it offers three outputs, two positive and one inverting. The dominant pole of the transfer function is the same as for nMOS current mirror; it is the best option among presented amplifiers. Due to usage of current source $4I_{BIAS}$, available minimal power supply voltage is higher by voltage $V_{DS,\,SAT}$ than for simple nMOS mirror. Also, output resistance is similar to the simple current mirror. Summarising the whole comparison, the proposed core cell is suitable for usage in current mode circuits. At the price of a slightly larger area and power consumption, it offers multiple outputs and undegraded passband as compared to nMOS current mirror.

5. Application examples

The proposed current amplifier core can be used stand-alone after current sources I_{BIAS} and $4I_{BIAS}$ implementation, or as a sub-block of larger circuit, for example as output stage of current conveyor.

Table 1.
Comparison of proposed current amplifier with current mirror, double current mirror and current amplifying core from [3]

Parameter/Circuit	Proposed amplifier in Fig. 1	nMOS current mirror	Double current mirror	Current amplifying core [3]
Current gain	–1 and 1	–1	1	–1 and 1
Outputs count	3	1	1	2
Self regulated input voltage level	yes	no	no	yes
nMOS to pMOS devices scaling requirement	no	no	no	yes
Input current range	$-I_{BIAS}$ to I_{BIAS}	$-I_{BIAS}$ to more than I_{BIAS}	$-I_{BIAS}$ to more than I_{BIAS}	$-I_{BIAS}$ to I_{BIAS}
Dominant current transmittance pole	$-gm/(2C_{GS})$	$-gm/(2C_{GS})$	$-gm/(6C_{GS})$	$-gm/(4C_{GS})$
Input resistance	$2/gm$	$1/gm$	$1/gm$	$2/gm$
Output resistance	inv. $\approx r_O$ non inv. $\approx 2r_O$	r_O	r_O	inv. $\approx r_O$ non inv. $\approx 2r_O$
Current consumption	$4I_{BIAS}$	$2I_{BIAS}$	$3I_{BIAS}$	$3I_{BIAS}$
Devices count	7	4	6	5
Minimal power supply voltage $V_{DD} - V_{SS}$	$V_{GS} + 2V_{DS,SAT}$	$V_{GS} + V_{DS,SAT}$	$V_{GS} + V_{DS,SAT}$	$V_{GS} + 2V_{DS,SAT}$

5.1. Triple output current amplifier

Figure 2 presents stand-alone current amplifier. The circuit was designed using a 90nm CMOS TSMC process; simulations were performed in CADENCE Virtuoso environment. It has 1 input and 3 outputs. Unused outputs should be connected to signal ground for proper operation. Otherwise, due to the high resistance of the unconnected pin, MOS devices located at outputs

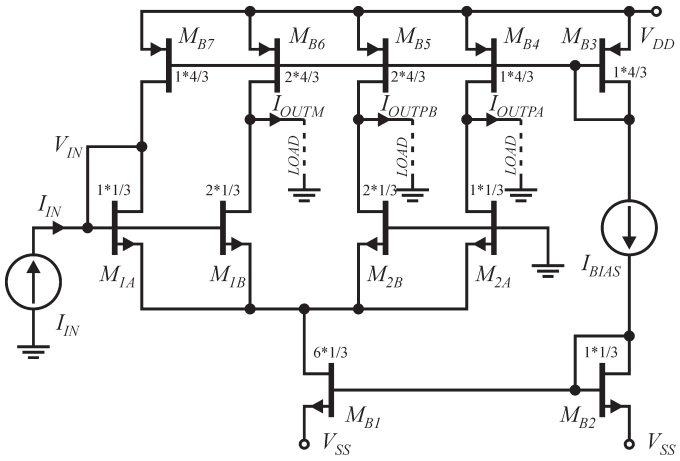

Fig. 2. Triple output current amplifier including bias circuitry with scaling factor SF=2; device dimensions are given in µm and the format is multiplier*width/length

Table 2.
Simulated parameters of the current amplifier from Fig. 2

Power Supply $V_{DD} - V_{SS}$	1.2V
Current consumption	7.77µA
Bias current I_{BIAS}	1.1µA
Current gains at *OUTM*, *OUTPA* and *OUTPB* at $I_{IN} = 0$	–1.941; 0.9662; 1.932
3dB passband for inverting output	21.75MHz
3dB passband for non-inverting outputs	20.57MHz
Input resistance at $I_{IN} = 0$	131.4kΩ
Input capacitance at $I_{IN} = 0$	58fF
Output resistance I_{OUTM} at $V_{OUTM} = 0$	2.49MΩ
Output resistance I_{OUTPA} at $V_{OUTPA} = 0$	5.56MΩ
Output resistance I_{OUTPB} at $V_{OUTPB} = 0$	3.15MΩ
Output capacitance I_{OUTM} at $V_{OUTM} = 0$	8.65fF
Output capacitance I_{OUTPA} at $V_{OUTPA} = 0$	4.32fF
Output capacitance I_{OUTPB} at $V_{OUTPB} = 0$	8.65fF
Input voltage at $I_{IN} = 0$	1.215mV
Input referred current noise at 100kHz	1.583pA/$\sqrt{Hz}$
Amplitude of harmonic 10kHz input signal at THD = 1% for *OUTPB*	1.06µA

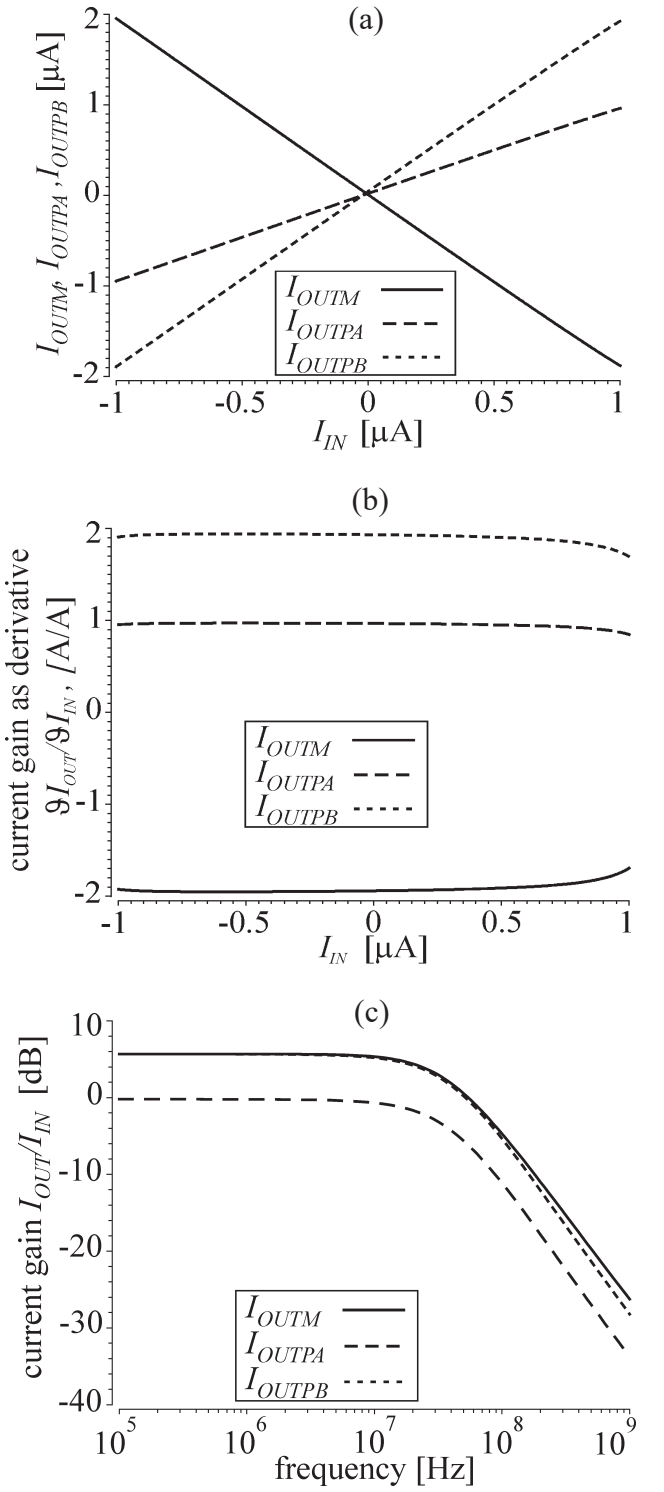

Fig. 3. Simulated responses of current amplifier from Fig. 2, a) and b) DC transfer responses, c) frequency responses of amplifier

can go out of saturation region. In the case of current gains other than 1 or –1 being desirable, M_{1A} to M_{1B} and identical M_{2B} to M_{2A} together with accompanying current sources devices scaling can be used. Thus, any current gain can be achieved. Note that gain to *OUTPA* is always equal to 1, while the gain to *OUTPB* and *OUTM* can be scaled. Assuming that all devices have the same channel length, current gain after MOS scaling is equal to:

$$\frac{I_{OUTPB}}{I_N} = -\frac{I_{OUTM}}{I_N} = \frac{W_{M1b}}{W_{M1a}} = \frac{W_{M2b}}{W_{M2a}} = SF. \qquad (14)$$

In the presented application example in Fig. 2, scaling coefficient *SF* equal to 2 was chosen, thus, through proper outputs' shorting, current amplifier of gain equal to –2, –1, 1, 2 and 3 can be implemented. Simulated circuit responses and parameters are presented in Fig. 3 and Table 2. The current gains obtained (–1.941, 0.9662 and 1.932) differ slightly from the theoretical ones (–2, 1 and 2). This small difference is caused mainly by nMOS output resistances, which were omitted in calculations. Note that the amplifier can also be arranged by splitting the nMOS pair into any number of transistors instead of two. This way a multiple output circuit can be achieved, with any desired output count and gains. The number of devices creating differential pair M1 and M2 is not important as long as the total width of all devices included in M1 is equal to the total width of all devices included in transistor M2, assuming additionally identical lengths for all transistors.

5.2. Bandpass biquad section

Current amplifiers can be used to build current mode circuits such as filters and biquad sections [4–9]. As an examplary application, a bandpass biquad section is presented in Fig. 4. It uses the current amplifier from Fig. 2, two capacitors and one resistor. Input resistance of the amplifier is used as resistance R_2. The feedback path utilises *OUTPB* output pin, while pins *OUTPA* and *OUTM* are non-inverting and inverting outputs of the biquad, respectively. The transfer functions of the section to both outputs are equal to:

$$\frac{I_{OUTPA}(s)}{I_N(s)} = \frac{\frac{R_1C_2}{R_1R_2C_1C_2}}{s^2 + \frac{R_1C_1 + R_2C_2 + R_1C_2 - BR_1C_2}{R_1R_2C_1C_2}s + \frac{1}{R_1R_2C_1C_2}}, \qquad (15)$$

$$\frac{I_{OUTM}(s)}{I_N(s)} = M\frac{\frac{R_1C_2}{R_1R_2C_1C_2}}{s^2 + \frac{R_1C_1 + R_2C_2 + R_1C_2 - BR_1C_2}{R_1R_2C_1C_2}s + \frac{1}{R_1R_2C_1C_2}}, \qquad (16)$$

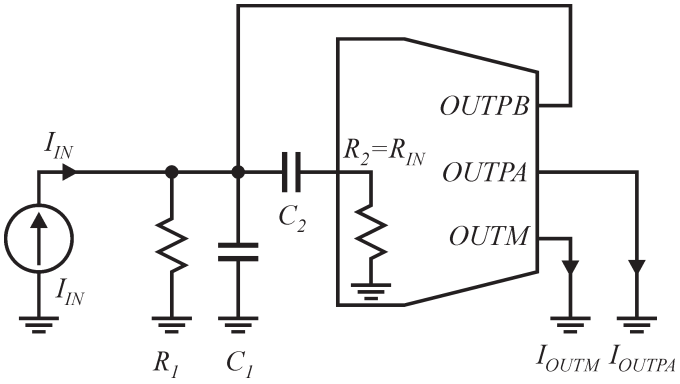

Fig. 4. Bandpass biquad section with the use of current amplifier from Fig. 2

where *A*, *B* and *M* are the current gains of the outputs *OUTPA, OUTPB* and *OUTM* and are realised through device scaling according to (14). In order to keep the circuit stable, all denominator coefficients must be positive, so the following condition must be satisfied:

$$R_1C_1 + R_2C_2 + R_1C_2 > BR_1C_2 \qquad (17)$$

Both transmittances (15) and (16) differ only in coefficient before fraction. Comparing (15) and (16) to general transmittance of bandpass biquad section [10], one can calculate gain H_O, quality factor Q and pole frequency ω_O as:

$$H_{O,OUTPA} = A\frac{R_1C_2}{R_1C_1 + R_2C_2 + R_1C_2 - BR_1C_2}, \qquad (18)$$

$$H_{O,OUTM} = M\frac{R_1C_2}{R_1C_1 + R_2C_2 + R_1C_2 - BR_1C_2}, \qquad (19)$$

$$Q = \frac{\sqrt{R_1R_2C_1C_2}}{R_1C_1 + R_2C_2 + R_1C_2 - BR_1C_2}, \qquad (20)$$

$$\omega_O = \frac{1}{\sqrt{R_1R_2C_1C_2}}. \qquad (21)$$

Although the resistance R_1 is necessary for proper biquad operation, the relatively high value of output resistance of the amplifier can be used instead; thus, lower pole frequency can be obtained and R_1 can be removed. For testing purposes, simulations of biquad section were performed. Values of resistors and capacitors were chosen to obtain quality factor Q = 4 and pole radial frequency $\omega_O = 2\pi 100$ krad/s. As R_2, input resistance of the current amplifier was employed. Unfortunately, the gain parameters $H_{O,\,OUTPA}$ and $H_{O,\,OUTM}$ are scaled simultaneously with Q factor. Resulting gain factors are equal to $H_{O,\,OUTPA} = 7.3$ and $H_{O,\,OUTM} = -14.6$. To obtain specific desirable gain factors of the filter, actual current gains of the amplifier can be arranged ac-

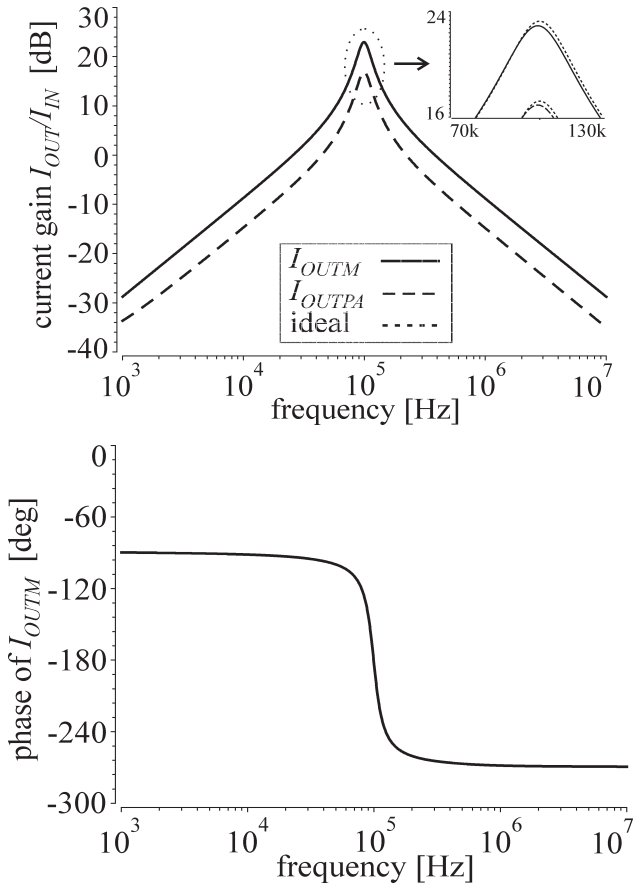

Fig. 5. Simulated frequency responses of bandpass biquad section from Fig. 4

cording to (14). Simulated circuit responses and parameters are presented in Fig. 5 and Table 3. Dotted lines represent theoretical frequency responses of the biquad section. To see differences between theoretical and obtained amplitude frequency responses, the central part of Fig. 5 (a) was zoomed in and is presented in the upper right corner. Differences of phase responses are too small to be seen and due to this, only the obtained characteristics are presented in Fig. 5 (b). Power consumption of the filter is the same as in the amplifier. Higher order filters and other current mode circuits can be implemented by cascading presented biquad or using known synthesis techniques [4–10].

6. Conclusions

The current amplifying core circuit has been introduced. It combines a current follower and a current mirror amplifier in one core. Through further appropriate device scaling, any current gain can be realised instead of unity gains equal to –1 and 1. The circuit is based on a split differential pair. The proposed circuit is very simple and capable of operating in modern, low voltage technologies. It also exhibits good frequency responses with frequency range of operation comparable to current mirrors and differential pairs. The proposed current amplifier core can be used stand-alone or as a subcircuit, for example as an output stage of current conveyors or transconductance

Table 3.
Parameters of the bandpass biquad section from Fig. 4

Power Supply $V_{DD} - V_{SS}$	1.2V
Current consumption	7.77µA
Designed pole frequency f_O	100kHz
Designed quality factor Q	4
Designed gain factors $H_{O,OUTPA}$ and $H_{O,OUTM}$	7.3 and –14.6
Simulated pole frequency f_O	99.3kHz
Simulated gain factors $H_{O,OUTPA}$ and $H_{O,OUTM}$	7.01 and –14.02
Input referred current noise at 100KHz	2.68pA/$\sqrt{Hz}$
Calculated value of R_1	268kΩ
Value of R_2 – input resistance of the current amplifier	131.4kΩ
Calculated value of C_1	6.44pF
Calculated value of C_2	12.11pF

amplifiers. Due to 3 built-in outputs, it is especially suited for applying in multiple output circuits such as current-mode filters, signal converters, etc. Computer simulations using CMOS TSMC 90nm technology of two application examples confirm the usability of the proposed circuit.

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