

# Low-power low-area techniques for multichannel recording circuits dedicated to biomedical experiments

P. KMON\*

Department of Measurement and Electronics, AGH University of Science and Technology, 30 Mickiewicza Av., 30-059 Krakow

**Abstract.** This paper presents techniques introduced to minimize both power and silicon area of the multichannel integrated recording circuits dedicated to biomedical experiments. The proposed methods were employed in multichannel integrated circuit fabricated in CMOS 180nm process and were validated with the use of a wide range of measurements. The results show that both a single recording channel and correction blocks occupy about  $0.061 \text{ mm}^2$  of the area and consume only  $8.5 \mu\text{W}$  of power. The input referred noise is equal to  $4.6 \mu\text{V}_{\text{RMS}}$ . With the use of additional digital circuitry, each of the recording channels may be independently configured. The lower cut-off frequency may be set within the range of  $0.1 \text{ Hz}$ – $700 \text{ Hz}$ , while the upper cut-off frequency, depending on the recording mode chosen, can be set either to  $3 \text{ kHz}$ / $13 \text{ kHz}$  or may be tuned in the  $2 \text{ Hz}$ – $400 \text{ Hz}$  range. The described methods were introduced in the 64-channel integrated circuit. The key aspect of the proposed design is the fact that proposed techniques do not limit functionality of the system and do not deteriorate its overall parameters.

**Key words:** biomedical experiments, noise, multichannel integrated circuits.

## 1. Introduction

There are many different biomedical experiments that involve using advanced electronics for recording biomedical signals [1–4]. These are mainly run to extract valuable information regarding human nervous system with a view to help people either by developing new medicines or artificial implants. Additionally, there is a growing demand for integrated systems recording different biomedical signals to support people in their daily lives [5–10]. The common attribute of abovementioned applications is the fact that they need to be very small, otherwise these could not allow for increasing spatial resolution of the recordings, nor could they be implanted into the body for experiment purposes. Also, there would be little demand on the specific consumer market. Furthermore, depending on the final purpose, these applications should consume very little power (in the order of  $\mu\text{W}$  or even less) so as to allow for utilization of the power provided either by a battery or wireless connection [11]. Also, such systems should allow for recording different species of biomedical signals [12] (see Table 1) from many sites simultaneously (tens/hundreds of recording sites). Finally, recording electronics should have very low input referred noise (IRN) to allow for measurements of very weak input signals (see Table 1).

In order to develop such a system one needs to utilize modern processes for fabrication of integrated electronics. However, the key problem in the design of such a multichannel system for biomedical signals recordings is the fact that its main parameters (i.e. its area occupation, power consumption, IRN or functionality) are in contradiction with each other. For example,

Table 1  
Examples of biomedical signal parameters [12]

Type of Signal	Frequency Band	Amplitudes
Local Field Potential (LFP)	1 Hz–500 Hz	$10 \mu\text{V}$ – $5 \text{ mV}$
Action Potential (AP)	300 Hz–7 kHz	$10 \mu\text{V}$ – $500 \mu\text{V}$
EEG	<1 Hz–100 Hz	$1 \mu\text{V}$ – $10 \mu\text{V}$
ECG	5 Hz–500 Hz	$1 \text{ mV}$ – $10 \text{ mV}$
EMG	20 Hz–1 kHz	$100 \mu\text{V}$ – $10 \text{ mV}$

minimization of power consumption affects the IRN whilst recording channels area minimization may limit the functionality of the system, have adverse effect on the IRN or deteriorate uniformity of its main parameters. Therefore, one needs to propose solutions to both effectively utilize the available power and area budgets, and not to deteriorate other important parameters.

There are many prominent examples of systems that present different approaches for recording channels architecture [3, 6, 13–16]. In this paper, the design of the whole recording path is presented with the emphasis on the methods allowing for minimization of both power and area with no negative influence on other system parameters.

The paper is organized as follows. In Section 2, the design of a recording channel is presented with a special attention paid on its power consumption and area occupation. Section 3 provides information regarding analog multiplexer where techniques for the area and power minimization are also presented. Section 4 looks at the measurement results of designed multichannel recording circuits, while Section 5 provides conclusions.

\*e-mail: kmon@agh.edu.pl

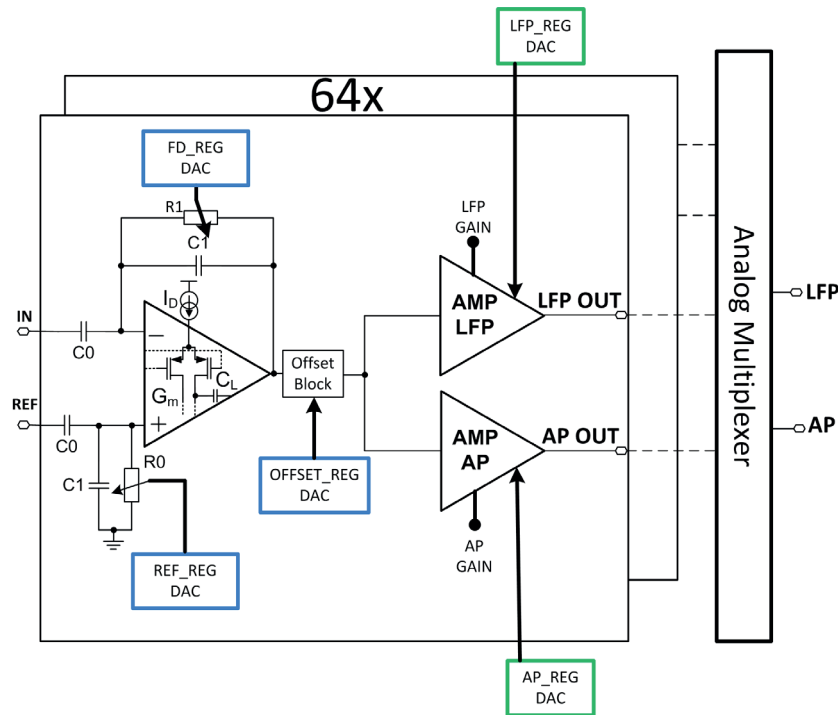


Fig. 1. Schematic idea of the proposed recording channel

## 2. Recording channel

The main task of the recording channel is to perform amplification and filtration of weak input biomedical signals. Additionally, as these signals are conveyed using recording electrodes and there may exist large DC time varying voltage offset, one also needs to protect inputs of the recording stage from that potential to not saturate the amplifier. The above architecture of the recording stage (see Fig. 1) meets the stated requirements. A recording channel is divided into two paths, i.e. for conditioning slow (LFP) and fast (AP) signals as we decided in our former work [17, 18]. The reason for the channel division comes from the fact we wanted to develop an IC capable of simultaneous recording both slow and fast signals. Additionally, these signals may differ in amplitudes (see Table 1) so channel separation and its further individual control allows both to obtain an optimal analog-to-digital conversion and to decrease the amount of transmitted data [17]. Also, the recording channel is digitally assisted in order to minimize its main parameters spread from channel to channel and to adapt it to different experiments. The digital assistance is realized thanks to:

- FD\_REG DAC – local control of the lower cut-off frequency of the recording channel,
- REF\_REG DAC – local control of the symmetry of the preamplifiers inputs (important for improving Common Mode Rejection Ratio),
- OFFSET\_REG DAC – local control to minimize the voltage offsets,
- LFP\_REG DAC – global control of the upper cut-off frequency of the LFP channel,

- AP\_REG DAC – global control of the upper cut-off frequency of the AP channel.

The preamplifier is based on the commonly used stage [13–15] that works with the capacitive feedback. The reason for this amplifier adaptation lies in its architecture, which is attractive in terms of power dissipation, noise, input dynamic range and simplicity of implementation. Furthermore, it has the inherent AC coupling at the input [19]. The voltage gain of this stage is set by the ratio of  $C_0/C_1$  while the lower cut-off frequency is proportional to  $1/(2\pi R_1 C_1)$ . In order to obtain lower cut-off frequencies much below 1 Hz the  $R_1 C_1$  time constant should be very high. Therefore, to minimize the area of this block, the  $R_1$  is based on a PMOS transistor working in subthreshold region (its channel dimensions are  $W/L = 0.4 \mu\text{m}/50 \mu\text{m}$ ) while  $C_1$  has been made as a MIM (metal-insulator-metal) capacitor. The upper cut-off frequency is proportional to  $G_m/C_L$  ratio ( $G_m$  is preamplifiers' transconductance and  $C_L$  is its loading capacitance – see Fig. 1). In order to record different biomedical signals the ability to control both voltage gain and frequency bandwidth needs to be provided to its recording stage also. Here, the lower cut-off frequency is set in the preamplifier stage by an 8-bit DAC (FD\_REG) that changes  $R_1$  resistance. This setting is independent in each of the channels (8-bit DAC is a local block located in the channel) so the user can set lower cut-off frequencies independently of other channels. The voltage gain of a particular path of the recording stage is controlled with the channel independent inputs LFP\_GAIN and AP\_GAIN. Additionally, to record different signals in the LFP and AP path the user can change upper cut-off frequency of this blocks with the use of 6 bit DACs (LFP\_REG and AP\_REG respectively) – that part of the control is global.

**2.1. Design of the first stage.** It is well known that it is mainly the preamplifier that defines the IRN performance of the whole recording channel. Electronic stages that follow the preamplifier operate with already filtered and amplified signals, therefore their noise contribution may be assumed as irrelevant. Thus, the following part of the article refers solely to the IRN of the preamplifier in term of its influence on the area occupation and power consumption of the whole recording channel.

Having looked at the preamplifier schematic idea (see Fig. 1) one can clearly see that its overall IRN is a contribution of two main components, i.e. noise of the core of the amplifier and the noise of resistors  $R_0$ ,  $R_1$ . Because in the described design, a CMOS process was selected (mainly because of its relatively low cost production and fabrication accessibility) the amplifier's core noise is a product of two components, i.e. thermal and  $1/f$  flicker noise. Therefore, the relation of the amplifier's IRN can be written as

$$IRN = \sqrt{IRN_{TH}^2 + IRN_{1/f}^2 + IRN_R^2}, \quad (1)$$

where  $IRN_{TH}$  and  $IRN_{1/f}$  are thermal and flicker input referred noise components of the preamplifier's core and  $IRN_R$  is the input referred noise generated by the resistors  $R_0$ ,  $R_1$ .

To illustrate the influence of the preamplifier on its area and power consumption the following assumptions were taken into account. The area occupation of a single recording channel was equal to the area of the employed capacitors as most of current technologies allow for placing capacitors above active circuitry (i.e. the core of the preamplifier is placed below the capacitors). The capacitance/area ratio was assumed to  $c = 1$  fF/ $\mu\text{m}^2$  (it is a reasonable assumption for most available technologies). Therefore, the total area occupied by the recording channel was about  $2(C_0 + C_1)/c$ , which may be assumed as  $2C_0/c$  (because normally the  $C_0 \gg C_1$ ).

As it comes to the core of the preamplifier, it was assumed that the input transistors of differential pair work in the weak inversion region (its transconductance is equal to  $g_m = I_D/(n_s \varphi_T) - n_s$  is the subthreshold slope factor usually in the range of 1.1–1.3,  $\varphi_T$  is thermal voltage,  $I_D$  is a current sourcing preamplifier) and that they are the major noise contributors of this block.

Having these in mind, one can write the formulas for both thermal and  $1/f$  noise components of the preamplifier [20]:

$$\frac{dv_{TH}^2}{df} = 8kT \frac{\gamma}{g_m} = \frac{4qn_s \varphi_T^2}{I_D} \quad (2)$$

and

$$\frac{dv_{1/f}^2}{df} = \frac{2K_F}{WLC_{ox}} \frac{1}{f}, \quad (3)$$

where  $K_F$  is the flicker noise coefficient,  $C_{ox}$  is the oxide capacitance per input transistor channel area,  $f$  is the frequency,  $\gamma = 0.5$  in weak inversion and  $W$ ,  $L$  are channel dimensions of input transistors.

Below, equations regarding particular noise contributions are given. The starting formulas are presented which are followed by the final equations that may be used to easily count a IRN. Calculation details were earlier presented and may be found in [21].

The thermal noise component is given by the following formula:

$$IRN_{TH\_MIN} = \sqrt{\int_{f_{Low}}^{f_{High}} \left( \frac{C_0 + C_1 + C_{in}}{C_0} \right)^2 \overline{dv_{TH}^2} df} \approx \approx 2.85 \times 10^{-11} \sqrt{\frac{f_{High} - f_{Low}}{I_D}}, \quad (4)$$

where  $C_{in}$  is the input capacitance of the preamplifier,  $f_{High}$  and  $f_{Low}$  are upper and lower cut-off frequencies of the amplifier.

The flicker noise component is given with the following equation:

$$IRN_{1/f} = \sqrt{\int_{f_{Low}}^{f_{High}} \left( \frac{C_0 + C_1 + C_{in}}{C_0} \right)^2 \overline{dv_{1/f}^2} df} \approx \approx 2 \sqrt{\frac{2}{3} \frac{K_F}{C_0} \ln \frac{f_{High}}{f_{Low}}}. \quad (5)$$

The input referred noise generated by the  $R_0$ ,  $R_1$  resistors is defined by:

$$IRN_R = \frac{C_1}{C_0} \sqrt{2 \frac{kT}{C_1}}, \quad (6)$$

where  $k$  is Boltzmann constant,  $T$  is temperature.

Finally, in order to calculate the overall IRN (1) of the preamplifier one has to take into account (4), (5) and (6). However, it should be pointed out that whenever the  $1/f$  noise is minimized the  $C_{in}$  is equal to  $(C_0 + C_1)$ . Therefore, the  $IRN_{TH}$  becomes higher  $\sqrt{2}$  times than the  $IRN_{TH\_MIN}$ . For that reason the overall IRN can be written as

$$IRN = \sqrt{(\sqrt{2} \times 2.85 \times 10^{-11} \sqrt{\frac{(f_{High} - f_{Low})}{I_D}})^2 + (2 \sqrt{\frac{2}{3} \frac{K_F}{C_0} \ln \frac{f_{High}}{f_{Low}}})^2 + (\frac{C_1}{C_0} \sqrt{2 \frac{kT}{C_1}})^2}. \quad (7)$$

It can be seen that the overall IRN depends strongly on the recording channel's frequency band and the chosen IC fabrication process (component  $K_F$  vary with CMOS technology [22–25]). Also, power consumption (represented by  $I_D$ ) and area occupation (represented by capacitors  $C_0$ ,  $C_1$ ) has a significant influence on the IRN. Figure 2 presents how area, power, and the  $K_F$  parameter influence the overall IRN. For that analysis the amplifier was set to record both the LFP and AP signals, i.e. its bandwidth was set to 0.1 Hz–7 kHz with its voltage gain at 100 V/V.

For instance, if the area of the preamplifier is very small, i.e.  $50 \times 50 \mu\text{m}^2$ , and a process with  $K_F = 22,5 \times 10^{-25}$  J is se-

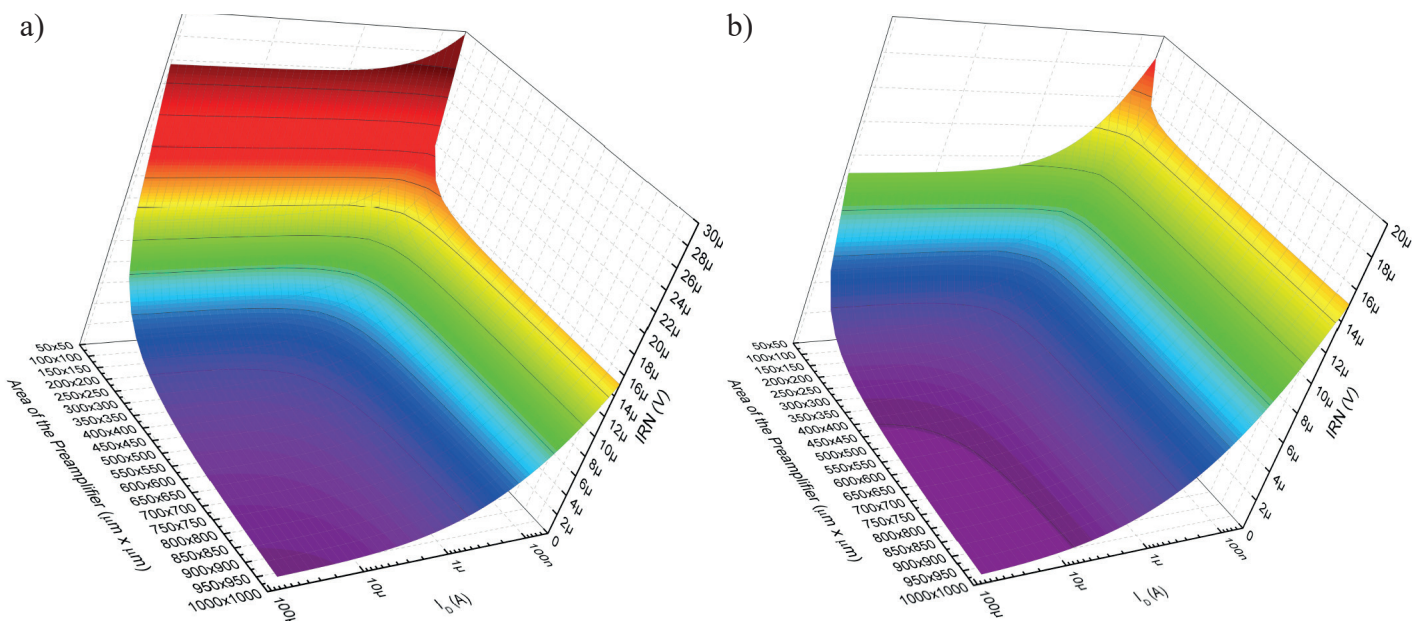


Fig. 2. Preamplifier's area occupation and power consumption influence on the IRN for: a)  $K_F = 22.5 \times 10^{-25}$  J, b)  $K_F = 2 \times 10^{-25}$  J

lected, one cannot decrease the IRN below  $26 \mu\text{V}_{\text{RMS}}$  by using additional current  $I_D$ . This is because for very small area,  $1/f$  noise starts to dominate and this component cannot be minimized adding power. However, the  $1/f$  noise contribution may be decreased by using the CMOS process with lower  $K_F$  coefficient (see Eq. 7). If the  $K_F = 2 \times 10^{-25}$  J and the same area is considered the IRN can be decreased to  $15 \mu\text{V}_{\text{RMS}}$  with additional current. On the other hand, for a large pixel area (in the region of  $1000 \times 1000 \mu\text{m}^2$ ), the noise cannot be lower than  $1.3 \mu\text{V}_{\text{RMS}}$  (for  $K_F = 22.5 \times 10^{-25}$  J) and  $0.6 \mu\text{V}_{\text{RMS}}$  (for  $K_F = 2 \times 10^{-25}$  J) even if the current sourcing the preamplifier is over  $100 \mu\text{A}$ . This phenomenon is the reason of  $1/f$  noise and noise contributed by resistors  $R_0$  and  $R_1$ .

Additionally, one should keep in mind that area minimization may also be limited by the lower cut-off frequency of the preamplifier. Keeping the same voltage gain of the preamplifier ( $C_0/C_1 \approx \text{const.}$ ), if the silicon area is reduced, both capacitances must be reduced. Namely, the smaller the area of the preamplifier, the smaller  $C_1$  is, which means that there is a need to introduce extremely high resistances occupying small area in order to keep proper  $R_1C_1$ . This, however, results in other difficulties combined with current leakages of the CMOS processes and the need to introduce these resistances with good channel-to-channel uniformity [26]. Here, a PMOS transistor is used whose channel dimensions are  $W/L = 0.4 \mu\text{m}/50 \mu\text{m}$ . To control the lower cut-off frequency and minimize its channel-to-channel spread, the 8-bit DAC (FD\_REG) is used. Additionally, in order to reduce leakage current influence, the voltage offset minimization block is used that is controlled by the DAC OFFSET\_REG (see Fig. 1). This results from the fact that if the  $R_1$  is set very high, small leakage currents of the preamplifier inputs [26] generate voltage drop on  $R_1$ , finally shifting the DC voltage at the recording channel outputs.

Having in mind area budget destined to preamplifier it was fitted into  $200 \times 200 \mu\text{m}^2$  of area. It resulted in the capacitors  $C_0 = 10 \text{ pF}$  and  $C_1 = 0.2 \text{ pF}$ . The channel dimensions of input transistors are  $W/L = 400 \mu\text{m}/0.75 \mu\text{m}$ , while the preamplifier is sourced by  $I_D = 3.3 \mu\text{A}$ .

**2.2. Design of the second stage.** The purpose of the second stage is to amplify output signals of the preamplifier to meet input compliance voltage of the analog-to-digital converter that will be combined with slow and fast outputs stages. Moreover, there is also the need to control upper corner frequency to allow for different signals recordings (see Table 1). This control should cover broad frequency range to extract particular biomedical signal components.

Both, the AP and LFP amplifier cores are based on the similar two-stage amplifier presented in Fig. 3. It is a popular am-

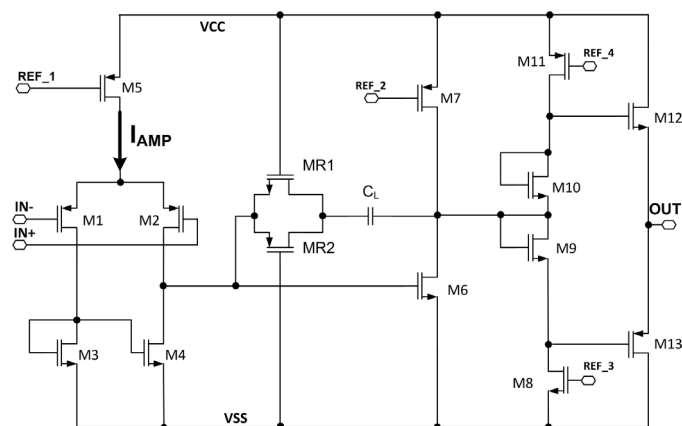


Fig. 3. Schematic idea of the amplifier used as the core of the AP and LFP stages



plifier consisting of an input differential pair followed by the common source amplifying stage. The amplifier has a push-pull output stage as it will drive long routing lines conducting analog signals to the multiplexer. Because the upper cut-off frequency of the AP and LFP blocks is proportional to  $I_{AMP}/C_L$  and it has different values (see Table 1), the  $I_{AMP}$  and  $C_L$  were appropriately set in each of these blocks.

The AP stage works with capacitive feedback while the LFP stage with resistive feedback (see Fig. 4). The user can change voltage gains of these blocks individually in each of the recording channels, i.e. voltage gain of the LFP can be set to 4 V/V or 7 V/V, while AP to 10 V/V or 20 V/V. Moreover, the AP stage allows to tune its lower cut-off frequency to further minimize undesired low frequency components. That control is based on the MOS transistor  $M_{F4}$  (its channel dimensions are  $W/L = 0.4 \mu\text{m}/50 \mu\text{m}$ ) working as a tunable resistor. In order to keep transistors'  $M_{F4}$  gate-source drop-out voltage constant the voltage shifter is used [18].

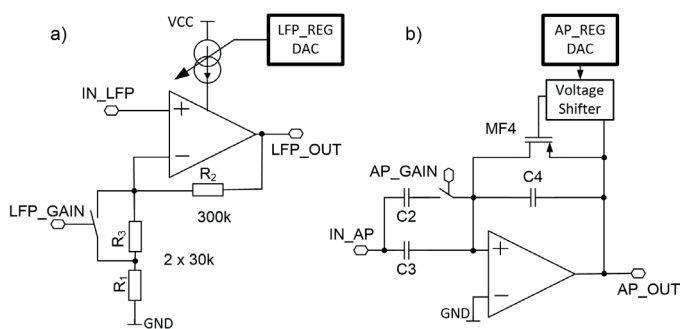


Fig. 4. Schematic idea of the amplifier used in a) LFP and b) AP stage

Since the upper cut-off frequency of the amplifier is proportional to  $I_{AMP}/C_L$  (see Fig. 3), the simplest way to its control is to change either the sourcing current of the amplifier  $I_{AMP}$  or loading capacitance  $C_L$ . The former option, however, seems better as the capacitances may occupy a lot of area. Still, this method causes two main problems. Firstly, changing  $I_{AMP}$  one may also influence other important parameters of the amplifier, such as open loop gain or noise performance. Secondly, the minimum  $I_{AMP}$  level is limited by the transistor leakage currents. The first of the disadvantages mentioned is not a case here, because the LFP amplifier adds no more than 7 V/V, so even if the amplifier's open loop gain changes with  $I_{AMP}$ , there will still be enough gain not to introduce considerable amplification error. Additionally, the noise degradation with  $I_{AMP}$  reduction is also not an issue as the LFP amplifier is preceded by the high gain low noise preamplifier (see Fig. 1).

We investigated the problem of bottom  $I_{AMP}$  limits in our former work [18]. The  $I_{AMP}$  was controlled by the 6-bit DAC and in that way the upper cut-off frequency was modified. However, during the measurements we encountered a large discrepancy between simulations and real results of the frequency bandwidth control range. Fig. 5 shows the upper cut-off frequency measurement results versus the 6-bit DAC setting. As it can be seen there is no way of decreasing the upper

cut-of frequency below about 150 Hz with the DAC. It is worth noting that simulation results of the same controlling approach showed it is possible to obtain the upper cut-off frequency at 10 Hz.

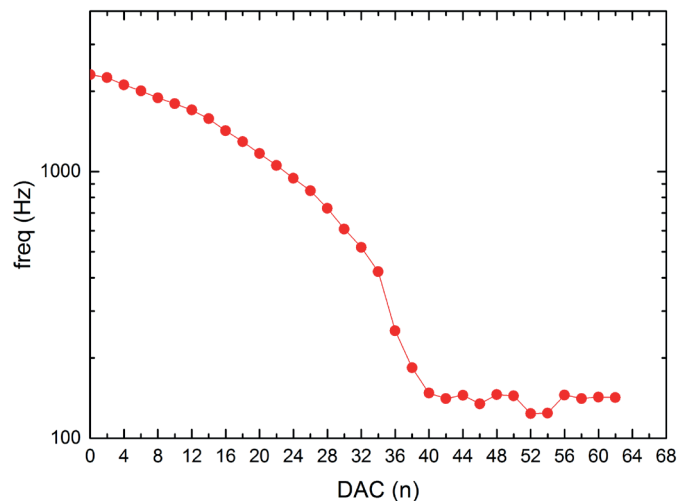


Fig. 5. Measurement results of the upper cut-off frequency of the prototype LFP amplifier

A possible solution of that problem would be increasing the  $C_L$  of the amplifier. However, for the presented measurements one should increase the  $C_L$  value about fifteen times to get similar results to those achieved in simulations, i.e. the area of the LFP stage would increase by the same value. However, this solution is not acceptable due to too much area occupation.

The reason of the abovementioned discrepancies comes from the fact the leakage currents of the transistors working as current mirrors (see  $M_3$ – $M_5$  in Fig. 3) were not properly modeled within library files. Namely, even if the DAC was completely turned off, that is the  $I_{AMP}$  was set to zero, there was still current (a product of leakage currents) that was sourcing amplifier. In order to minimize that effect, the core of the amplifier was changed. Leaky transistors ( $M_3$ – $M_5$ ) were exchanged with transistors of thicker gate oxide with operating voltage at 3.3 V (previous transistors were destined to 1.8 V). It is worth noting that their gate oxide is 1.74 times thicker than those counterparts destined to 1.8 V supply voltage and new transistors have 30 times lower leakage currents.

Finally, the upper cut-off frequency of the AP and LFP were set by loading capacitance  $C_L$  and current  $I_{AMP}$  as shown in Table 2.

Table 2  
AP and LFP core configuration

Recording Block	$C_L$ (F)	$I_{AMP}$ (A)
LFP	2.5 p	60 p–14 n
AP	1 p	220 n

### 3. Analog Multiplexer

In order to limit the IC lines coming from the recording channels outputs, one needs to utilize the analog multiplexer. In that way, the  $n$  lines may be directed to a single output that is switched among the  $n$  multiplexer's inputs (see Fig. 6). The multiplexer should be equipped with voltage buffers to minimize channel kick back noise of the recording and to properly steer long routing lines.

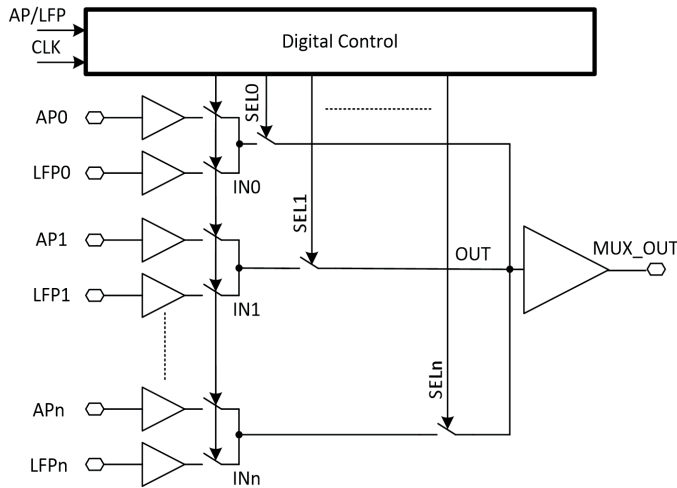


Fig. 6. Block idea of the analog multiplexer applied in the presented project

During the multiplexer design following aspects were taken into account:

- area and power constraints,
- voltage swing of the signal, both at the input and output of the multiplexer,
- sampling frequency of each channel defining the frequency of the clock controlling the multiplexer.

**3.1. Design of the analog multiplexer.** Taking into account the recording channel frequency bandwidth requirements, the sampling frequency of the multiplexer was chosen to be  $f_s = 40$  kHz to avoid aliasing issues. As a result, the switching frequency of the consecutive  $n$  channels of the global multiplexer is  $n \times f_s$ .

Considering the clock frequency of the multiplexer, one should also keep in mind that the lines conducting the analog signals within the multiplexer may constitute considerable parasitics (both the capacitance and resistance). This may pose limits in decreasing both, the area and power of a multiplexer block.

Having the above in mind, a possible option for voltage buffer used as a multiplexer's core is to use a rail-to-rail input/output trans-impedance amplifier. In that way, the voltage swing will be high and the output resistance will be sufficiently low to work with parasitic capacitances that have to be recharged within a short time. However, this solution cannot be applied in the following project because of substantial area occupation.

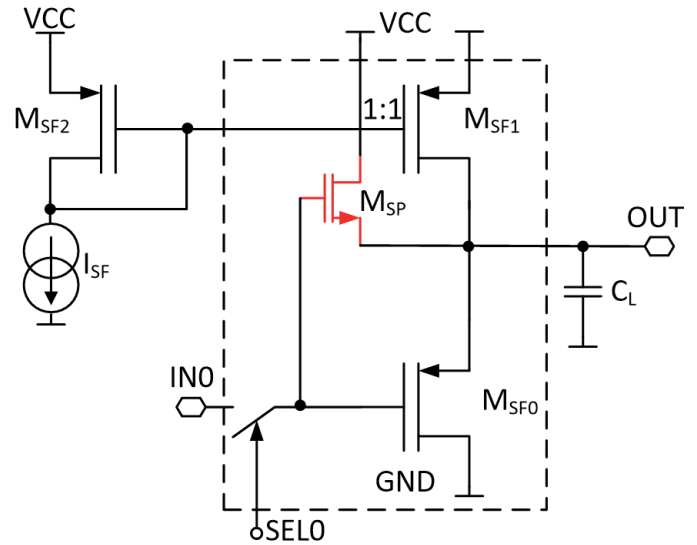


Fig. 7. Schematic idea of the analog buffer employed in the multiplexer

Therefore, the source follower with the proposed modification was introduced as the multiplexer's buffer (see transistor  $M_{SP}$  in Fig. 7). It is used as a sampling circuit of signals provided either by AP or LFP blocks (see Fig. 6). The main reason for the source follower adaptation is its simplicity and small area occupation. Its main disadvantages are input/output voltage swing depending on biasing conditions and  $I_{SF}$  current while working with capacitive loads. Let us analyze the voltage buffer in terms of the abovementioned multiplexer requirements. One may notice that both the input and output voltage swing are equal and may be given as:

$$V_{IN\_MAX} - V_{IN\_MIN} = V_{OUT\_MAX} - V_{OUT\_MIN} = V_{CC} - V_{DSAT\_MSF1} - V_{GS\_MSF0}, \quad (8)$$

where  $V_{DSAT}$  is saturation voltage of the  $M_{SF1}$  based current source,  $V_{GS}$  is gate-source voltage of the  $M_{SF}$  transistor. Both of these voltages depend on the source follower biasing condition which is given by the following formula:

$$V_{DSAT\_MSF1} = \sqrt{\frac{2I_{SF}L_{MSF1}}{\mu C_{OX}W_{MSF1}}}, \quad (9)$$

where  $\mu$  is carrier mobility.

Next,

$$V_{GS\_MSF0} = \sqrt{\frac{2I_{SF}L_{MSF0}}{\mu C_{OX}W_{MSF0}}} + V_{TH\_MSF0}, \quad (10)$$

where  $V_{TH}$  is threshold voltage of the transistor  $M_{SF0}$ .

Furthermore, in terms of a fast operation of the source follower a main limit comes from the drain current of the  $M_{SF1}$  current source. Let us assume that the output DC difference voltage of the neighboring channels is 1 V. Additionally, let us consider that due to the off-chip controller requirements, the

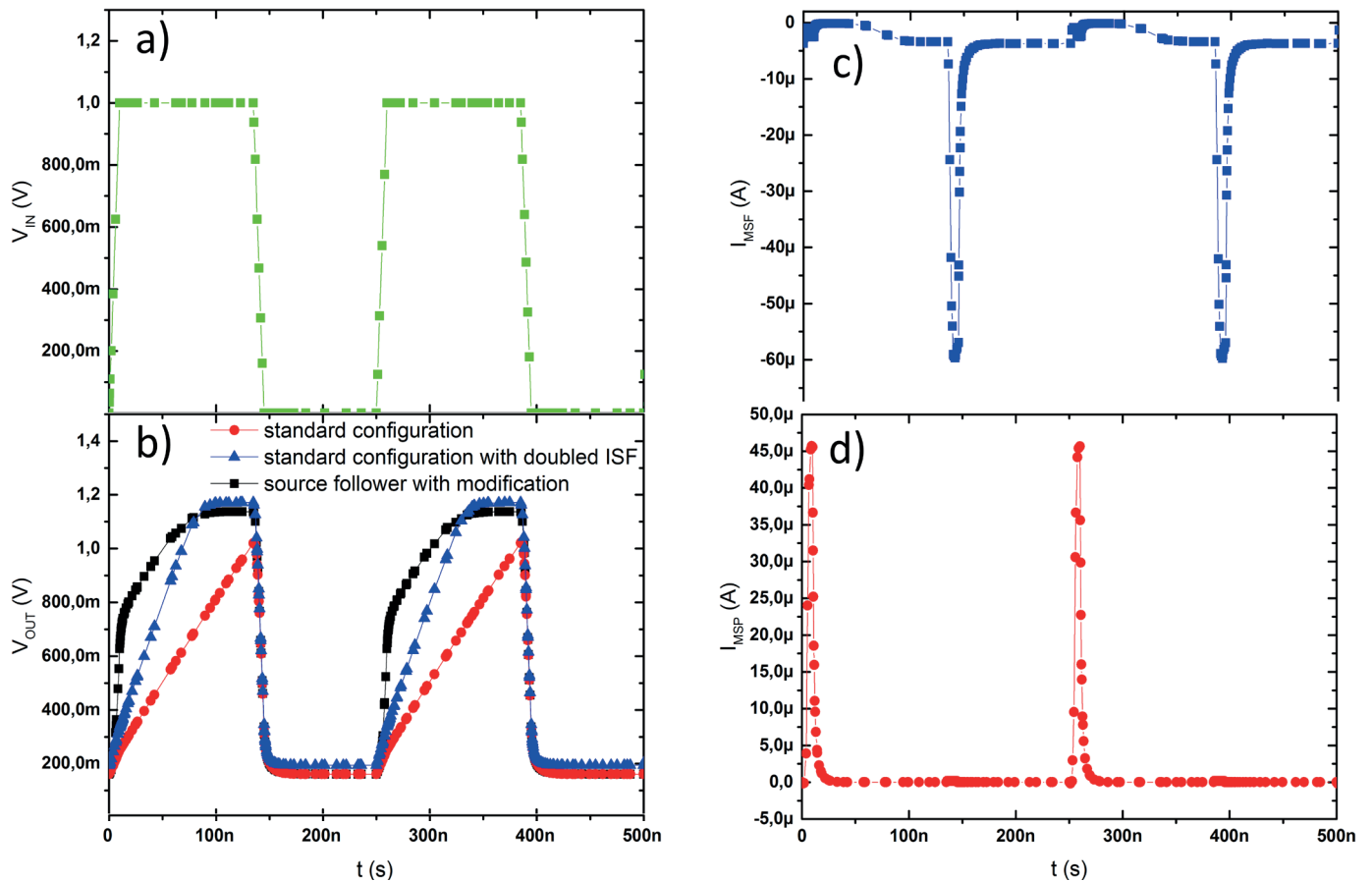


Fig. 8. Simulation results of the source follower: a) input voltage, b) output voltage for different source follower configurations, c) current of the  $M_{SF}$  transistor, d) current of the  $M_{SP}$  transistor

output voltage of the multiplexer has to be set at  $0.25 \times (2/f_s)$  before multiplexer switches to the next channel. Considering 40 MHz clock frequency, it is about 40 ns before switching to the next channel. Supposing the  $C_L$  is charged to 1 V and a 0 V is applied to the input of the source follower, the capacitor is discharged via low output resistance of the  $M_{SF0}$  transistor (it is equal to  $1/g_{mMSF0}$ , where  $g_{mMSF0}$  is  $M_{SF0}$  trans-conductance). On the other hand, if the loading capacitance is charged from 0 V with current  $I_{SF}$ , then the  $M_{SF0}$  is cut off until capacitor voltage becomes high enough to switch  $M_{SF0}$  on. In order to minimize that time the  $I_{SF}$  can be increased or the  $C_L$  decreased, which is not the case in this project. Therefore, a source follower voltage buffer modification is presented. It is based on using an additional transistor  $M_{SP}$  (see Fig. 7) named a supporting transistor. Its role is to inject an extra current to increase the speed of the capacitor charging and in that way to decrease the time with the  $M_{SF0}$  being switched off. As a result, a  $I_{SF}$  current may be decreased while operating with the same loading capacitance. The important thing is that under normal  $M_{SF0}$  working condition, i.e. while it is conducting current, the gate-source drop-out voltage of  $M_{SF0}$  transistor switches off the supporting transistor.

Simulation results of the proposed modification are presented in Fig. 8. One can see three different source follower configurations. Based on the post layout simulations, for

a given routing lines, their parasitic capacitance  $C_L$  is assumed to be 500 fF. The first solution is a basic construction with  $I_{SF} = 3.7 \mu\text{A}$ . It can be seen that charging phase is too slow to finish before the next channel readout is started. The second option is also based on the standard configuration but with two times higher  $I_{SF}$ , i.e. equal to  $7.4 \mu\text{A}$ . It can be seen that in this scenario, the output voltage settling time is acceptable. Finally, the last option uses a supporting transistor and  $I_{SF} = 3.7 \mu\text{A}$ . As it can be noticed, the capacitors charging phase becomes twice faster and its speed is equal to standard configuration with doubled  $I_{SF}$ . Figure 8 shows the transients of the currents of both  $M_{SF0}$  and  $M_{SP}$  transistors where additional current injections of  $M_{SP}$  are clearly visible. In that way, both, the area and power of the voltage buffer are significantly decreased. For a given project, channel dimensions of the  $M_{SF0}$  and  $M_{SP}$  transistors are equal to  $W/L = 20 \mu\text{m}/0.24 \mu\text{m}$  and  $W/L = 5 \mu\text{m}/0.5 \mu\text{m}$  respectively.

#### 4. Measurement results

The described techniques were utilized in the recording channel being a part of the large IC processed in the CMOS 180nm technology. The IC consists of 64 recording channels followed

by an analog multiplexer. Figure 9 shows the percentage of a particular block's area occupation and power consumption. As it can be seen, the preamplifier is a block that uses large amount of the available power and area budget.

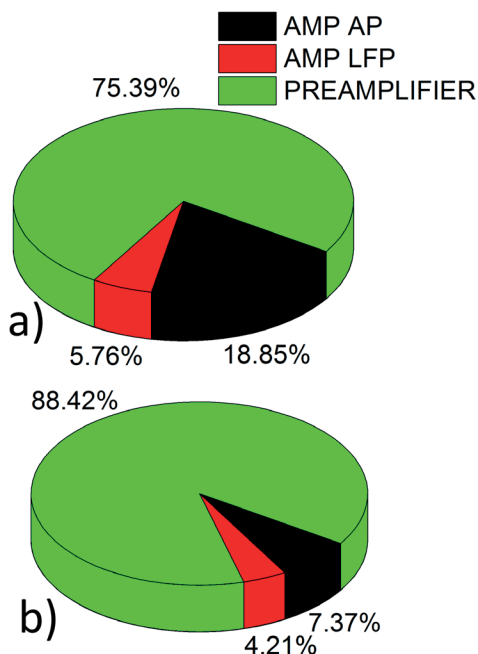


Fig. 9. The percentage of the area occupation a) and power consumption b) of particular recording channel blocks

The upper cut-off frequency of the LFP stage was measured (see Fig. 10). As it can be seen there is a considerable improvement of the frequency controlling range (see Fig. 5 for comparison). Here, the lowest upper cut-off frequency is improved almost eighty times with no expense on additional area occupation.

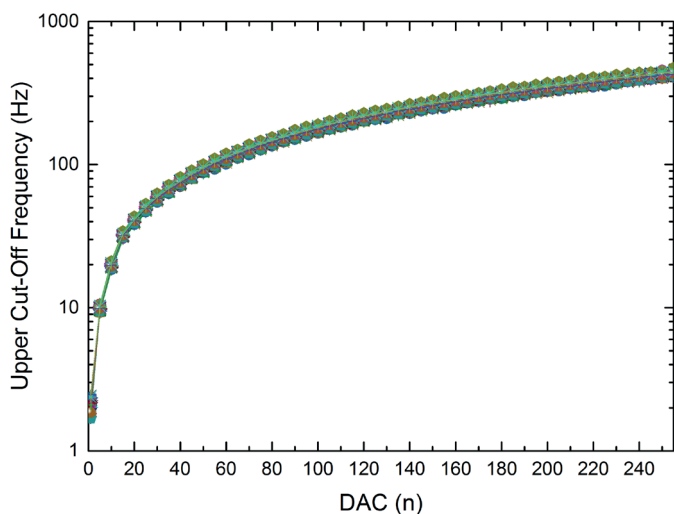


Fig. 10. Upper cut-off frequency vs. DAC for the LFP stage of 64 recording channels.

A single recording channel has a large functionality thanks to its input signal division into two paths and extra circuitry (independent digital control and DACs) responsible for controlling channel's main parameters (see Fig. 1). The proposed channel architecture allows to configure a particular channel for different signal recordings (see Table 1). As for the LFP stage, its voltage gain can be switched to 130 V/V or 240 V/V while for the AP stage, it may be set either to 340 V/V or 700 V/V. The lower cut-off frequency may also be set independently for a particular channel in the range of 0.1 Hz–700 Hz, while the upper cut-off frequency of the LFP stage can be controlled in the 2 Hz–400 Hz.

Additionally, thanks to the correction circuits (see Fig. 1) one can perform minimization of the main parameters spread. Figure 11 presents transfer characteristics of the recording channel before and after correction. The correction was done with the use of FD\_REG DAC (see Fig. 1). Results show that the standard deviation of the lower cut-off frequency was reduced from 0.32 Hz to 0.022 Hz (about 14 times).

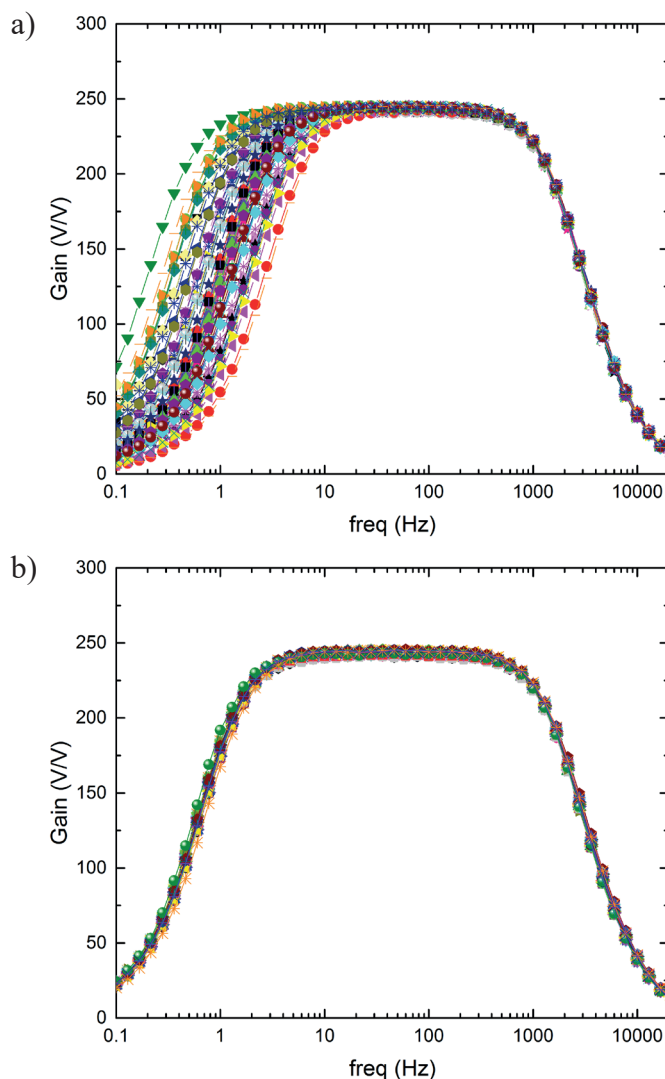


Fig. 11. Frequency response of the recording channel: a) before, b) after lower cut-off frequency calibration



The IRN of the recording channel was also measured at both channel outputs (see Fig. 12). The bandwidth of the AP stage was configured to 300 Hz–13 kHz, the voltage gain was set to 340 V/V, which resulted in 4.6  $\mu\text{V}$  of the IRN. The bandwidth of the LFP stage was configured to 1 Hz–300 Hz, voltage gain was set to 130 V/V which resulted in 4.7  $\mu\text{V}$  of IRN.

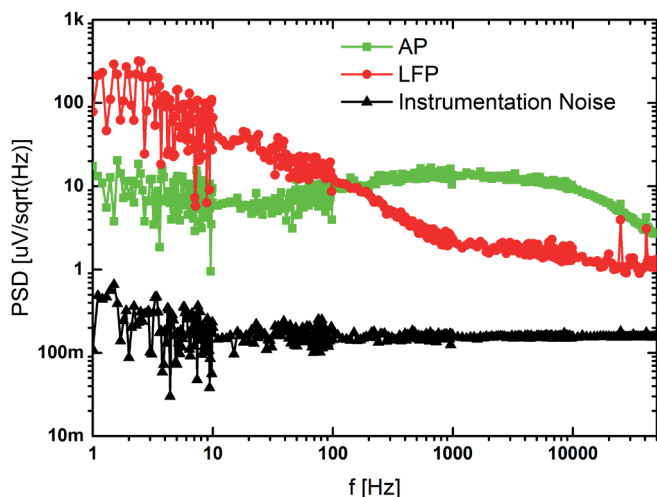


Fig. 12. Power spectrum density measured at LFP and AP outputs

The presented recording channel was compared to other works [27–30] in terms of its current consumption and area occupation.

In order to minimize the process influence on the comparison (see Eq. 5), only works with similar processes, i.e. CMOS 180 nm were taken into account. It can be seen that the recording channel presented in [28] has one of the best parameters. Still, the work presented in this paper has larger functionality, i.e., it allows for individual recording channels parameter setting in a broad range. Additionally, compared to these works, the presented solution also performs well in terms of power consumption and area occupation.

## 5. Conclusions

The paper presents techniques that were introduced in the design of multichannel recording circuits dedicated to biomedical experiments to minimize power consumption and area occupation. The most important aspect of the recording channel's path is to concentrate efforts on preamplifier design as it consumes a major part of power and area budgets. It was pointed out that the area, power and chosen CMOS processes have significant influence on power and area minimization of the recording channel. The paper also shows limits combined with leakage currents regarding modern CMOS processes. An example of minimizing this problem with the use of thick oxide transistors is presented. Finally, a modification of a simple source follower based buffer is proposed. Thanks to additional transistor supporting the loading capacitance recharging phase, a reduction of

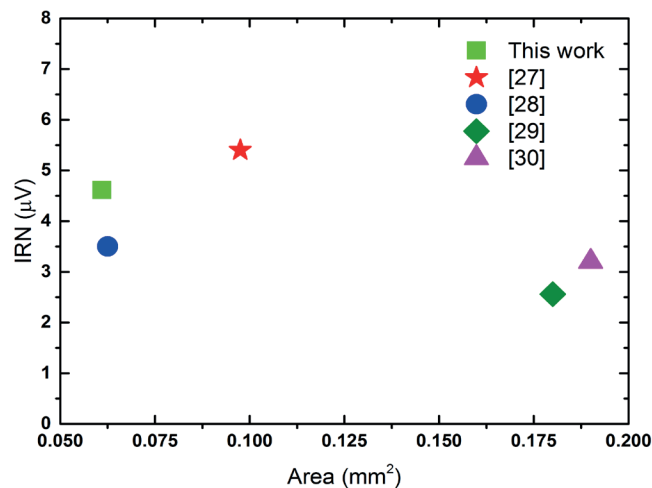


Fig. 13. Comparative analysis of recording channels in terms of area occupation

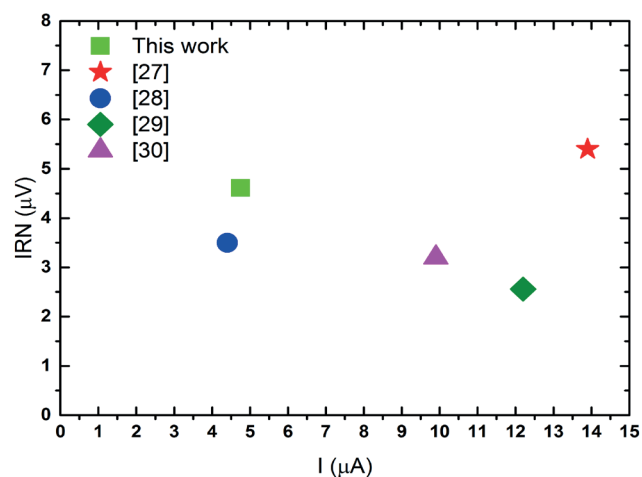


Fig. 14. Comparative analysis of recording channels in terms of current consumption

area and power was achieved. The proposed techniques adapted in the IC allowed for successful verification of measurements. The main IC parameters are very attractive for systems requiring recordings of different biomedical signals.

**Acknowledgements.** This research and development project was granted support by Polish Ministry of Science and Higher Education in 2015. The author acknowledges the support of Prof. P. Gryboś and Prof. R. Szczygieł by a helpful discussion, as well as the support of M. Żołądź and A. Lisicka during IC measurements.

## REFERENCES

- [1] E. Doi, J. L. Gauthier, G. D. Field, J. Shlens, A. Sher, M. Gerschner, T. A. Machado, L. H. Jepson, K. Mathieson, D. E. Gunning, A. M. Litke, L. Paninski, E. J. Chichilnisky, and E. P. Simoncelli, "Efficient coding of spatial information in the primate retina", *The Journal of Neuroscience*, 32(46), 16256–16264 (2012).

- [2] L. R. Hochberg, D. Bacher, B. Jarosiewicz, N. Y. Masse, J. D. Simeral, J. Vogel, S. Haddadin, J. Liu, S. S. Cash, P. van der Smagt, and J. P. Donoghue, "Reach and grasp by people with tetraplegia using a neurally controlled robotic arm," *Nature*, 485, 372–375 (2012).
- [3] M. Ballini, J. Müller, P. Livi, Y. Chen, U. Frey, A. Stettler, A. Shadmani, V. Viswam, I. L. Jones, D. Jäckel, M. Radivojevic, M. K. Lewandowska, W. Gong, M. Fiscella, D. J. Bakum, F. Heer, A. Hierlemann, "A 1024-channel CMOS microelectrode array with 26,400 electrodes for recording and stimulation of electrogenic cells in vitro", *IEEE Journal of Solid-State Circuits*, 49(11), 2705–2719 (2014).
- [4] A. F. Johnstone, G. W. Gross, D. G. Weiss, O. H. Schroeder, A. Gramowski, T. J. Shafer, "Microelectrode arrays: a physiologically based neurotoxicity testing platform for the 21st century", *Neurotoxicology*, 31(4), 331–350(2010).
- [5] Y. H. Chen, M. O. de Beeck, L. Vanderheyden, E. Carrette, V. Mihajlović, K. Vanstreels, B. Grundlehner, S. Gadeyne, P. Boon, Ch. V. Hoof, "Soft, comfortable polymer dry electrodes for high quality ECG and EEG recording", *Sensors*, 14(12), 23758–23780(2014).
- [6] N. V. Helleputte, M. Konijnenburg, J. Pettine, D. W. Jee, H. Kim, A. Morgado, R. V. Wegberg, T. Torfs, R. Mohan, A. Breeschoten, H. de Groot, Ch. V. Hoof, R. F. Yazicioglu, "A 345  $\mu$ W multi-sensor biomedical SoC with bio-impedance, 3-channel ECG, motion artifact reduction, and integrated DSP", *IEEE Journal of Solid-State Circuits*, 50(1), 230–244(2015).
- [7] L. Yan, P. Harpe, V. R. Pamula, M. Osawa, Y. Harada, K. Tamaya, Ch. V. Hoof, R. F. Yazicioglu, "A 680 nA ECG acquisition IC for leadless pacemaker applications", *IEEE Transactions on Biomedical Circuits and Systems*, 8(6), 779–786(2014).
- [8] F. G. Zeng, S. Rebscher, W. V. Harrison, X. Sun, H. Feng, "Cochlear implants: system design, integration and evaluation", *IEEE Review Biomedical Engineering, IEEE Reviews in Biomedical Engineering*, 1, 115–142(2008).
- [9] J. D. Weiland, M. S. Humayun, "Visual prosthesis", *Proceedings of the IEEE*, 96(7), 1076–1084(2008).
- [10] J. Xu, R. Yazicioglu, B. Grundlehner, P. Harpe, K. A. A. Makinwa, C. V. Hoof, "A 160 W 8-channel active electrode system for EEG monitoring," *IEEE Transactions on Biomedical Circuits and Systems*, 5(6) 555–567(2011).
- [11] P. Harpe, H. Gao, R. V. Dommele, E. Cantatore, A. V. Roermund, "A 3nW signal acquisition IC integrating an amplifier with 2.1 NEF and a 1.5fJ/conversion-step ADC", *Proceedings of the ISSCC 382* (2015).
- [12] R. F. Yazicioglu, P. Merken, R. Puers, Ch. V. Hoof, "A 60 $\mu$ W 60nV/ $\sqrt{\text{Hz}}$  readout front-end for portable bipotential acquisition systems", *IEEE Journal of Solid-State Circuits*, 42(5), 1100–1110 (2007).
- [13] R. R. Harrison, "The design of integrated circuits to observe brain activity", *Proceedings of the IEEE*, 96(7), 1203–1216(2008).
- [14] A. Rodríguez-Pérez, M. Delgado-Restituto, A. Darie, C. Soto-Sánchez, E. Fernández-Jover, Á. Rodríguez-Vázquez, "A 330 $\mu$ W, 64-Channel neural recording sensor with embedded spike feature extraction and auto-calibration", *Proceedings of the IEEE Asian Solid-State Circuits Conference*, 205–208(2014).
- [15] R. Shulyzki, K. Abdelhalim, A. Bagheri, M. T. Salam, C. M. Florez, J. L. Perez Velazquez, P. L. Carlen, R. Genov, "320-channel active probe for high-resolution neuromonitoring and responsive neurostimulation", *IEEE Transactions On Biomedical Circuits and Systems*, 9(1), 34–49(2015).
- [16] R. Muller, S. Gambini, J. Rabaey, "A 0.013 mm<sup>2</sup>, 5  $\mu$ W, dc-coupled neural signal acquisition IC with 0.5 V supply," *IEEE Journal of Solid State Circuits*, 47(1), 232–243(2012).
- [17] M. Żołądź, P. Kmon, J. Rauza, P. Gryboś, T. Blasiak, "Multichannel neural recording system based on family ASICs processed in sub-micron technology", *Microelectronics Journal*, 45(9), 1226–1231 (2014).
- [18] P. Kmon, "Digitally assisted neural recording and spike detection multichannel integrated circuit designed in 180nm CMOS technology", *Microelectronics Journal*, 45(9), 1187–1193 (2014).
- [19] J. Ruiz-Amaya, A. Rodríguez-Pérez, M. Delgado-Restituto, "A comparative study of low-noise amplifiers for neural applications," *Proceedings of the 2010 International Conference on Microelectronics*, 327–330 (2010).
- [20] P. Gryboś, *Front-end Electronics for Multichannel Semiconductor Detector Systems*, WUT Publishing House, Warsaw, Poland, 2010.
- [21] P. Kmon, "Noise minimization limits in multichannel integrated circuits dedicated to neurobiology experiments", *Microelectronics Journal*, Elsevier, 51, 67–74(2016).
- [22] P. F. Manfredi, M. Manghisoni, L. Ratti, V. Re, V. Speziali, "Resolution limits achievable with CMOS front-end in X- and -ray analysis with semiconductor detectors," *Nucl. Instrum. Methods Phys. Res., A*(512), 167–178(2003).
- [23] P. O. Connor and G. De Geronimo, "Prospects for charge sensitive amplifiers in scaled CMOS," *Nucl. Instrum. Methods Phys. Res., A*(480), 713–725(2002).
- [24] V. Re, M. Manghisoni, L. Ratti, V. Speziali, G. Traversi, "Survey of noise performances and scaling effects in deep submicrometer CMOS devices from different foundries", *IEEE Transactions on Nuclear Science*, 52(6), 2733–2740(2005).
- [25] D. Binkley, *Tradeoffs and Optimization in Analog CMOS Design*, Wiley, 2008.
- [26] P. Kmon, P. Gryboś, "Energy efficient low-noise multichannel neural amplifier in submicron CMOS process", *IEEE Transactions on Circuits and Systems*, 60(7), 1764–1775 (2013).
- [27] B. Gosselin, A. E. Ayoub, J.-F. Roy, M. Sawan, F. Lepore, A. Chaudhuri, D. Guitton, "A mixed-signal multichip neural recording interface with bandwidth reduction," *IEEE Transactions on Biomedical Circuits and Systems*, 3(3), 129–141(2009).
- [28] V. Majidzadeh, A. Schmid, Y. Leblebici, "Energy efficient low-noise neural recording amplifier with enhanced noise efficiency factor," *IEEE Transactions on Biomedical Circuits and Systems*, 5(3), 262–271(2011).
- [29] C. W. Chang, L. C. Chou, P. T. Huang, S. L. Wu, S. W. Lee, C. T. Chuang, K. N. Chen, W. Hwang, K. Hua Chen, C. T. Chiu, H. M. Tong, J. C. Chiou, "A double-sided, single-chip integration scheme using through-silicon-via for neural sensing applications", *Biomedical Microdevices*, 17(1), 1–15(2015).
- [30] C. Mora Lopez, A. Andrei, S. Mitra, M. Welkenhuysen, W. Eberle, C. Bartic, R. Puers, R. F. Yazicioglu, G. Gielen, "An implantable 455-active-electrode 52-channel CMOS neural probe", *IEEE Journal of Solid-State Circuits*, 49(1), 248–261(2014).