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INVESTIGATION OF HEAT TRANSFER IN INTEGRATED CIRCUITS

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Abstract

The paper analyzes the phenomenon of heat transfer and its inertia in solids. The influence of this effect on the operation of an integrated circuit is described. The phenomenon is explained using thermal analogy implemented in the Spice environment by an R-C thermal model. Results from the model are verified by some measurements with a chip designed in CMOS 0.7 µm (5 V) technology. The microcontroller-based measurement system structure and experiment results are described.

Keywords: temperature, heat transfer, VLSI, electric analogy.

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1. Introduction

Continuous scaling down the technology in order to make integrated circuits work faster causes that temperature of the chip silicon die increases. As a result the danger of overheating and damage of the circuit occurs [1] and the meaning of thermal measurements of the integrated circuits is constantly rising [2]. That means that monitoring and controlling chip temperature becomes necessary. Some real-time systems achieving that goal have already been developed [3]. The main aim of the paper is to present, explain and illustrate the case of the thermal inertia phenomenon when the temperature of some parts of the integrated circuit is still rising despite no active heat sources.

Thermal issues in semiconductors were investigated and modeled since the 70's, beginning from single elements [7] to quite complex systems nowadays. As an effect it is a quite well-described area of research. An early concept to model the integrated circuits are R-C networks [8, 9]. Despite their limitations, they are still simple and well-understood by electronic engineers, an approach which can be accurate enough for some applications. For these reasons the RC model will be used in this work.

Some interesting research in the past included dynamics of heat transfer in the circuit [10, 11]. On the other hand, most of the work in late years was focused on creating accurate electro-thermal simulators or thermal modeling of the circuit including its package and leads [9, 12]. The phenomenon of thermal inertia has been noticed before in some applications [13]. Paper [14] investigated thermal inertia considering junction-to-case thermal resistance and thermal capacity of the heat sink. Spatial distribution and dynamics of heat within the silicon die of the integrated circuit including heat transfer inertia is still to be described in detail.

The phenomenon of heat transfer inertia is a quite complex effect. It is obvious that when a power step is dissipated in the integrated circuit then its temperature rises. It is also expected that after the power dissipation stops the temperature would start to drop immediately. In reality, as a result of complex chip structure and non-uniform temperature distribution the temperature of some parts of the circuit can still rise, despite no power source at the moment.

The paper will prove that a simple DPM (Dynamic Power Management) method of control which scales down the power dissipated in the chip to obtain immediate cooling down [4]

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is not always efficient enough and some observation of the temperature dynamics should also be implemented. This assumption is a result of the phenomenon of heat transfer inertia which will be described and visualized in the paper.

Next sections will describe a Spice model created to illustrate the thermal inertia phenomenon. The thermal model [5] is based on well-known analogy between thermal and electrical parameters. In both areas there are similar values, for example resistance and thermal resistance. Consequently, electrical simulators can be used to visualize thermal phenomena and temperature changes can be represented by the value of voltage in a specific node of the electrical circuit. Main parameters of electrical-thermodynamic analogy are gathered in Tab. 1 [6]. This analogy will be used in the presented Spice simulations which are meant as an introduction to the measurements. The presented method of modeling was chosen because it should be easily understood by electronic engineers who can use it in their work with thermally-aware design of integrated circuits.

Table 1. Parameters of electrical-thermodynamic analogy.

THERMODYNAMIC PARAMETER	ELECTRIC PARAMETER
Temperature T [K]	Voltage U [V]
Power P [W]	Current I [A]
Heat Q [J]	Charge q [C]
Thermal resistance R_{th} [K/W]	Resistance R [W=V/A]
Thermal capacitance C_{th} [J/K]	Capacitance C [F=C/V]
Thermal time constant $\tau_{th} = R_{th}C_{th}$ [s]	Time constant $\tau = RC$ [s]

Finally, some experiment results verifying the theory will be presented. Tests were done with an application-specified circuit designed in CMOS 0.7 μm (5 V) technology using a microcontroller-based measurement system and LabView application. Conditions for both simulation and experiment were similar and the gathered results are consistent.

2. Thermal model

The phenomenon of thermal inertia in integrated circuits will be described firstly by a Spice model based on analogy between electrical and thermodynamic parameters which will illustrate the expected thermal behavior of the integrated circuit. The model should explain effects which will be seen in an experiment described in the next section of the paper. The structure of the created model for heat transfer investigation is presented in Fig. 1. Exact values of the model parameters have been chosen to correspond to real-world elements which have thermal time constants of tens of seconds.

Every circuit consists of many different layers and elements. Each of them can be represented by thermal resistance and capacitance. The thermal resistance $R_{i,j_p,q}$ between i,j and p,q nodes of the circuit can be calculated from (1)

$$R_{i,j_p,q} = \frac{l_{i,j_p,q}}{S_{i,j_p,q}\lambda}, \tag{1}$$

where l_{i,j_pq} is the length of the i,j_p,q element, $S_{i,j_p,q}$ is its area and λ is the thermal conductivity of the element layer in [W/mK] [15]. As it is clearly visible this parameter is similar to electrical resistance. Heat is a specific kind of energy which can flow between two points of a solid and is analogous to electric charge. Every node also has its own thermal capacity $C_{i,j}$. Heat transfer can be visualized as currents in the circuit. As a consequence, power dissipated by a specific element can be represented by current source I_{th} connected to a corresponding node. In the presented model a silicon die of area of 1 mm^2 and thickness

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of 700 μm was used, what refers to the circuit tested in the next section. Silicon thermal conductivity $\lambda = 149$ W/mK and volumetric thermal capacity $C_v = 1{,}547$ J/cm^{3}K were the basis for calculation of $R_{i,j_p,q}$ and $C_{i,j}$ elements. Obviously, the assumption of a pure-silicon die comparing to a real situation and the complex structure of the chip is too simplified and the influence of other chip material has to be included into the model since the areas of silicon with diffusion have different thermal conductivities, not to mention the highly resistive polysilicon or metal connective layers. It means that for uniform die division into several sections (according to Fig. 1) a mean value including the influence of many parameters has to be calculated. Values of thermal parameters calculated from the silicon base had to be optimized for precise fitting of the experiment result. Final values are quite close to pure-silicon ones since the silicon occupies the major part of the die volume.

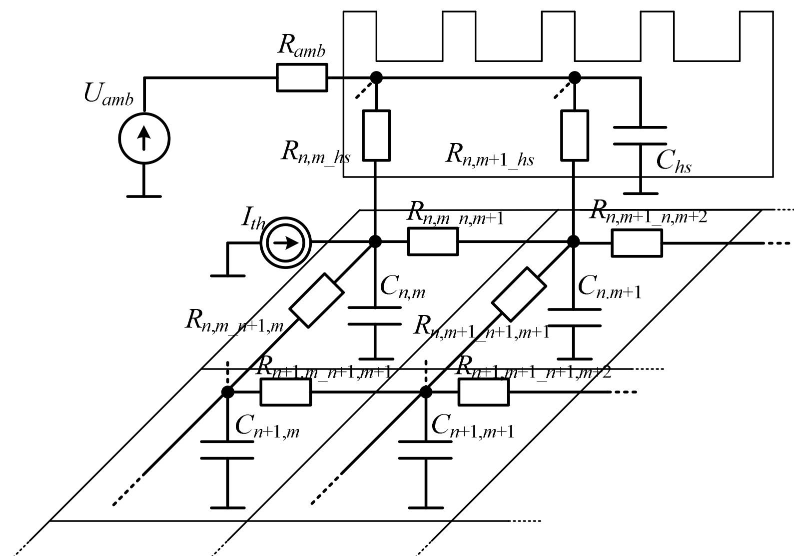

Fig. 1. Schematic diagram of the model for heat transfer investigation.

Additionally, in the presented case the temperature of one side of the circuit is stabilized near ambient temperature by a heat sink. This constant temperature is realized as a DC voltage source U_{amb} connected to the heat sink. Some more attention has to be paid to the heat sink thermal parameters interpretation and calculation. The *hs* (heat sink) node of the circuit has its thermal capacitance C_{hs} and thermal resistance R_{hs}. Since the spatial distribution of these elements is not relevant for the heat distribution on the chip surface, the capacity has been simplified to one element and the resistance was included into resistance between the circuit surface and the *hs* node (which also includes the influence of the thermal grease used) instead of creating an additional net of nodes for the heat sink layer. To obtain values of these elements, absolute values of thermal resistance R_{th} and C_{th} for the complete test chip with and without heat sink have been measured according to (2) and (3):

$$R_{th} = \frac{\Delta T}{P}, \tag{2}$$

$$C_{th} = \frac{\Delta Q}{\Delta T} = \frac{P \Delta t}{\Delta T}. \tag{3}$$

From their difference the values of the heat sink parameters could be deduced and divided into a net of resistors referring to the model structure. In that way the R_{i,j_hs} elements represent all the resistance which is present between the surface of the integrated circuit and the mounted heat sink. Additionally, the parameters of the *hs* node have been verified based

on theoretical calculations referring to the aluminium heat sink used with a thermal conductivity of λ = 237 W/mK and volumetric heat capacity C_v = 2,422 J/cm^{3}K.

Finally, a thermal resistance between the heat sink and the ambient is implemented. This parameter is mainly the result of convection and can be defined by (4)

$$R_{amb} = \frac{1}{\alpha S_{hs}}, \tag{4}$$

where S_{hs} is the area and α is a convection coefficient in [W/m^{2}K] [15]. To calculate the R_{amb} value a one-side natural convection was assumed and as a consequence the generalized convection coefficient was set to α = 10 W/m^{2}K.

In the stable state every node has its own temperature represented by the value of voltage in the simulated circuit. More interesting for observation are transient states when the temperature of each layer changes and depends on the temperature of neighboring elements. In that case some inertia in heat transfer can occur and reaction to the control signal can be delayed. This phenomenon is similar to the example of boiling of milk. Even if the kitchen fire is already turned off, the foam will rise for the next few seconds. The described effect can be explained by the fact that milk has a stable temperature of 100°C and the heat still flows from the hotter pot or heating plate to the liquid.

A similar effect can be observed in an integrated circuit where all elements have different temperatures caused by heat dissipated in them and the temperature of the top layer is stabilized by a heat sink or other kind of cooling. At a specific moment the heat distribution between the circuit nodes is not uniform and heat flows between them. Standard thermal control of the chip includes turning off (or scaling down) power dissipation when the chip reaches a high temperature. That action results in immediate cooling of the hottest element but heat from it would flow to other ones. It means that a temperature sensor located in another (the not hottest) part of the chip would still indicate a rising temperature. This inertia of heat transfer has to be taken into account by designers of the integrated circuits working in DPM systems.

The analyzed model consisted of forty nine (square network with an edge of seven elements) identical elements with current ("power") source connected to the node *2,2* and the voltage ("temperature") value investigated in nodes *6,6* and *7,7*. Values of thermal resistance and capacitance referred to the real-world elements can be characterized by a thermal time constant of tens of seconds. The control signal which heated the circuit was a square wave representing two phases when power was and was not dissipated in the chip. The period of the wave (10 s) was calculated not to fully load capacitors so in the cooling phase heat transfer could occur. All parameters were chosen to refer to the integrated circuit used in the experiment described in the next section.

Fig. 2 presents an example of transient simulation run on the described R-C net. In the first phase some power is dissipated in node *2,2* (top graph). As a result the temperature is rising from an initial temperature (35˚C represented by 35 V) both at the heated node (upper line at bottom graph) and tested nodes (lower lines at bottom graph). When heating of node *2,2* stops at time t = 5 s the temperature of this node starts to drop but the temperature of other nodes is still rising for a significant period of time (above 1 s). That can be considered as an example that the described phenomena can take place in integrated circuits. The next section will describe a similar effect observed in a real integrated circuit.

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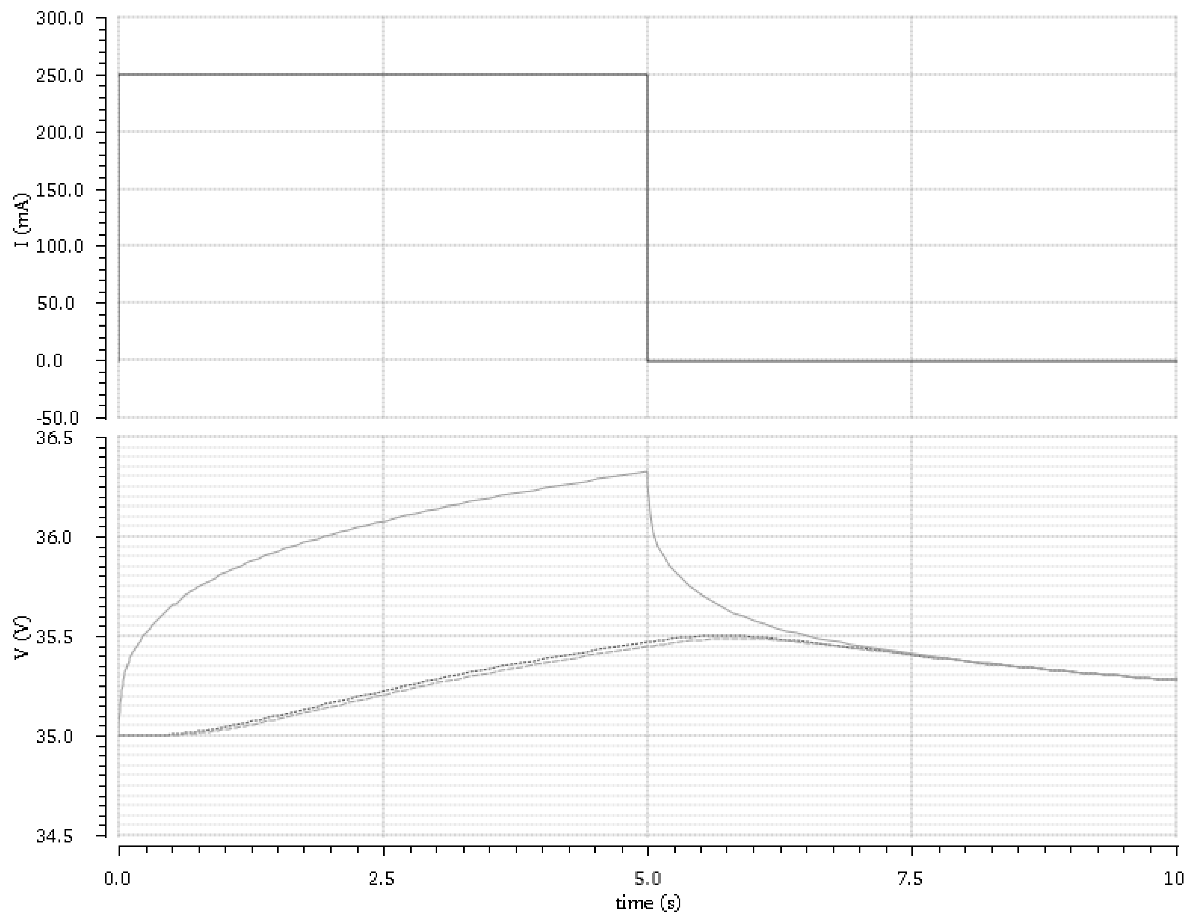

Fig. 2. Transient simulation result for thermal model: dissipated power at node 2,2 (top graph), temperature in heated node 2,2 (bottom graph, upper line) and temperature in tested nodes 6,6 and 7,7 (bottom graph, lower lines).

The presented compact model does not fully represent the complex structure of the real integrated circuit. In the described case of thermal inertia phenomenon the only part relevant for consideration is the spatial distribution of heat on the surface of the silicon die. The presented model consists only of the elements which are needed for clear and legible visualization of the described phenomenon. Elements whose influence was small or not relevant for the thesis and only made the structure less intuitive for analysis were neglected or simplified. As a result some differences between simulation and measurements have to occur. The aim of the model is to present that case of thermal inertia phenomenon when the temperature of some parts of the integrated circuit rises despite no active heat sources at the moment can occur in the chip and to explain it, not to exactly copy the situation presented in the section about the experiment. The overall behavior of both simulation and experiment is similar enough to state that the presented compact model is not universal but sufficient for the specified case.

3. Measurements

Modeling of the heat transfer inertia phenomenon was necessary to explore conditions when this effect can occur (e.g. thermal capacitances cannot be fully loaded) but are not an unquestionable proof that this phenomenon would also take place in real integrated circuits. For that reason some tests had to be made to confirm the theory by obtaining results from real-world measurements.

The chip [16] used for tests was designed in CMOS 0.7 µm technology with 5 V supply. Its layout is presented in Fig. 3. The chip consists of 15 temperature sensors (marked 'S' in the figure) distributed regularly on the integrated circuit surface and 8 different heat sources. Four digital ('D') sources are a series of CMOS inverters while analogue ones ('A') are NMOS transistors with quite big gate area to conduct a large current. In case of digital sources the static power losses can be neglected (they are very small in CMOS circuits) and only dynamic losses while switching the gate should be taken into account. Such 'heat source' would produce rapid and short peaks and could be used in thermal tests of digital circuits but would not be efficient enough in the presented experiment. Four analogue sources, when turned on, conduct quite a large current and as an effect dissipate up to about 260 mW at the maximally allowed control voltage. Such amount of power is sufficient for the test purposes so these analogue parts will be used in the presented experiment.

The temperature sensors used in presented chip were CMOS PTAT (Proportional To Absolute Temperature) sensors built of five MOS transistors, two planar PNP transistors and two resistors made of highly resistive polysilicon, as presented in Fig. 4a. Such a sensor produces an output voltage proportional to the present chip temperature corresponding to (5) where W_i are MOS transistors widths, k is Boltzmann's constant, T is chip temperature, q is the charge and n is the ratio between emitter areas of planar transistors. In the presented case the emitters area multiplication factor is $n = 2$. The main advantage of the presented PTAT sensor structure is its linear characteristic. The most important constraint is current conducted by the sensor to prevent self-heating. The sensors had to be calibrated before first use and their measured characteristics are presented in Fig. 4b. The spread of characteristics is a result of inaccuracy of the fabrication process and chip layout design. Proper curve parameters for each sensor had to be implemented in the application which was used in the experiment and will be described in the next part of the paper.

$$V_{PTAT} = \frac{W_5}{W_2} \frac{kT}{q} \ln(n) \frac{R_2}{R_1}. \tag{5}$$

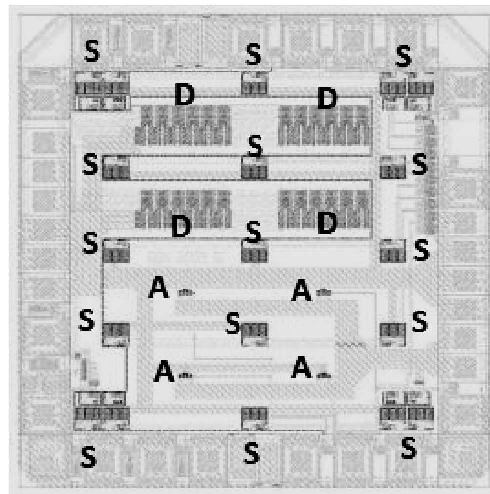

Fig. 3. Layout of the test chip.

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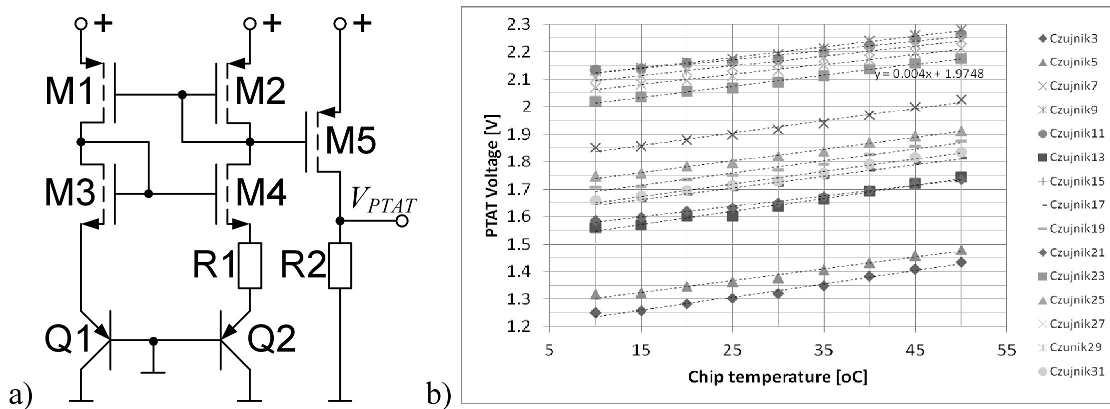

Fig. 4. Schematic diagram of the PTAT sensor (a) and characteristics of all the sensors from the tested chip (b).

The temperature measured inside the integrated circuit under test was read by an analog-to-digital converter built-in in the EFM32G890F128 microcontroller and converted into digital form for further processing. The result was sent via RS232 protocol to the PC with LabView application for acquisition and visualization of the data. The resolution of the conversion was 12 bit what gave a temperature measurement resolution of about 0.15°C. The sample rate and conversion speed were not very relevant due to large thermal time constants so they could be traded for better accuracy of the measurement. The temperature sensors in the test chip were multiplexed by the microcontroller. At the moment the value produced by only one sensor was read and sent to the application together with the proper sensor number. When the measurement was already done the controller switched the sensor address and data from the next sensor was processed. The structure of the described test system is presented in Fig. 5 while Fig. 6 presents a picture of the test board with the equipment used for measurements. Elements of the test system are marked as: 1 – power supply; 2 – integrated circuit under test; 3 – IC control board; 4 – microcontroller; 5 – PC with LabView application.

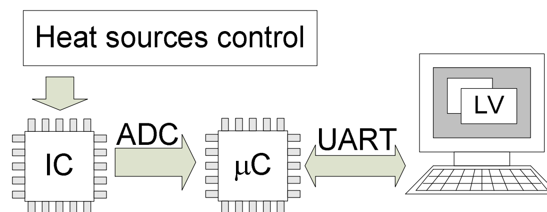

Fig. 5. Schematic diagram of the system for measurement verification.

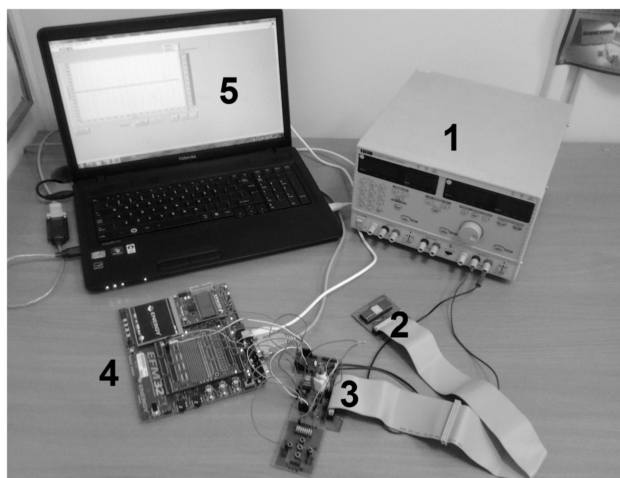

Fig. 6. Picture of the laboratory test system.

The performed tests included repeating phases of dissipating the maximum possible amount of power in the chip and waiting until it will cool down. The control signal was a voltage square wave connected to the gates of the transistors acting as heat sources. In the effect they were turned on and off repeatedly. In the described case the measurements from two temperature sensors will be presented: one located in the middle of the heat sources and one located near the edge of the circuit, possibly far from the heat sources. Measurements done by other sensors are not plotted for better clarity of the graph. Main difficulty in this test was the quite noisy environment. There were several important sources of noise, including temperature sensors output and analogue to digital conversion noise. Precise filtering of these distortions or strong averaging of the samples was risky because it was crucial not to disturb system dynamics. Another difficulty was the quite large thermal time constant of the integrated circuit (in the range of tens of seconds) so measurements took quite a long time. These time constants were also the reason why such a complex measurement system had to be created instead of simple use of an oscilloscope. The next problem during tests was how to control the chip in order not to fully load the thermal capacitances what is a necessary condition to observe the heat transfer inertia. Proper test conditions were set based on conclusions led from a previously described model.

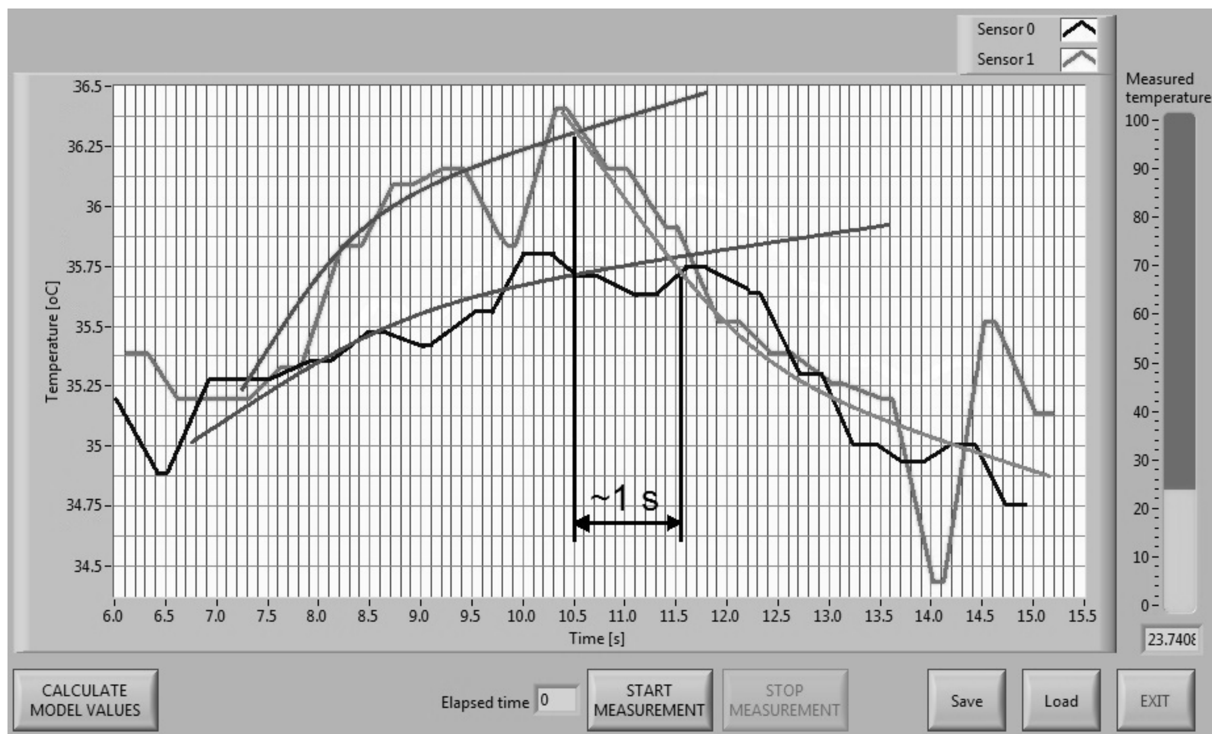

Fig. 7. Temperature of the integrated circuit measured by two sensors with heat transfer inertia marked.

Finally, Fig. 7 presents an example of the measurement results. Polygonal lines are values of temperature measured directly at two different points of the circuit under test (near and far to heat sources). The noise disturbing the measurement is clearly seen. Continuous lines which correspond to polygonal lines are approximations of the measured samples. In the first phase of this test the maximum amount of power from analogue heat sources was dissipated in the circuit so the temperature indicated by both sensors was rising. Since about the tenth second the transistors were turned off and the phase of cooling the chip began. Sensor 1, which was located near the heat sources, started to cool down immediately, while sensor 0 located in a cooler neighbourhood continued the trend of indicating temperature growth until the temperature of both parts of the circuit were approximately equal. This means

that reaction of one of the sensors to the control signal was delayed for about 1 s. The figure presented above proves that the phenomenon of heat transfer inertia can occur in integrated circuits.

4. Conclusions and summary

The paper described the phenomenon of heat transfer inertia which can be observed in integrated circuits. Some Spice models, based on electrical-thermodynamic analogy, were created and tested as an introduction to the investigation of this effect. The final step of analysis of this phenomenon were measurements of the integrated circuit with many heat sources and temperature sensors spread on its area.

Both simulation and experiment confirmed that heat transfer inertia can occur in integrated circuits. Results gathered by both methods were consistent.

Most of power management systems which are currently modeled and developed assume that reaction of the circuit to a control signal is immediate. That means that the temperature of every part of the chip would follow without any delay the action of the control system which tries to protect the circuit from overheating.

Analysis of the heat transfer inertia phenomenon shows that measuring temperature in one point of the circuit and taking action based on information from this sensor can lead to false conclusions, because lowering the temperature of this point does not mean that every other part of the circuit would also be cooled. As an effect the control systems must include information of temperature dynamics and its distribution over the integrated circuit area. It is also possible that some kind of temperature prediction which would be aware of this phenomenon could be helpful for proper control of the circuit thermal behaviour.

The presented results are planned to be taken into account in the dynamic power management system designed by the authors.

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