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Metrol. Meas. Syst., Vol. XXII (2015), No. 3, pp. 351–362.

PAN POLSKA AKADEMIA NAUK

METROLOGY AND MEASUREMENT SYSTEMS

Index 330930, ISSN 0860-8229

www.metrology.pg.gda.pl

M&MS

A NOVEL DESIGN OF AN NTC THERMISTOR LINEARIZATION CIRCUIT

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Abstract

A novel design of a circuit used for NTC thermistor linearization is proposed. The novelty of the proposed design consists in a specific combination of two linearization circuits, a serial-parallel resistive voltage divider and a two-stage piecewise linear analog-to-digital converter. At the output of the first linearization circuit the quasi-linear voltage is obtained. To remove the residual voltage nonlinearity, the second linearization circuit, *i.e.*, a two-stage piecewise linear analog-to-digital converter is employed. This circuit is composed of two flash analog-to-digital converters. The first analog-to-digital converter is piecewise linear and it is actually performing the linearization, while the second analog-to-digital converter is linear and it is performing the reduction of the quantization error introduced by the first converter. After the linearization is performed, the maximal absolute value of a difference between the measured and real temperatures is 0.014ºC for the temperature range between –25 and 75ºC, and 0.001ºC for the temperature range between 10 and 40ºC.

Keywords: linearization, NTC thermistor, piecewise linear flash analog-to-digital converter, serial-parallel resistive voltage divider.

1. Introduction

The application area of temperature measurements is very wide and it is spanning from simple ambient temperature measurements to very complex measurements that are used in advanced space or laser technology. To select an adequate temperature sensor for an application some important demands must be considered. Some of them are the measurement accuracy and resolution, sensor dimensions, easiness of installing the sensor, and interfacing it with the instrumentation system, low costs of the sensor itself and of its calibration procedure, *etc*. The performed investigations, regarding these selection criterions, have shown that for the most temperature sensing applications NTC thermistors offer the most desirable sensor features [1]. An NTC thermistor is a thermally sensitive resistor with a negative temperature coefficient, *i.e.*, its resistance decreases with the temperature increase [2]. Additionally, NTC thermistors have a wide application range due to their cost-effectiveness, ruggedness, large temperature sensitivity and accuracy, good electrical noise immunity, a wide temperature range that can be extended from −80ºC to 300ºC [2]. The particular features and advantages of NTC thermistors in comparison to other temperature sensor types are shadowed by a highly non-linear relation between the thermistor resistance and the temperature that is measured. To obtain the digital form of the measured temperature, a voltage signal proportional to the temperature must be provided. For this reason, the thermistor is put in a circuit with a constant voltage or current source. The circuit output voltage is non-linearly related to the temperature due to a non-linear relation between the thermistor resistance and the temperature. The linearization of this voltage-temperature relation has been a matter of interest for many years. As a result, a great number of linearization methods have been proposed. In this way, a possibility to choose an adequate

Article history: received on Mar. 16, 2015; accepted on May 29, 2015; available online on Sep. 21, 2015; DOI: 10.1515/mms-2015-0035.

linearization method that can provide a satisfying performance of a measurement system is offered.

Any sensor linearization method can be classified into one of the following three groups of methods: analog, digital or mixed ones [3]. The analog group of methods includes sensor linearization procedures that are performed before the analog-to-digital (A/D) conversion by using passive or active analog circuits [4–6]. The linearization procedure performed after the A/D conversion of the sensor output belongs to the digital group of linearization methods. A common method in this group applies a look-up table. The third group includes linearization methods performed during the A/D conversion. In this case, the linearization is performed with a non-linear ADC that has a non-linear transfer function inverse to the sensor transfer function (static input-output characteristic). In this way, the A/D conversion and the sensor output linearization are performed simultaneously by the same circuit [7–10].

In a paper [4], the linearization of NTC thermistor using voltage divider linearizing circuits, such as a Wheatstone bridge and a serial-parallel resistive voltage divider, is examined. The output voltage of the thermistor is modeled using the first order and the third order polynomial fitting equations. The fitting is performed between taken calibration points (input temperature, output voltage). The numerical results showed that the lowest fitting error is obtained when the output voltage of the NTC thermistor put in a serial-parallel voltage divider is modeled by using the third order polynomial fitting equation. A low cost and simple solution for the compensation of the NTC thermistor nonlinearity presents an active analog circuit proposed in [5]. The proposed circuit is composed of a stable DC voltage source, a unity-gain amplifier, a linearizing resistor connected in series with the NTC thermistor and an inverting amplifier. The unity-gain amplifier employs an operational amplifier in order to decrease the excitation voltage to avoid self-heating of the thermistor. Since the excitation voltage is negative, the inverting amplifier produces a positive voltage at its output. In addition, the output voltage increases with the temperature increase. Moreover, a proper choice of the linearizing resistance can provide linear dependence between the output voltage and the measured temperature. The relative measurement error after the linearization is ±1% for the temperature range from 30 to 120ºC, and ±0.5% for a narrower range. Another, even more simple linearizing circuit based on a combination of a serial-parallel voltage divider and an operational amplifier has been proposed in [6]. This circuit is another example of performing linearization of the NTC thermistor in the analog domain. The NTC thermistor is put in a serial-parallel resistive voltage divider, while the operational amplifier is used to increase the sensitivity and operating range of the NTC thermistor.

In [7] and [8], application of a piecewise linear ADC for the simultaneous digitalization and linearization of the sensor output is proposed. The converters proposed in these papers are composed of two flash ADCs. In particular, the first flash ADC has a piecewise linear transfer function (the output digital code in relation to the analog input voltage) that approximates the non-linear function inverse to the sensor transfer function (the output voltage in relation to the input temperature). In this way, the linearization is actually performed by the first ADC. The second flash ADC is linear and is used to reduce the quantization error introduced by the first converter. A combination of an analog and a mixed method for the NTC thermistor linearization is proposed in [9]. More precisely, the linearization is performed first by using a logarithmic amplifier that compensates the inverse exponential nature of the thermistor resistance-temperature relation. A voltage signal that is obtained at the output of the logarithmic amplifier is further linearized and digitized with a dual-slope ADC. In a paper [10], a two-phase linearization method of a sine voltage signal obtained by the rotary position encoder is proposed. At the output of the first linearization phase, which is performed using comparators, inverting amplifiers and a network of logic circuits, a pseudo-linear voltage signal is obtained.

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The pseudo-linear signal is further linearized and digitized by a two-stage piecewise linear ADC.

By considering the results obtained after application of the linearization methods that are proposed in the references listed above, an NTC thermistor linearization circuit composed of a serial-parallel resistive voltage divider and a two-stage piecewise linear analog-to-digital converter (two-stage PWL ADC) is proposed in this paper. The novelty of the proposed linearization method consists in a specific combination of two linearizing circuits that are suitable for compensation of the NTC thermistor type of non-linearity. The NTC thermistor is a part of a serial-parallel resistive voltage divider, while the two-stage PWL ADC includes two flash ADCs: the piecewise linear flash ADC and the linear flash ADC. In particular, in the two-stage PWL ADC the linearization is performed by the piecewise linear flash ADC. The piecewise linear flash ADC has a transfer function composed of linear segments that approximate the function inverse to the functional dependence of the serial-parallel resistive voltage divider output voltage on the temperature. In this way, a difference between the measured and real temperature values is reduced.

The rest of the paper is organized as follows. The NTC thermistor modeling using the Steinhart-Hart three-parameter equation is discussed in the second section of the paper. The third section of the paper presents the proposed linearization circuit. The numerical results obtained using the LabVIEW simulation software are the subject of the paper's fourth section. Presentation of the conclusions drawn after the analyses of the obtained results is given in the concluding part of the paper.

2. NTC thermistor model

As mentioned above, the NTC thermistor is a thermally sensitive resistor with the negative temperature coefficient. The change of resistance R with temperature T can be modeled, *i.e.*, approximated by the three-parameter Steinhart-Hart fitting equation [2, 11]. Steinhart and Hart proposed the fitting equation for the oceanographic range from −2 to 30ºC which was actually useful for a much wider temperature range. It is important to note that some models express better fitting accuracy than the others for a specific temperature range [1, 2]. The Steinhart-Hart fitting equation has the following form:

$$R = \exp\left[\left(x - \frac{y}{2}\right)^{\frac{1}{3}} - \left(x + \frac{y}{2}\right)^{\frac{1}{3}}\right], \tag{1}$$

$$y = \frac{\left(\mathrm{A} - \frac{1}{T}\right)}{\mathrm{C}}, \tag{2}$$

$$x = \sqrt{\left(\frac{\mathrm{B}}{3 \cdot \mathrm{C}}\right)^3 + \left(\frac{y}{2}\right)^2}, \tag{3}$$

where T is the temperature in ºK, R is the thermistor resistance in Ω and A, B and C are the Steinhart-Hart fitting parameters. To find the parameters of the Steinhart-Hart equation, at least three calibration points must be used, *i.e.*, three resistance values for three temperatures must be known. In this paper the NTC thermistor NTSD0XV103FE1B0 manufactured by *Murata* is considered [12]. Its operational range is spanning from −40ºC to 125ºC. Using three calibration points (−30ºC, 179.973 kΩ), (40ºC, 5.353 kΩ) and (110ºC, 0.527 kΩ), the Steinhart-Hart fitting parameters are calculated and are: A = 0.0011, B = $2.412 \cdot 10^{-4}$ and C = $6.2763 \cdot 10^{-8}$.

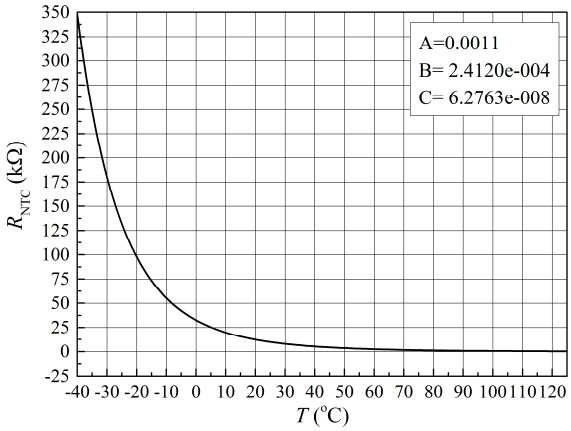

Fig. 1. The resistance-temperature relation of a NTSD0XV103FE1B0 thermistor.

The resistance-temperature relation of the considered thermistor is given by the manufacturer and presented in Fig. 1.

3. NTC thermistor linearization using the proposed circuit

3.1. The serial-parallel resistive voltage divider linearization circuit

The simplest circuit for the NTC thermistor linearization is a serial resistive voltage divider that contains the thermistor and has a constant non-standard voltage source. This circuit is shown on the left side of Fig. 2. The voltage U_1, obtained at the circuit output, is quasi-linear and has one inflection point [2, 6]. For the considered thermistor, the inflection point is set to correspond to 25ºC. In other words, this voltage expresses the highest linearity around 25ºC. By changing the position of inflection point we can change the temperature range where the voltage linearity is the most expressed. A disadvantage of this circuit is a non-standard voltage source E_1. To overcome this drawback conversion to the serial-parallel resistive voltage divider that employs a standard voltage source of 5 V is performed [2, 6]. On the right side of Fig. 2 the serial-parallel resistive voltage divider is presented.

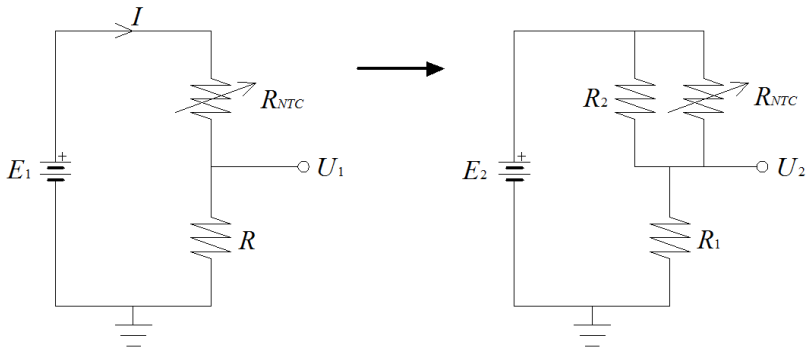

Fig. 2. Conversion from the serial voltage divider circuit (left) with a non-standard voltage source E_1 to the serial-parallel voltage divider circuit (right) using a standard voltage source $E_2 = 5$V.

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To convert the serial to the serial-parallel resistive voltage divider circuit, the parameters related to the serial voltage divider (I, R, E_1) must be determined. For the considered NTC thermistor, the dissipation constant is $C_d = 2.1$ mW/ºC and the thermistor resistance at 25ºC is $R_{NTC}(25ºC) = 10$ kΩ. By taking into consideration the condition that the self-heating error ΔT of the thermistor does not exceed 0.05ºC [1, 2, 4], a permissive operating current I of the thermistor at 25°C can be determined:

$$I = \sqrt{\frac{C_d \cdot \Delta T}{R_{NTC}\left(25^\circ C\right)}} = 0.1\,\text{mA}. \tag{4}$$

The constant resistance of the resistor R is calculated from the condition which implies that the second derivative of the voltage U_1 in relation to the temperature is equal to zero:

$$\frac{\partial^2 U_1(T)}{\partial T^2} = 0. \tag{5}$$

The previous condition governs that the output voltage U_1 will be linear in a narrow temperature range that is symmetrical around 25ºC (inflection point). From the condition (5), the expression for the resistance R can be derived and its value can be determined as follows:

$$R = R_{NTC}\left(25^\circ C\right) \cdot \frac{\beta - 2T}{\beta + 2T},\ T = 25^\circ C, \tag{6}$$

$$R = 9.747\,\text{k}\Omega. \tag{7}$$

As it can be seen from (6), the parameter β figures and represents the material constant that indicates the relationship of the thermistor material resistivity to the temperature [2]. For the considered thermistor, β is equal to 3900ºK [12]. Now, that the thermistor permissive operating current I and the value of the resistor R are known, the value of the non-standard voltage source E_1 can be calculated:

$$E_1 = I \cdot \left(R_{NTC}\left(25^\circ C\right) + R\right) = 1.9747\,\text{V}. \tag{8}$$

Since the obtained value is not a standard value for the voltage source, the serial voltage divider circuit is converted to the serial-parallel voltage divider that employs a standard voltage source $E_2 = 5$ V. By observing the right side of Fig. 2, one can conclude that an additional resistor R_2 is introduced in parallel with the thermistor R_{NTC}. In addition, the resistor R is replaced with the corresponding resistor R_1. Using the conversion equations from [2], the values of the resistors R_1 and R_2 are obtained:

$$\frac{E_1}{E_2} = \frac{R}{R_1} \Rightarrow R_1 = \frac{E_2}{E_1} \cdot R = 24.68\,\text{k}\Omega, \tag{9}$$

$$R_2 = \frac{R \cdot R_1}{R_1 - R} = 16.11\,\text{k}\Omega. \tag{10}$$

The output voltage U_2 is also quasi-linear around 25ºC, and in order to reduce its residual nonlinearity (and in this way to reduce the difference between the measured and real temperature values) an additional linearization circuit is required. For this purpose we are proposing application of a two-stage PWL ADC that is thoroughly described in the following subsection.

3.2. The two-stage piecewise linear ADC linearization circuit

As already mentioned, in order to improve the linearity of voltage U_2, it is brought to the input of the two-stage PWL ADC. The first stage flash ADC is a piecewise linear converter, *i.e.*, its transfer function represents the piecewise linear approximation of the non-linear function inverse to the function $U_2(T)$ [7, 8, 10]. The relation between the voltage U_2 and the temperature T is presented in Fig. 3a. The nonlinearity of U_2 is especially pronounced at the boundaries of the observed temperature range. Fig. 3b presents the non-linear function inverse to the function $U_2(T)$. These mutually inverse graphs are generated using the LabVIEW software for the thermistor NTSD0XV103FE1B0. In both figures the temperature range is set from −25°C to 75°C. Beside this one, three more temperature ranges are examined.

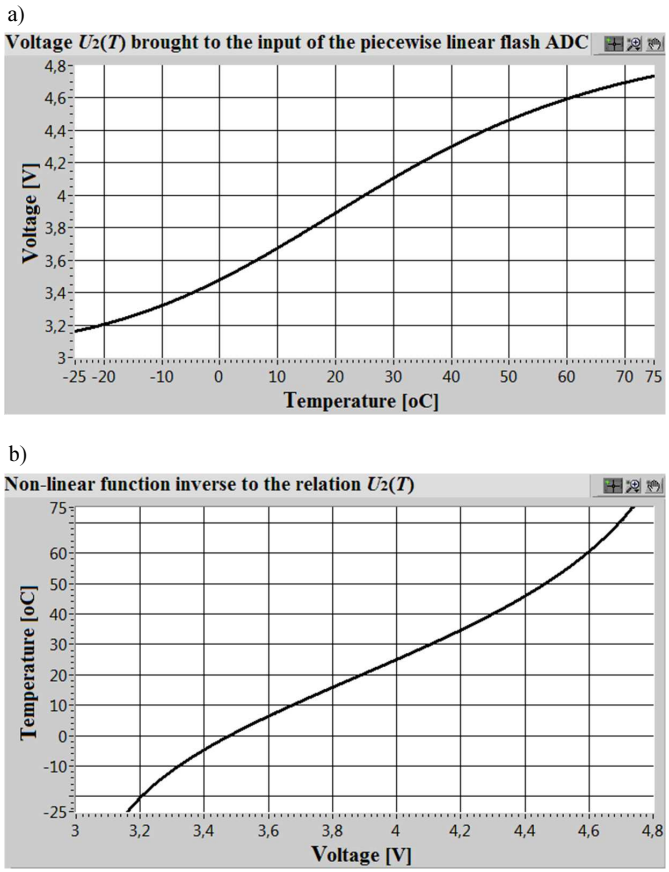

Fig. 3. a) The quasi-linear voltage $U_2(T)$ brought to the input of the two-stage PWL ADC; b) the non-linear function inverse to the relation $U_2(T)$.

The complete block diagram of the proposed linearization circuit is presented in Fig. 4. The serial-parallel voltage divider circuit with the NTC thermistor and the two-stage PWL ADC are separated by a unity-gain buffer amplifier used for impedance matching. The two-stage PWL ADC can have different combinations of resolutions N_1 and N_2 for the first and the second conversion stages, respectively, but as an example, the ADC in Fig. 4 has the 2-bit first stage and the 8-bit second conversion stage. Both stages employ flash type ADCs.

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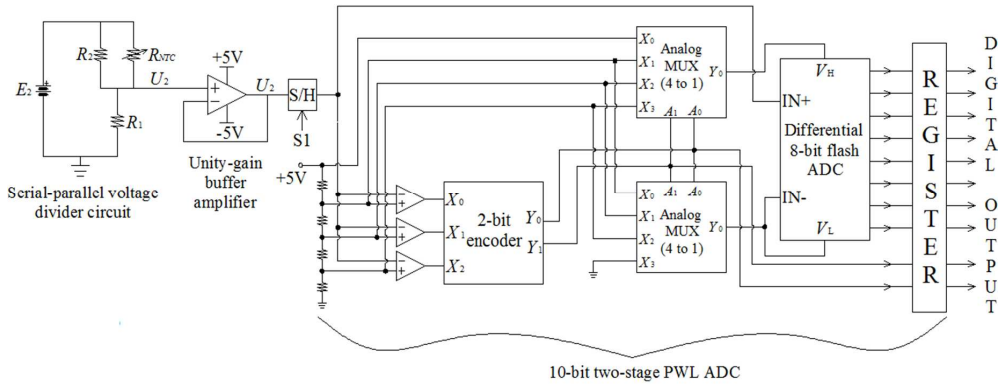

Fig. 4. A block diagram of the proposed NTC thermistor linearization circuit with a 10-bit two-stage PWL ADC.

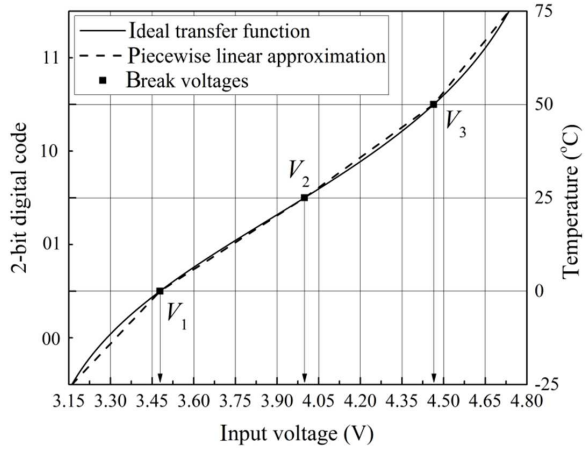

Fig. 5. The piecewise linear approximation of the ideal transfer function of the 2-bit first stage flash ADC with the break voltages V_1, V_2 and V_3.

Since the maximal value of the voltage U_2 is not higher than 5 V, the reference voltage for the first stage flash ADC is set to 5V. The first stage flash ADC converter with 2-bit resolution requires a network of four unequal resistors setting up the reference voltages for three comparators. These voltages, called the break voltages [7, 8, 10], are the boundaries of the linear segments that compose the piecewise linear transfer function of the first stage flash ADC. The 2-bit piecewise linear flash ADC transfer function is given in Fig. 5. The solid line represents the ideal transfer function that has the shape of the function presented in Fig. 3b. However, the real transfer function is composed of linear segments (the dashed lines) bounded by the break voltages V_1, V_2 and V_3 (black squares). In particular, the break voltages are non-uniformly distributed within the ADC input range due to nonlinearity of the function $U_2(T)$. These voltages correspond to the temperatures that are obtained by dividing the temperature range into $n_1 = 2^{N1}$ uniform segments. The most outer boundaries of the temperature range are not used for the calculation of the break voltages. For example, if $N_1 = 2$ bits, the temperature range from –25 to 75ºC is divided into $n_1 = 4$ segments spanning from –25 to 0ºC, 0 to 25ºC, 25 to 50ºC and from 50 to 75ºC. The break voltages are determined only for the temperatures of 0, 25 and 50ºC, *i.e.*, the number of determined voltages is 3 as is the number of comparators used for construction of the 2-bit flash ADC. The input range of the first stage ADC is determined by

the output range of the serial-parallel resistive voltage divider. Once more, the first stage ADC determines the segment to which the sample of the quasi-linear voltage U_2 belongs. The boundaries of that segment are the input range boundaries of the second flash ADC with differential inputs. Two analog multiplexers 4 to 1, put between two ADCs, are setting the boundaries of the second ADC input range that is further divided into $n_2 = 2^{N2}$ uniform cells of equal width. The second stage flash ADC reduces the quantization error introduced in the first stage of A/D conversion and determines the uniform cell within the corresponding segment to which the sample belongs. In this way the measurement resolution is increased and the measurement accuracy is improved. The digital representations of the segment and of the cell, together, represent the digital output of the two-stage PWL ADC. For the case shown in Fig. 4, the final code word is 10 bits long.

4. Simulation results and discussions

For deriving the numerical results that prove efficiency of the linearization circuit we are proposing, four different temperature ranges, symmetrical around 25°C, are examined. For each of these temperature ranges, different combinations of resolutions N_1 and N_2 are examined. As the parameter for evaluation of the residual nonlinearity after the linearization is performed, the absolute error is used:

$$E_{\text{abs}}\left[^{\circ}\text{C}\right] = \left|T_{\text{out}} - T_{\text{in}}\right|. \tag{11}$$

The parameters T_{out} and T_{in} are the temperatures at the output of the two-stage PWL ADC (measured value) and at the NTC thermistor input (real value), respectively. As given, the absolute error also represents the accuracy of the NTC thermistor after the linearization is performed, *i.e.*, it represents the difference between the measured temperature value and the real temperature value. The relative measurement error in % is also calculated:

$$E_{\text{rel}}\left[\%\right] = \frac{\left|T_{\text{out}} - T_{\text{in}}\right|}{\textit{full scale}} \cdot 100\,\%, \tag{12}$$

wherein the *full scale* represents the width of a particular temperature range. The results obtained with the simulations performed in LabVIEW software are given in Tables 1 and 2.

Let us now discuss the obtained results. The second columns in both tables contain the results obtained when the linearization with the first stage piecewise linear flash ADC is not performed, *i.e.*, when $N_1 = 0$. In particular, these results correspond to the case when the linearization is performed only with the serial-parallel resistive voltage divider. As it can be seen from Tables 1 and 2, the maximal absolute error and the maximal relative error are decreasing as the temperature range narrows. When the linearization with the piecewise linear flash ADC is performed, different combinations of resolutions N_1 and N_2 produce different results.

Table 1. The maximal absolute error in [°C] with and without the linearization performed by the two-stage PWL ADC.

	Without linearization N_1[bit] N_2[bit]	**With linearization N_1[bit] N_2[bit]**							
Temperature range [°C]	N_1 =0 N_2 = 16	N_1 = 2 N_2 = 10	N_1 = 2 N_2 = 12	N_1 = 2 N_2 = 14	N_1 = 4 N_2 = 8	N_1 = 4 N_2 = 10	N_1 = 4 N_2 = 12	N_1 = 6 N_2 = 8	N_1 = 6 N_2 = 10
–25–75	7.85	2.598	2.588	2.586	0.22	0.211	0.209	0.017	0.014
–15–65	5.006	1.314	1.308	1.306	0.115	0.109	0.107	0.009	0.007
0–50	1.904	0.39	0.386	0.384	0.033	0.028	0.027	0.003	0.002
10–40	0.658	0.108	0.106	0.105	0.011	0.008	0.008	0.002	0.001

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Table 2. The maximal relative error in [%] with and without the linearization performed by the two-stage PWL ADC.

	Without linearization N_1[bit] N_2[bit]	**With linearization N_1[bit] N_2[bit]**							
Temperature range [°C]	$N_1 = 0$ $N_2 = 16$	$N_1 = 2$ $N_2 = 10$	$N_1 = 2$ $N_2 = 12$	$N_1 = 2$ $N_2 = 14$	$N_1 = 4$ $N_2 = 8$	$N_1 = 4$ $N_2 = 10$	$N_1 = 4$ $N_2 = 12$	$N_1 = 6$ $N_2 = 8$	$N_1 = 6$ $N_2 = 10$
–25–75	7.85	2.598	2.588	2.586	0.22	0.211	0.209	0.017	0.014
–15–65	6.257	1.642	1.634	1.632	0.144	0.136	0.134	0.012	0.009
0–50	3.807	0.779	0.771	0.769	0.066	0.057	0.055	0.006	0.004
10–40	2.192	0.361	0.352	0.350	0.035	0.028	0.025	0.006	0.002

As expected, the higher the resolution of the first ADC, the lower the errors. The second flash ADC reduces the quantization error introduced in the first conversion stage, and with the increase of resolution N_2 the errors are decreasing, but slightly. Also, for wider temperature ranges the errors are greater. For example, when $N_1 = 2$ bits and $N_2 = 12$ bits, the maximal absolute error for the widest temperature range is 2.588°C. For $N_1 = 2$ bits and $N_2 = 14$ bits the maximal absolute error is 2.586°C, *i.e.*, it is slightly lower, but for $N_1 = 4$ bits and $N_2 = 10$ bits, the error is more than 10 times lower in comparison to the case when $N_1 = 2$ bits and $N_2 = 12$ bits. By increasing the resolution N_1 to 6 bits and by reducing N_2 to 8 bits the error is reduced by another 10 times in comparison to the case when $N_1 = 4$ bits and $N_2 = 10$ bits. Therefore, with each increase of the resolution N_1 by 2 bits, the maximal absolute error is reduced 10 times. These results led us to a conclusion that the increase of the first stage ADC resolution has a greater impact on the nonlinearity reduction and the measurement accuracy improvement. However, with the increase of resolution N_1, calculation of the first stage flash ADC reference voltages becomes more complex and time-consuming. For this reason, the resolution N_1 is not greater than 6 bits.

In Fig. 6a and b the transfer function of the whole system (from the NTC thermistor input to the two-stage PWL ADC output) and the absolute error graph are presented for two different cases. Fig. 6a presents the case when the linearization is not performed with the piecewise linear flash ADC ($N_1 = 0$ bits and $N_2 = 16$ bits), and Fig. 6b presents the case when the linearization is performed using the 6-bit piecewise linear flash ADC, while the overall resolution is again 16-bits ($N_1 = 6$ bits and $N_2 = 10$ bits). The simulation results obtained for temperatures between –25 and 75°C prove the efficiency of the linearization circuit we are proposing since the maximal absolute error is reduced to 0.014°C. As the temperature range narrows the errors become lower. Therefore, for the temperatures between 10 and 40°C, when $N_1 = 6$ bits and $N_2 = 10$ bits, the maximal absolute error is the lowest and equals to 0.001°C. For example, in a paper [4], the serial-parallel voltage divider is used as the linearization circuit and the lowest absolute error obtained is 0.04°C for the temperatures between 10 and 39°C.

By comparing our results with those obtained in [4] one can conclude that the contribution of the two-stage PWL ADC to the reduction of the absolute error is significant, *i.e.*, that our proposition of a specific combination of two different linearization circuits for the NTC thermistor linearization is justified.

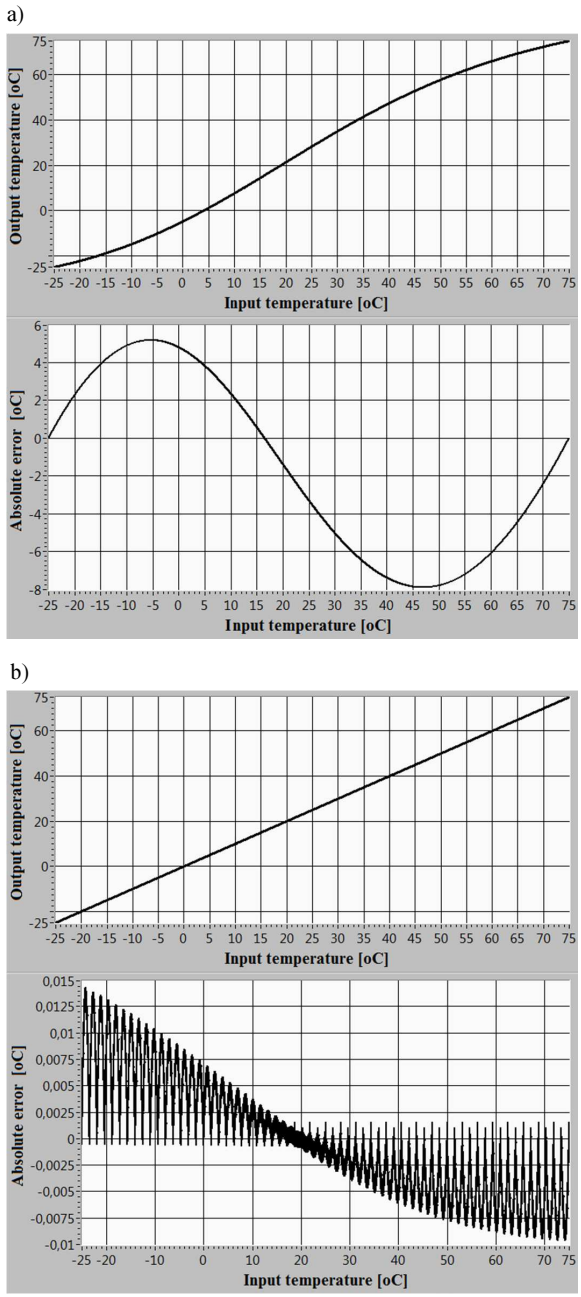

Fig. 6. The transfer function of the whole system and the absolute error [°C] for the temperature range from –25 to 75°C: a) before the linearization is performed by the two-stage PWL ADC ($N_1 = 0$ bit, $N_2 = 16$ bit); b) after the linearization is performed by the two-stage PWL ADC ($N_1 = 6$ bit, $N_2 = 10$ bit).

5. Conclusions

The NTC thermistor linearization using a serial-parallel resistive voltage divider and a two-stage PWL ADC was presented. The goal that led us to the proposition of this particular

combination of linearization circuits was the reduction of the NTC thermistor nonlinearity, *i.e.*, improvement of the NTC thermistor accuracy. At the output of the serial-parallel resistive voltage divider the quasi-linear voltage was obtained. For further linearization of this quasi-linear voltage, a two-stage PWL ADC composed of piecewise linear and linear flash ADCs was employed. The piecewise linear flash ADC transfer function is the piecewise linear approximation of the function inverse to the dependence of the quasi-linear voltage on the temperature. In other words, the linearization was performed by the piecewise linear flash ADC, and for this reason its resolution has the greatest impact on the nonlinearity reduction. In particular, the absolute value of a difference between the measured temperature value and the real temperature value was significantly reduced in comparison to the case when only the serial-parallel resistive voltage divider was used.

The most significant advantage of the proposed novel linearization circuit represents the simultaneous linearization of the NTC thermistor transfer function and digitalization of the temperature measurement results. In other words, the same circuit is used for two different and demanding processes, providing time, power and production costs savings. In addition, the serial-parallel voltage divider circuit, which contains the NTC thermistor, provides a possibility to use a standard voltage source in comparison to the serial voltage divider circuit, which is simpler but employs a nonstandard voltage source.

By changing resolutions of the two flash ADCs, the measurement accuracy can be significantly improved. The only restriction for the resolution increase represents the complexity of the break voltages calculation and adjustment of the values of resistors that compose the resistive voltage divider of the piecewise linear flash ADC. These voltages are calculated offline, *i.e.*, in accordance with the sensor transfer function that needs to be linearized. On the other hand, this means that the two-stage PWL ADC can be used for linearization of any type of a sensor.

Depending on the temperature range and on the resolutions of flash ADCs, the residual nonlinearity error can be reduced to 0.001°C. This result proves that the goal to improve the NTC thermistor accuracy was achieved.

Acknowledgements

This work was supported by the Ministry of Education, Science and Technological Development of the Republic of Serbia (grant # TR32045).

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