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Metrol. Meas. Syst., Vol. 23 (2016), No. 2, pp. 239–250.

PAN POLSKA AKADEMIA NAUK

METROLOGY AND MEASUREMENT SYSTEMS

Index 330930, ISSN 0860-8229

www.metrology.pg.gda.pl

M&MS

DIAGNOSIS OF SOFT SPOT SHORT DEFECTS IN ANALOG CIRCUITS CONSIDERING THE THERMAL BEHAVIOUR OF THE CHIP

Michał Tadeusiewicz, Stanisław Hałgas

Lodz University of Technology, Faculty of Electrical, Electronic, Computer and Control Engineering, Stefanowskiego 18/22, 90-924 Łódź, Poland (✉ michal.tadeusiewicz@p.lodz.pl, +48 42 631 2526, stanislaw.halgas@p.lodz.pl)

Abstract

The paper deals with fault diagnosis of nonlinear analogue integrated circuits. Soft spot short defects are analysed taking into account variations of the circuit parameters due to physical imperfections as well as self-heating of the chip. A method enabling to detect, locate and estimate the value of a spot defect has been developed. For this purpose an appropriate objective function was minimized using an optimization procedure based on the Fibonacci method. The proposed approach exploits DC measurements in the test phase, performed at a limited number of accessible points. For illustration three numerical examples are given.

Keywords: analog circuits, fault diagnosis, short spot defects, thermal effects.

1. Introduction

Fault diagnosis of analogue circuits is an important and still open problem for design validation of electronic devices [1–21]. Generally, fault diagnosis includes detection of the faulty circuits, location of the faulty elements, and evaluation of their parameters. If a faulty parameter drifts from its tolerance range, but does not lead to some topological changes, the fault is said to be the soft or parametric one. Most physical failures (80–90)% in integrated circuits are opens and shorts [9–10, 21]. In both CMOS and BJT circuits (70–80)% of failures are shorts and (10–20)% opens. Open and short faults, called hard faults, are extreme cases of large increase or decrease of values, which occur in actual circuits. A real open fault can be simulated by a high resistor, usually 100 kΩ – 10 MΩ, connected in series with the element or path, whereas a real short fault can be simulated by a small resistor, usually 10 Ω – 1 kΩ, connected to the pair of points. The above mentioned faults can be considered as near-opens or near-shorts [8–11, 13, 15, 21], and occur as soft spot defects. They can take the form of missing or extra materials [9]. The spot defects represent majority of IC defects that are met in their production and operation. Each of these failures changes branch currents and voltages of the circuit, that affect the power consumed by the circuit and its temperature. In consequence, the circuit parameters vary. In the reference [21] a method of spot defect diagnosing analogue circuits based on parametric characteristic tracing is proposed. The approach enables to test the circuits with multiple operating points but fails to consider the thermal effects.

In this paper a different method for detection, location and evaluation of a single soft spot short is developed. The method takes into account the technological deviations of parameters within their tolerance ranges as well as the thermal behaviour of the chip, leading to variations of the parameters in the circuit under test. They may be large and may considerably influence both the diagnostic process and the obtained results.

The diagnostic method is based on a measurement test, leading to currents flowing through some accessible branches. The values of these currents depend on the applied sources, the spot

Article history: received on Nov. 11, 2015; accepted on Feb. 06, 2016; available online on May 16, 2016; DOI: 10.1515/mms-2016-0023.

defect, and the parameters of fault-free elements. The temperature inside the chip, higher than the ambient temperature, affects these parameters and the measured currents. Thus, to operate with actual values of the parameters, the diagnostic method should take into account the thermal behaviour of the chip. This is especially important in the bipolar transistor circuits, where neglecting the temperature effects may lead to inaccurate or even wrong results. Thus, considering the thermal constraints improves reliability of the method and leads to more accurate results.

2. Diagnostic test

To diagnose a spot defect, taking into account the thermal behaviour of the chip, the test is performed as follows. The circuit is driven by m power supply sources consisting of voltage sources $E_1, \cdots, E_m$ and internal resistors $R_1, \cdots, R_m$, applied at the input nodes, and is terminated by a resistor R_o connected to the output nodes, as shown in Fig. 1. The input currents $i_1, \cdots, i_m$ and the output current i_o are measured. Their values are labelled $\bar{i}_1, \cdots, \bar{i}_m$ and $\bar{i}_o$, respectively, whereas the values of the corresponding input and output voltages are labelled $\bar{v}_1, \ldots, \bar{v}_m, \bar{v}_o$. The power consumed by the chip is given by:

$$\bar{P} = \sum_{j=1}^{m} \bar{v}_j \bar{i}_j - R_o \bar{i}_o^2 = \sum_{j=0}^{m} \left(E_j \bar{i}_j - R_j \bar{i}_j^2 \right), \tag{1}$$

where $E_o = 0$. Under the assumption that the temperature of all elements inside the chip is the same, the thermal behaviour of the chip can be analysed using the electrical analogue circuit [22–23], shown in Fig. 2. In this model the voltage is analogous to the temperature, the current is analogous to the flow of power, T_a means the ambient temperature, and R_T is the thermal resistance, including junction-to-case and case-to-ambient thermal resistances. Analysing the circuit shown in Fig. 2 gives:

$$T = T_a + R_T \bar{P}. \tag{2}$$

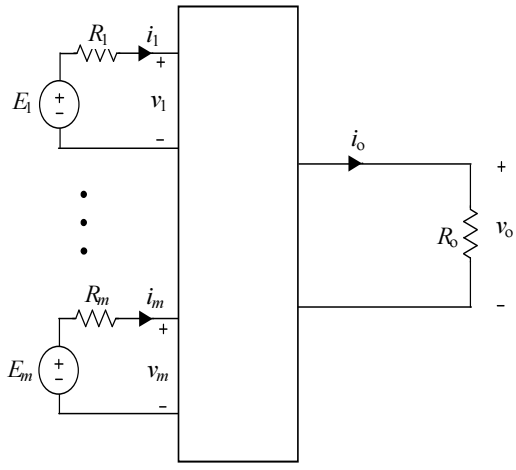

Fig. 1. Arrangement of the diagnostic test.

Given the interior temperature T, the actual parameters of the devices inside the chip can be evaluated.

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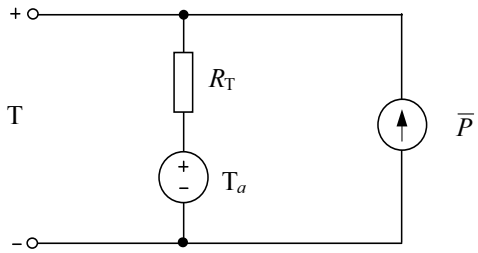

Fig. 2. The electrical analogue circuit of the chip thermal behaviour.

3. The diagnostic method

Let N_{sc} be the number of the soft spot short defects that are diagnosed. To identify the failure that actually occurs in the circuit under test and estimate its value, the diagnostic test is arranged and some simulations are performed. Each soft short is represented by a resistor having the resistance R from the range $[10\,\Omega, 1\,\mathrm{k}\Omega]$. The first part of the algorithm developed in this paper consists in location of the actual defect. For this purpose all N_{SC} soft shorts are considered in succession and in each case the function $f(R)$ is created:

$$f(R) = \sum_{j=0}^{m} \left| \bar{i}_j - i_j(R) \right|, \tag{3}$$

and $f(R) = 0$ is solved using an optimization procedure based on the Fibonacci method. The procedure finds the minimum of $f(R)$ within the range $[10\,\Omega, 1\,\mathrm{k}\Omega]$ by narrowing this range in a systematic way.

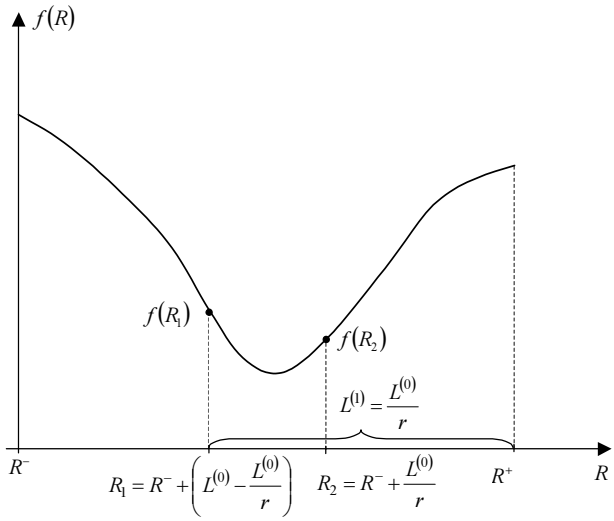

Fig. 3. Illustration of the Fibonacci method.

The basic concept of the Fibonacci method is as follows [24]. Find $R = \tilde{R}$ such that $f(R)$ is minimized over the range (R^-, R^+), where $f(R)$ is unimodal. The length of the range is labelled $L^{(0)}$. To find $\tilde{R}$ the internal points R_1 and R_2 are chosen in such a way that

$R_1 = R^- + \left(L^{(0)} - \frac{L^{(0)}}{r} \right)$, $R_2 = R^- + L^{(0)} - \left(L^{(0)} - \frac{L^{(0)}}{r} \right) = R^- + \frac{L^{(0)}}{r}$ (see Fig. 3), where r is a constant determined as described in the sequel. If $f(R_1) > f(R_2)$, as in Fig. 3, $\tilde{R}$ must lie between R_1 and R^+, forming the range (R_1, R^+) whose length is labelled $L^{(1)}$. Otherwise, *i.e.* if $f(R_1) < f(R_2)$, $\tilde{R}$ must lie between R^- and R_2. In that case the range (R^-, R_2) is considered. Next, the internal points R_3 and R_4 are selected in the range (R_1, R^+) or (R^-, R_2) using the same rules as for the range (R^-, R^+). This procedure is continued leading to the intervals $L^{(0)}, L^{(1)}, \cdots, L^{(j)}, \cdots,$, making the following assumptions. The internal points in each interval $L^{(j)}$ should be symmetrically located, so that $L^{(j)} = L^{(j+1)} + L^{(j+2)}$, $j = 0, 1, \ldots$. Moreover, the relative reduction in the size of interval, r, should be the same in each cycle, hence, $\frac{L^{(j)}}{L^{(j+1)}} = r$, $j = 0, 1, \ldots$. Under these assumptions it can be written:

$$\frac{L^{(j)}}{L^{(j+1)}} = r = \frac{L^{(j+1)} + L^{(j+2)}}{L^{(j+1)}} = 1 + \frac{1}{r}, \tag{4}$$

or

$$r = 1 + \frac{1}{r}. \tag{5}$$

The solution of (5) is $r \cong 1.618$. Thus, after k steps the obtained interval is $L^{(k)} = L^{(0)} r^{-k}$ and $\tilde{R} \in L^{(k)}$. The described search is terminated once $L^{(k)}$ is less than the required accuracy of $\tilde{R}$. This method is simple, effective, and easy to implement. It exploits the values of $f(R)$ at some points and does not require gradients at these points. In consequence, the currents $i_j(R)$, $j = 0, 1, \ldots, m$, have to be determined at these values of R. For this purpose the circuit analyses are performed.

If the function $f(R)$ is not unimodal the Fibonacci method may give an inappropriate result. Therefore, in order to increase the reliability of the optimization process, we divide the initial region into η sub-regions and apply the method in each of them.

To make possible checking whether the circuit is fault-free, N analyses of the circuit without any spot defect are performed, choosing N sets of the circuit element values (resistances and transistor parameters) selected within their tolerance ranges using the LOT selection method [25, 26]. During the analyses every time the currents $i_o, i_1, \cdots, i_m$ are computed, as long as the thermal constraints are satisfied. They enable to find the ranges $\left[i_j^-, i_j^+ \right]$, $j = 0, 1, \ldots, m$, comprising the currents of fault–free circuits.

3.1. A sketch of the algorithm

1. Choose the load resistor R_o, perform the test described in Section 2, and store the measured currents $\bar{i}_o, \bar{i}_1, \cdots, \bar{i}_m$.
2. Decide the status of the circuit. If $\bar{i}_j \in \left[i_j^-, i_j^+ \right]$, $j = 0, 1, \ldots, m$, the circuit is fault-free; otherwise it is faulty.

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3. Find the power consumed by the chip using (1) and apply (2) to determine the temperature T inside the chip. The thermal resistance of the chip can be found in catalogues (*e.g.* [22]) provided by a local sales representative, or it can be measured.
4. For each of N_{SC} potential defects find the value of the resistor that simulates the failure, corresponding to the minimum of $f(R)$. For this purpose the optimization procedure based on the Fibonacci method is used over the interval $\left[10\ \Omega, 1\ \mathrm{k}\Omega\right]$. The parameter values of fault–free elements are calculated taking into account the nominal values, updated at the temperature T determined in Step 3. If $f(R)$ (see (3)) is less than ε, where ε is a small positive number, the obtained resistance is accepted. Otherwise, the analysed failure is discarded. As a result, one or several possible defects are found and their approximate values are determined.
5. For each defect, determined in Step 4, correct the obtained resistance that simulates the failure, due to deviations of the fault-free parameters within the tolerance ranges, considering the thermal constraints. For this purpose M optimization processes are performed. In each case the parameter values are selected from their tolerance ranges using the LOT selection method [25, 26] and updated at the temperature T. Thus, the final result is one or several ranges of the spot short values. In the last case, in order to obtain a unique result, another test should be arranged, the algorithm repeated and the common part chosen.

4. Numerical examples

The diagnostic procedure was implemented in the DELPHI. The computations were executed on a PC computer with an Intel Core (TM) i7-2600 processor and 4GB RAM.

Example 1.

Let us consider the circuit, shown in Fig. 4, comprising five bipolar transistors. The transistors are represented by the Gummel-Poon model with the parameters depending on temperature according to the formulas given in the reference [27]. The nominal values of the parameters at the temperature 27ºC are as follows: BF = 400, BR = 4, CJC = $4.7\cdot10^{-12}$, CJE = $1.6\cdot10^{-11}$, IKF = 0.06, IS = $1.02\cdot10^{-14}$, ISE = $4.42\cdot10^{-12}$, NE = 2.0, NF = 1.0, NR = 1.0, RB = 3.3, RC = 0.33, RE = 0.81, TF = $4.7\cdot10^{-10}$, TR = $6.2\cdot10^{-8}$, VAF = 121, VAR = 24, XTB = 1.5.

The currents *IC* and *IB* of the Gummel-Poon model are determined by the following equations including the temperature-dependent quantities:

$$\begin{aligned} IC &= \frac{IS(\mathrm{T})}{QB(\mathrm{T})}\left(\mathrm{e}^{\frac{v_{be}}{NF\cdot VT}}-\mathrm{e}^{\frac{v_{bc}}{NR\cdot VT}}\right)-\frac{IS(\mathrm{T})}{BR(\mathrm{T})}\left(\mathrm{e}^{\frac{v_{bc}}{NR\cdot VT}}-1\right)-ISC(\mathrm{T})\left(\mathrm{e}^{\frac{v_{bc}}{NC\cdot VT}}-1\right), \\ IB &= \frac{IS(\mathrm{T})}{BF(\mathrm{T})}\left(\mathrm{e}^{\frac{v_{be}}{NF\cdot VT}}-1\right)+\frac{IS(\mathrm{T})}{BR(\mathrm{T})}\left(\mathrm{e}^{\frac{v_{bc}}{NR\cdot VT}}-1\right)+ISE(\mathrm{T})\left(\mathrm{e}^{\frac{v_{be}}{NE\cdot VT}}-1\right)+ISC(\mathrm{T})\left(\mathrm{e}^{\frac{v_{bc}}{NC\cdot VT}}-1\right). \end{aligned} \tag{6}$$

The formulas for the parameters depending on the temperature T: *IS*(T), *BR*(T), *BF*(T), *ISE*(T), *ISC*(T), *QB*(T) and *V*T are presented in the references [25, 27]. The resistances of linear resistors inside the chip are specified by:

$$R(\mathrm{T}) = R^{(\mathrm{o})}\left(1+\mathrm{T}_{C_1}(\mathrm{T}-\mathrm{T}_{\mathrm{o}})\right), \tag{7}$$

where $R^{(\mathrm{o})}$ is the resistance at $\mathrm{T_o}$, T_{C_1} is the first order temperature coefficient.

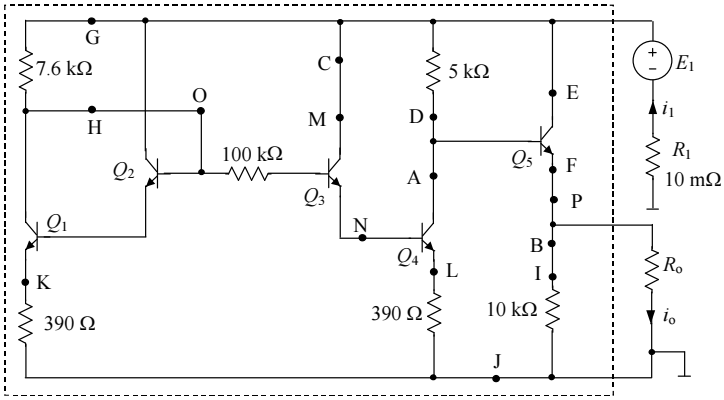

Fig. 4. The bipolar transistor circuit for Example 1.

The nominal values of resistors at the temperature 27°C are indicated in Fig. 4. The temperature coefficient of the resistors is $T_{C_1} = 2 \cdot 10^{-3} 1/K$. The thermal resistance of the chip is $R_T = 90°C/W$. Let the ambient temperature be $T_a = 27°C$, $\varepsilon = 0.001$, $N = 500$, $M = 20$. We intend to diagnose eight soft spot shorts, labelled $F_1, \cdots, F_8$, included in Table 1, and the fault-free case F_o. For this purpose a test, called Test A, is arranged as described in Section 2 with $E_1 = 12\,V$ and $R_o = 150\,\Omega$, at the accuracy of 10 μA.

Table 1. The results obtained with the proposed method using Test A.

Actual spot short	Interior temperature of the chip in °C	Possible faults indicated by the algorithm (R in Ω)
F_1 $R_{AB} = 200\,\Omega$	30.92	F_1 $R_{AB} \in [195.92 - 207.06]$
F_2 $R_{CD} = 80\,\Omega$	37.54	F_2 $R_{CD} \in [73.65 - 83.32]$ F_3 $R_{EF} \in [12.89 - 13.13]$
F_3 $R_{EF} = 50\,\Omega$	47.08	F_3 $R_{EF} \in [49.79 - 50.15]$
F_4 $R_{GH} = 500\,\Omega$	62.41	F_4 $R_{GH} \in [489.88 - 508.43]$
F_5 $R_{IJ} = 350\,\Omega$	60.51	F_5 $R_{IJ} \in [337.75 - 358.55]$ F_7 $R_{MN} \in [659.34 - 671.67]$
F_6 $R_{KL} = 20\,\Omega$	50.54	F_3 $R_{EF} \in [244.08 - 261.54]$ F_6 $R_{KL} \in [16.41 - 23.75]$
F_7 $R_{MN} = 30\,\Omega$	68.88	F_7 $R_{MN} \in [28.03 - 31.88]$
F_8 $R_{OP} = 200\,\Omega$	42.80	F_8 $R_{OP} \in [190.97 - 209.57]$

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Table 2. The results obtain with the proposed method using Test B.

Actual spot short	Interior temperature of the chip in °C	Possible faults indicated by the algorithm (R in Ω)
F_2 $R_{CD} = 80\ \Omega$	32.45	F_2 $R_{CD} \in [72.33 - 86.95]$ F_3 $R_{EF} \in [30.92 - 31.35]$
F_5 $R_{IJ} = 350\ \Omega$	43.80	F_5 $R_{IJ} \in [343.36 - 359.37]$ F_7 $R_{MN} \in [426.92 - 437.55]$
F_6 $R_{KL} = 20\ \Omega$	37.52	F_3 $R_{EF} \in [325.91 - 350.08]$ F_6 $R_{KL} \in [15.68 - 26.32]$

Table 3. The faults F_2, F_5, and F_6 obtained on the basis of Tables 1 and 2.

Actual spot short	Common parts of the sets provided by Tables 1 and 2
F_2 $R_{CD} = 80\ \Omega$	F_2 $R_{CD} \in [73.65 - 83.32]$
F_5 $R_{IJ} = 350\ \Omega$	F_5 $R_{IJ} \in [343.36 - 358.55]$
F_6 $R_{KL} = 20\ \Omega$	F_6 $R_{KL} \in [16.41 - 23.75]$

Let the tolerances of the basic circuit parameters be $\pm 2\%$ for the resistances and $\pm 5\%$ for the forward beta BF and the transport saturation current IS. In each of the considered cases the actual values of the circuit parameters, at the ambient temperature, are within the tolerance ranges. For a fault-free circuit the current ranges $\left[i_1^-, i_1^+\right] = [29.75, 30.18]\,\text{mA}$ and $\left[i_o^-, i_o^+\right] = [26.82, 27.13]\,\text{mA}$ have been determined using the approach described in Section 3.

In the cases of faults F_1, F_3, F_4, F_7, and F_8 the results, summarized in Table 1, are unique and correct, whereas in the cases of F_2, F_5, and F_6 the algorithm finds the actual fault and the virtual one. Therefore, the diagnosis procedure is repeated for the latter faults using another test, called Test B, with $E_1 = 6\text{V}$ and $R_o = 200\Omega$. The results are shown in Table 2. The common parts of the sets provided in both tables, corresponding to the faults F_2, F_5, and F_6, are presented in Table 3. Thus, in all the cases the algorithm gives correct results. The CPU time consumed to diagnose a spot short on the basis of one test, listed in one row of Tables 1 and 2, is less than 1 second. To thoroughly evaluate the method efficiency, 10 sets of values of the spot defects $F_1, \cdots, F_8$, comprising 80 cases, have been diagnosed. In 77 cases the final results provided by the algorithm are unique and correct. In one of the cases the algorithm fails, whereas in two cases it finds both the actual and virtual faults.

Example 2

Let us consider the circuit, shown in Fig. 5, comprising twelve bipolar transistors. The transistor model as well as the parameters, constants, and tolerances are the same as in Example 1. The nominal values of the resistors at the temperature 27ºC are indicated in the figure. We diagnose eight soft spot shorts included in Table 4. For this purpose Test A is arranged, as described in Section 2, with $E_1 = 8\text{V}$, $E_2 = 4\text{V}$, $R_o = 200\Omega$, at the accuracy of 10 μA.

For a fault-free circuit the current ranges $\left[i_1^-, i_1^+\right] = [43.69, 44.33]$ mA, $\left[i_2^-, i_2^+\right] = [15.12, 15.74]$ mA, $\left[i_o^-, i_o^+\right] = [28.58, 28.62]$ mA have been found. On the basis of Test A the proposed algorithm gives the results summarized in Table 4. In all the cases the results are unique and correct. Therefore, there is no need to arrange another test. The CPU time consumed to diagnose one spot short is less than 2 seconds.

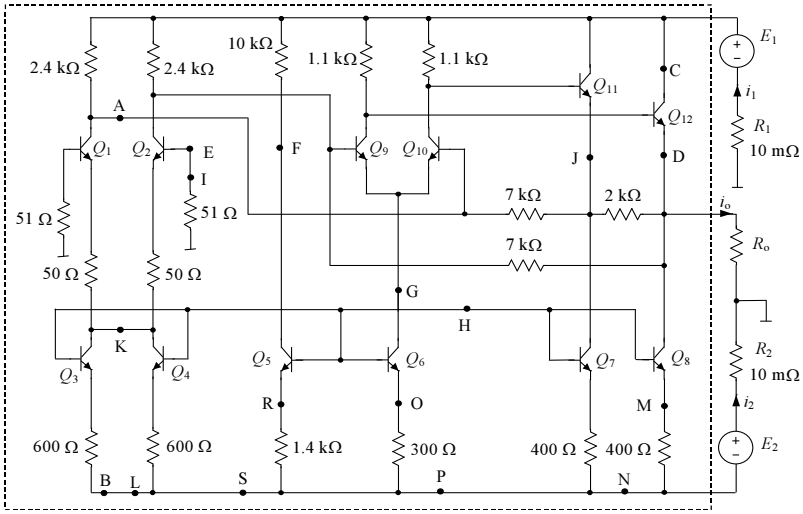

Fig. 5. The bipolar transistor circuit for Example 2.

Table 4. The results obtained with the proposed method using Test A.

Actual spot short	Interior temperature of the chip in °C	Possible faults indicated by the algorithm (R in Ω)
F_1 $R_{AB} = 200\ \Omega$	59.80	F_1 $[196.27 - 202.37]$
F_2 $R_{CD} = 70\ \Omega$	51.47	F_2 $[68.85 - 71.16]$
F_3 $R_{EF} = 120\ \Omega$	73.03	F_3 $[106.13 - 128.61]$
F_4 $R_{GH} = 400\ \Omega$	60.27	F_4 $[352.53 - 454.95]$
F_5 $R_{IJ} = 150\ \Omega$	52.45	F_5 $[142.84 - 158.95]$
F_6 $R_{KL} = 40\ \Omega$	81.62	F_6 $[38.47 - 41.46]$
F_7 $R_{MN} = 120\ \Omega$	61.51	F_7 $[116.68 - 123.80]$
F_8 $R_{OP} = 50\ \Omega$	58.03	F_8 $[48.78 - 50.82]$
F_9 $R_{RS} = 500\ \Omega$	39.08	F_9 $[490.11 - 510.81]$

The algorithm developed in this paper is mainly oriented towards the circuits comprising bipolar transistors. The circuits of this class contain resistors and BJTs, and consume rather

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large power. In that case the thermal behaviour of the chip considerably affects the parameter values. Neglecting the thermal effects may lead to inaccurate or even wrong results. To confirm this fact all the spot shorts F_1 – F_8 in Example 1 have been diagnosed neglecting the thermal constraints, using the parameters at the temperature 27°C. For the defects F_1, F_2, F_3, F_5 the method provides accepted results. For the F_4 and F_7 ones the method does not find defects within the range $[10\,\Omega, 1\,\mathrm{k}\Omega]$. For the defect F_6 the determined range [24.5–30.6] Ω is inaccurate, whereas for F_8 the found range [59.7–77.5] Ω is wrong.

CMOS circuits, as a rule, do not contain resistors and the parameters of MOS transistors slightly depend on the temperature. In consequence, influence of the self heating of the chip on the parameter values in the DC state is marginal. The numerical experiments show that, in this case, the algorithm is efficient for diagnosing the location of spot short defects of small complex circuits, but occasionally the ranges of parameter values may be considerably overestimated. This is illustrated by the following example.

Example 3

The CMOS circuit shown in Fig. 6 is made in 0.5 μm technology. MOS transistors are characterized using the Level 3 model, implemented in IsSPICE 4 [27]. The parameters of the model depend on the temperature, as described in [28]. The tolerances of the main parameters (KP, VTO, TOX) and the resistor R are ±2%, the tolerance of the channel length is $\pm 0.02 L_{\min}$ and of the channel width – $\pm 0.02 L_{\min}$, where $L_{\min}$ is equal to 1 μm. Eight soft spot short defects are considered (see Table 5). The algorithm developed in this paper correctly identifies all faults, but some ranges of the provided parameter values are overestimated. The results are shown in Table 5.

Note

In all the cases discussed in this section the proposed algorithm correctly identifies the fault-free circuits.

Table 5. The results obtained with the proposed algorithm.

Actual spot short	**Interior temperature of the chip in °C**	**Possible faults indicated by the algorithm (R in Ω)**
F_1 $R_{AB} = 220\ \Omega$	27.14	F_1 $R_{AB} \in [72.63 - 341.80]$
F_2 $R_{CD} = 50\ \Omega$	27.00	F_2 $R_{CD} \in [47.23 - 51.68]$
F_3 $R_{EF} = 20\ \Omega$	28.15	F_3 $R_{EF} \in [19.96 - 20.04]$
F_4 $R_{GH} = 80\ \Omega$	29.73	F_4 $R_{GH} \in [80.33 - 86.42]$
F_5 $R_{IJ} = 150\ \Omega$	30.47	F_5 $R_{IJ} \in [141.99 - 156.18]$
F_6 $R_{KL} = 600\ \Omega$	34.35	F_6 $R_{KL} \in [580.21 - 686.11]$
F_7 $R_{MN} = 40\ \Omega$	28.55	F_7 $R_{MN} \in [10.00 - 122.11]$
F_8 $R_{OP} = 400\ \Omega$	33.15	F_8 $R_{OP} \in [400.37 - 402.97]$

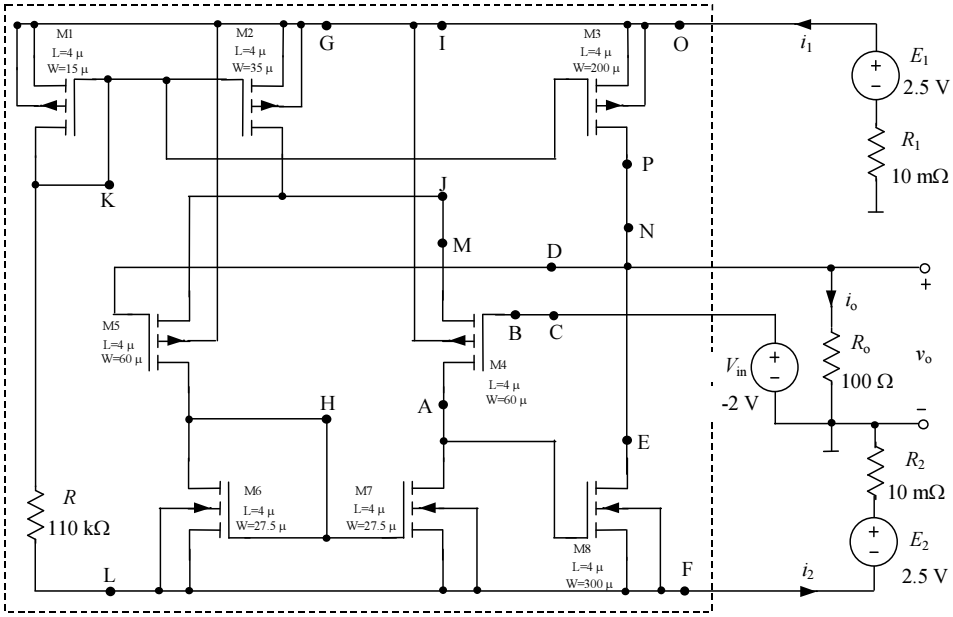

Fig. 6. The CMOS circuit for Example 3.

5. Conclusion

The paper deals with local soft spot short defects that represent majority of failures met in production and operation of integrated circuits. The proposed method of diagnosing a single soft short defect, taking into account the thermal behaviour of the chip, is simple and easy to implement. The thermal effect significantly influences the parameters of circuits considered as fault – free ones, for the circuits comprising bipolar transistors. Thus, neglecting this influence, the results provided by the diagnostic method may be inaccurate or even wrong. The provided examples of BJTs and other circuits show that the proposed approach is an efficient tool for location of the faulty parameters and estimation of their values. For CMOS circuits, the parameters slightly depend on the thermal effects in the DC state. The proposed method has the following limitations. The method is mainly dedicated to diagnosing spot shorts. Diagnosis of spot open defects needs more restrictive requirements of the measurement accuracy and the parameter tolerances, which are difficult to meet in real conditions. For CMOS circuits the method can be applied only to small complex circuits and it occasionally gives overestimated results. The main cost of implementation of the method for diagnosing CMOS circuits is the necessity of joining two environments: DELPHI - where the diagnostic method is implemented, and IsSPICE 4 – performing the circuit analyses.

Acknowledgement

This work was supported by the Statutory Activities of Lodz University of Technology I12/1/DzS/2015.

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